DATA SHEET

TDA8761A
9-bit analog-to-digital converter for digital video

Preliminary specification
File under Integrated Circuits, IC02

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Philips Semiconductors

PHILIPS

FEATURES

- 9-bit resolution
- Sampling rate up to 40 MHz
- DC sampling allowed
- One clock cycle conversion only
- High signal-to-noise ratio over a large analog input frequency range (8.2 effective bits at 10 MHz full-scale input at f_{clk} = 30 MHz)
- No missing codes guaranteed
- In range (IR) CMOS output
- CMOS compatible digital inputs
- 3 to 5 V CMOS digital outputs
- Low-level AC clock input signal allowed
- External reference voltage regulator
- Power dissipation only 165 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample-and-hold circuit required.

APPLICATIONS

Analog-to-digital conversion for:

- Video data digitizing
- Digital Video Broadcasting (DVB)
- Cable TV.

GENERAL DESCRIPTION

The TDA8761A is a 9-bit analog-to-digital converter (ADC) for professional video and digital video set box applications. It converts the analog input signal into 9-bit binary-coded digital words at a maximum sampling rate of 40 MHz. Its linearity performance ensures the required conversion accuracy in the event of 256QAM demodulator concept and for all symbol frequencies. All digital inputs and outputs are CMOS compatible, although a low-level sine wave clock input signal is allowed.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		3.0	3.3	5.25	V
I_{CCA}	analog supply current		–	18	tbf	mA
I_{CCD}	digital supply current		–	13	tbf	mA
I_{CCO}	output stages supply current	f_{clk} = 30 MHz; ramp input	–	3	tbf	mA
INL	integral non-linearity	f_{clk} = 30 MHz; ramp input	–	±0.8	tbf	LSB
AINL	AC integral non-linearity	full-scale input sine wave; note 1	–	±0.75	tbf	LSB
		50% full-scale input sine wave; note 1	–	±0.5	tbf	LSB
DNL	differential non-linearity	f_{clk} = 30 MHz; ramp input	–	±0.3	±0.7	LSB
ADNL	AC differential non-linearity	full-scale input sine wave; note 1	–	±0.5	tbf	LSB
		50% full-scale input sine wave; note 1	–	±0.3	tbf	LSB
$f_{clk(max)}$	maximum clock frequency		40	–	–	MHz
P_{tot}	total power dissipation		–	165	tbf	mW

Note

1. f_i = 10 MHz and f_{clk} = 30 MHz; f_i = 8 MHz and f_{clk} = 20 MHz.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8761AM	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1

BLOCK DIAGRAM

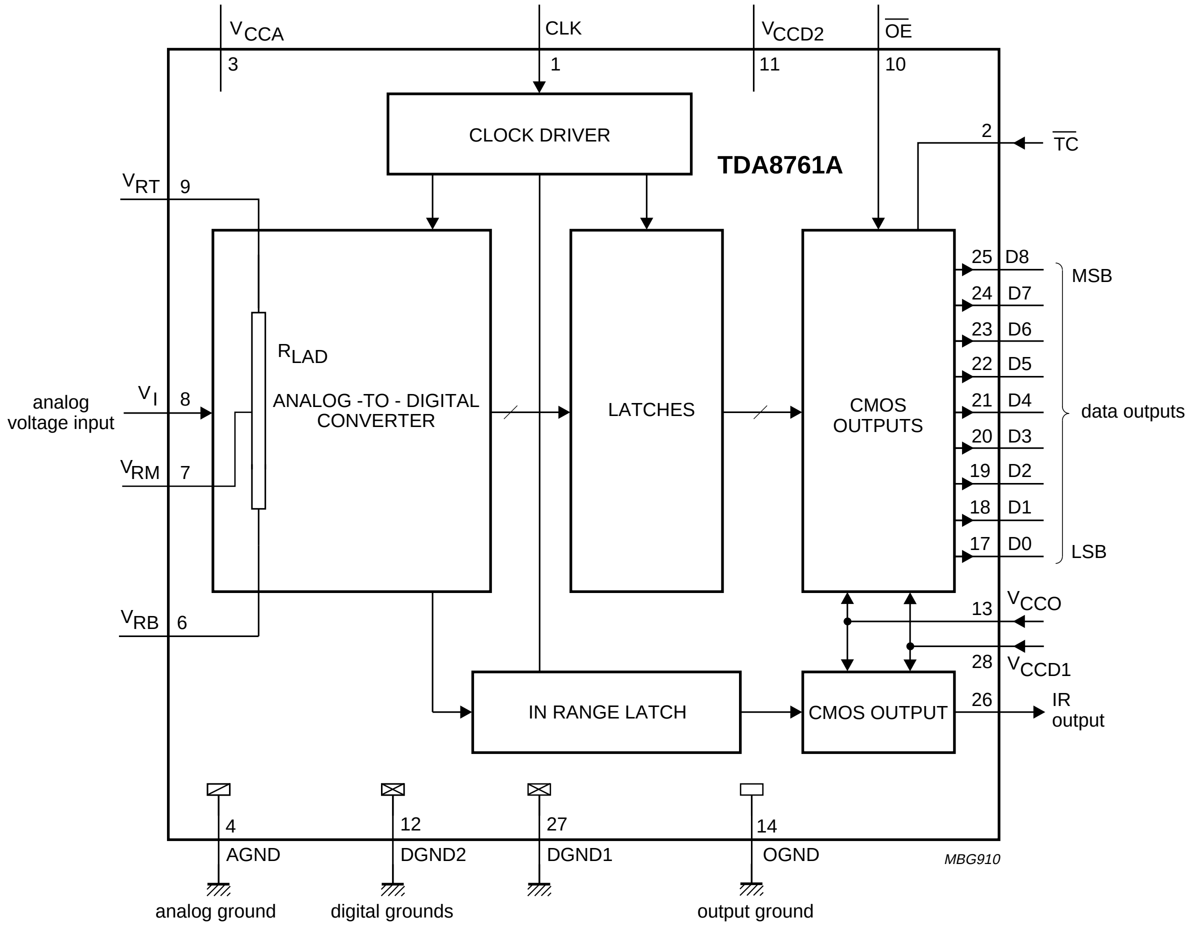


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CLK	1	clock input
$\overline{TC}$	2	two's complement input (active LOW)
V_{CCA}	3	analog supply voltage (+5 V)
AGND	4	analog ground
n.c.	5	not connected
V_{RB}	6	reference voltage BOTTOM input
V_{RM}	7	reference voltage MIDDLE
V_I	8	analog input voltage
V_{RT}	9	reference voltage TOP input
$\overline{OE}$	10	output enable input (CMOS level input, active LOW)
V_{CCD2}	11	digital supply voltage 2 (+5 V)
DGND2	12	digital ground 2
V_{CCO}	13	supply voltage for output stages (+3 to 5 V)
OGND	14	output ground
n.c.	15	not connected
n.c.	16	not connected
D0	17	data output; bit 0 (LSB)
D1	18	data output; bit 1
D2	19	data output; bit 2
D3	20	data output; bit 3
D4	21	data output; bit 4
D5	22	data output; bit 5
D6	23	data output; bit 6
D7	24	data output; bit 7
D8	25	data output; bit 8 (MSB)
IR	26	in range data output
DGND1	27	digital ground 1
V_{CCD1}	28	digital supply voltage 1 (+5 V)

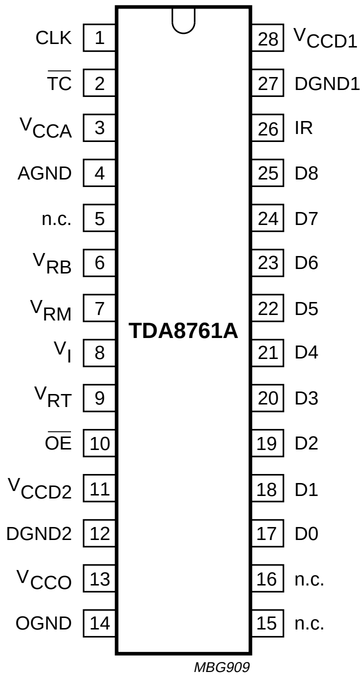


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	note 1	–0.3	+7.0	V
V_{CCD}	digital supply voltage	note 1	–0.3	+7.0	V
V_{CCO}	output stages supply voltage	note 1	–0.3	+7.0	V
ΔV_{CC}	supply voltage differences between				
	V_{CCA} and V_{CCD}		–1.0	+1.0	V
	V_{CCD} and V_{CCO}		–1.0	+4.0	V
	V_{CCA} and V_{CCO}		–1.0	+4.0	V
V_I	input voltage	referenced to AGND	–0.3	+7.0	V
$V_{i(p-p)}$	AC input voltage for switching (peak-to-peak value)	referenced to DGND	–	V_{CCD}	V
I_O	output current		–	10	mA
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
T_j	junction temperature		–	+150	°C

Note

1. The supply voltages V_{CCA}, V_{CCD} and V_{CCO} may have any value between –0.3 and +7.0 V provided that the supply voltage differences ΔV_{CC} are respected.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	110	K/W

CHARACTERISTICS

V_{CCA} = V_3 to V_4 = 4.75 to 5.25 V; V_{CCD} = V_{11} to V_{12} and V_{28} to V_{27} = 4.75 to 5.25 V; V_{CCO} = V_{13} to V_{14} = 3.0 to 5.25 V; AGND and DGND shorted together; T_{amb} = 0 to +70 °C; typical values measured at V_{CCA} = V_{CCD} = 5 V and V_{CCO} = 3.3 V; $V_{i(p-p)}$ = 1.8 V; C_L = 15 pF and T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		3.0	3.3	5.25	V
ΔV_{CC}	supply voltage differences between					
	V_{CCA} and V_{CCD}		–0.2	–	+0.2	V
	V_{CCA} and V_{CCO}		–0.2	–	+2.25	V
	V_{CCD} and V_{CCO}		–0.2	–	+2.25	V
I_{CCA}	analog supply current		–	18	tbf	mA
I_{CCD}	digital supply current		–	13	tbf	mA
I_{CCO}	output stages supply current	f_{clk} = 30 MHz; ramp input	–	3	tbf	mA
Inputs						
CLOCK INPUT CLK (REFERENCED TO DGND); note 1						
V_{IL}	LOW level input voltage		0	–	$0.3V_{CCD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{CCD}$	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{clk} = $0.3V_{CCD}$	–1	0	+1	μA
I_{IH}	HIGH level input current	V_{clk} = $0.7V_{CCD}$	–	2	10	μA
Z_i	input impedance	f_{clk} = 30 MHz	–	2	–	kΩ
C_i	input capacitance	f_{clk} = 30 MHz	–	2	–	pF
INPUTS $\overline{OE}$ AND $\overline{TC}$ (REFERENCED TO DGND); see Table 2						
V_{IL}	LOW level input voltage		0	–	$0.3V_{CCD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{CCD}$	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{IL} = $0.3V_{CCD}$	–1	–	–	μA
I_{IH}	HIGH level input current	V_{IH} = $0.7V_{CCD}$	–	–	1	μA
V_I (ANALOG INPUT VOLTAGE REFERENCED TO AGND)						
I_{IL}	LOW level input current	V_I = V_{RB} = 1.3 V	–	0	–	μA
I_{IH}	HIGH level input current	V_I = V_{RT} = 3.43 V	–	35	–	μA
Z_i	input impedance	f_i = 10 MHz	–	8	–	kΩ
C_i	input capacitance	f_i = 10 MHz	–	5	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference voltages for the resistor ladder; see Table 1						
V_{RB}	reference voltage BOTTOM		1.2	1.3	2.45	V
V_{RT}	reference voltage TOP		3.0	3.43	V_{CCA} – 0.8 V	V
V_{diff}	differential reference voltage $V_{RT} – V_{RB}$		1.8	2.13	3.0	V
I_{ref}	reference current	$V_{RT} – V_{RB}$ = 2.13 V	–	8.7	–	mA
R_{LAD}	resistor ladder		–	245	–	Ω
TC_{RLAD}	temperature coefficient of the resistor ladder		–	1860	–	ppm
			–	456	–	mΩ/K
V_{osB}	offset voltage BOTTOM	note 2	–	160	–	mV
V_{osT}	offset voltage TOP	note 2	–	160	–	mV
$V_{i(p-p)}$	analog input voltage (peak-to-peak value)	note 3	1.5	1.81	2.5	V
Outputs						
DIGITAL OUTPUTS D8 TO D0 AND IR (REFERENCED TO OGND)						
V_{OL}	LOW level output voltage	I_{OL} = 1 mA	0	–	0.5	V
V_{OH}	HIGH level output voltage	I_{OH} = –1 mA	V_{CCO}–0.5	–	V_{CCO}	V
I_{OZ}	output current in 3-state mode	0.5 V < V_O < V_{CCO}	–20	–	+20	μA
Switching characteristics						
CLOCK INPUT CLK; see Fig.4; note 1						
$f_{clk(max)}$	maximum clock frequency		40	–	–	MHz
t_{CPH}	clock pulse width HIGH		10	–	–	ns
t_{CPL}	clock pulse width LOW		10	–	–	ns
Analog signal processing						
LINEARITY						
INL	integral non-linearity	f_{clk} = 30 MHz; ramp input	–	±0.8	tbf	LSB
AINL	AC integral non-linearity	full-scale input sine wave; note 5	–	±0.75	tbf	LSB
		50% full-scale input sine wave; note 5	–	±0.5	tbf	LSB
DNL	differential non-linearity	f_{clk} = 30 MHz; ramp input	–	±0.3	±0.7	LSB
ADNL	AC differential non-linearity	full-scale input sine wave; note 5	–	±0.5	tbf	LSB
		50% full-scale input sine wave; note 5	–	±0.3	tbf	LSB
OFER	offset error	middle code; V_{RB} = 1.3 V; V_{RT} = 3.43 V	–	±1	–	LSB
GER	gain error (from device to device)	V_{RB} = 1.3 V; V_{RT} = 3.43 V; note 4	–	±0.1	–	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
BANDWIDTH (f_{clk} = 30 MHz)						
B	analog bandwidth	full-scale sine wave; note 6	–	10	–	MHz
		75% full-scale sine wave; note 6	–	14	–	MHz
		small signal at mid-scale; V_I = ±10 LSB at code 256; note 6	–	350	–	MHz
t_{STLH}	analog input settling time LOW-to-HIGH	full-scale square wave; Fig.6; note 7	–	2.0	tbf	ns
t_{STHL}	analog input settling time HIGH-to-LOW	full-scale square wave; Fig.6; note 7	–	2.5	tbf	ns
HARMONICS (f_{clk} = 30 MHz); see Figs 7 and 8						
THD	total harmonic distortion	f_i = 10 MHz	–	–56	–	dB
SIGNAL-TO-NOISE RATIO; see Figs 7 and 8; note 8						
S/N	signal-to-noise ratio (full scale)	without harmonics; f_{clk} = 30 MHz; f_i = 10 MHz	51	53	–	dB
EFFECTIVE BITS; see Figs 7 and 8; note 8						
EB	effective bits	f_{clk} = 30 MHz				
		f_i = 4.43 MHz	–	8.7	–	bits
		f_i = 10 MHz	–	8.2	–	bits
TWO-TONE; note 9						
TTIR	two-tone intermodulation rejection	f_{clk} = 30 MHz	–	–56	–	dB
BIT ERROR RATE						
BER	bit error rate	f_{clk} = 30 MHz; f_i = 10 MHz; V_I = ±16 LSB at code 256	–	10^{-13}	–	times/ sample
DIFFERENTIAL GAIN; note 10						
G_{diff}	differential gain	f_{clk} = 30 MHz; PAL modulated ramp	–	0.5	–	%
DIFFERENTIAL PHASE; note 10						
φ_{diff}	differential phase	f_{clk} = 30 MHz; PAL modulated ramp	–	0.3	–	deg

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing (f_{clk} = 30 MHz; C_L = 15 pF); see Fig.4; note 11						
t_{ds}	sampling delay time		–	–	2	ns
t_h	output hold time		5	–	–	ns
t_d	output delay time	V_{CCO} = 4.75 V	–	13	16	ns
		V_{CCO} = 3.15 V	–	16	19	ns
C_L	digital output load		–	15	40	pF
3-state output delay times; see Fig.5						
t_{dZH}	enable HIGH		–	14	18	ns
t_{dZL}	enable LOW		–	16	20	ns
t_{dHZ}	disable HIGH		–	16	20	ns
t_{dLZ}	disable LOW		–	14	18	ns

Notes

1. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 0.5 ns.
2. Analog input voltages producing code 0 up to and including code 511:
   a) V_{osB} (voltage offset BOTTOM) is the difference between the analog input which produces data equal to 00 and the reference voltage BOTTOM (V_{RB}) at T_{amb} = 25 °C.
   b) V_{osT} (voltage offset TOP) is the difference between V_{RT} (reference voltage TOP) and the analog input which produces data outputs equal to code 511 at T_{amb} = 25 °C.
3. In order to ensure the optimum linearity performance of such converter architecture the lower and upper extremities of the converter reference resistor ladder (corresponding to output codes 0 and 511 respectively) are connected to pins V_{RB} and V_{RT} via offset resistors R_{OB} and R_{OT} as shown in Fig.3.
   a) The current flowing into the resistor ladder is $I_L = \frac{V_{RT} - V_{RB}}{R_{OB} + R_L + R_{OT}}$ and the full-scale input range at the converter, to cover code 0 to code 511, is $V_I = R_L \times I_L = \frac{R_L}{R_{OB} + R_L + R_{OT}} \times (V_{RT} - V_{RB}) = \dot{0}.852 \times (V_{RT} - V_{RB})$
   b) Since R_L, R_{OB} and R_{OT} have similar behaviour with respect to process and temperature variation, the ratio $\frac{R_L}{R_{OB} + R_L + R_{OT}}$ will be kept reasonably constant from device to device. Consequently variation of the output codes at a given input voltage depends mainly on the difference $V_{RT} - V_{RB}$ and its variation with temperature and supply voltage. When several ADCs are connected in parallel and fed with the same reference source, the matching between each of them is then optimized.
4. $GER = \frac{(V_{511} - V_0) - 1.8\ V}{1.8\ V} \times 100$
5. f_i = 10 MHz and f_{clk} = 30 MHz; f_i = 8 MHz and f_{clk} = 20 MHz.
6. The analog bandwidth is defined as the maximum input sine wave frequency which can be applied to the device. No glitches greater than 2 LSBs, neither any significant attenuation are observed in the reconstructed signal.
7. The analog input settling time is the minimum time required for the input signal to be stabilized after a sharp full-scale input (square-wave signal) in order to sample the signal and obtain correct output data.

8. Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 8K acquisition points per equivalent fundamental period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency). Conversion to signal-to-noise ratio: S/N = EB × 6.02 + 1.76 dB.
9. Intermodulation measured relative to either tone with analog input frequencies of 10.0 MHz and 10.10 MHz. The two input signals have the same amplitude and the total amplitude of both signals provides full-scale to the converter.
10. Measurement carried out using video analyser VM700A, where the video analog signal is reconstructed through a digital-to-analog converter.
11. Output data acquisition: the output data is available after the maximum delay time of t_d.

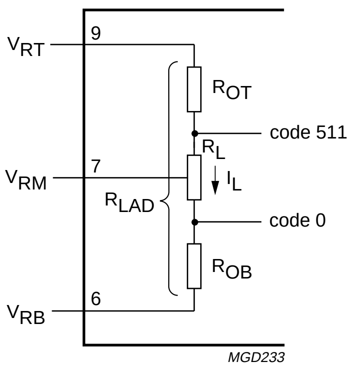


Fig.3 Explanation of note 3.

Table 1 Output coding and input voltage (typical values; referenced to AGND, V_{RB} = 1.3 V, V_{RT} = 3.43 V)

STEP	$V_{I(p-p)}$	IR	BINARY OUTPUT BITS									TWO'S COMPLEMENT OUTPUT BITS								
			D8	D7	D6	D5	D4	D3	D2	D1	D0	D8	D7	D6	D5	D4	D3	D2	D1	D0
U/F	<1.46	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1.46	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	.	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
510	.	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
511	3.27	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
O/F	>3.27	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 2 Mode selection

$\overline{TC}$	$\overline{OE}$	D8 to D0	IR
X	1	high impedance	high impedance
0	0	active; two's complement	active
1	0	active; binary	active

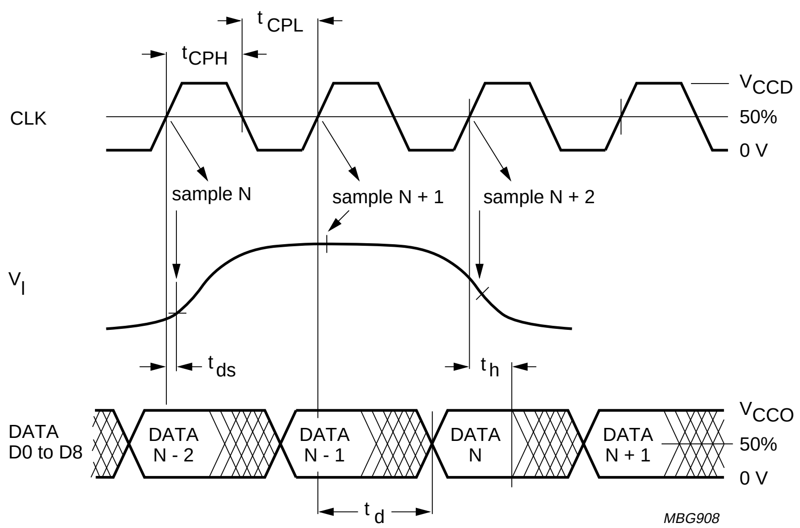
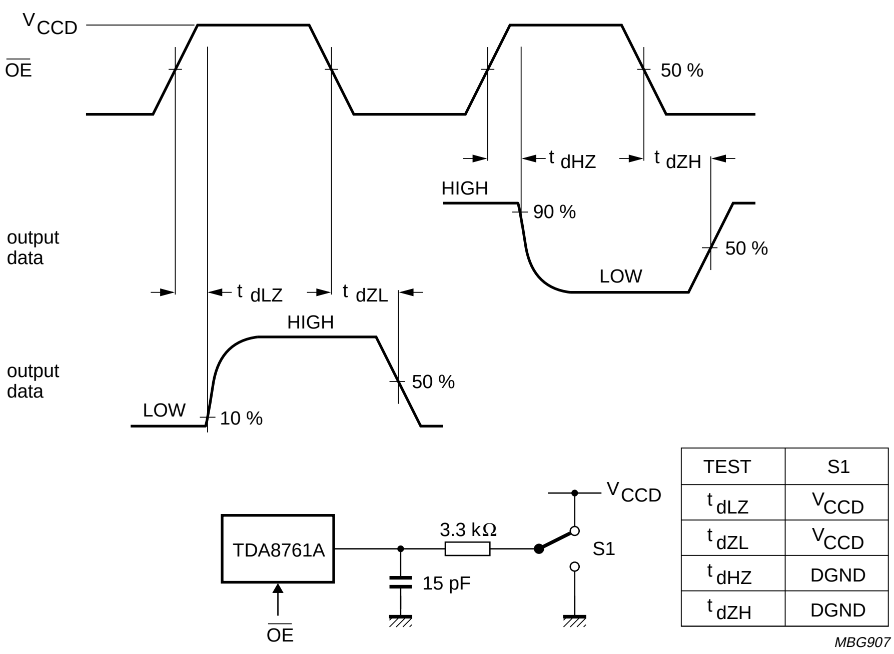


Fig.4 Timing diagram.



TEST	S1
t_{dLZ}	V_{CCD}
t_{dZL}	V_{CCD}
t_{dHZ}	DGND
t_{dZH}	DGND

$f_{\overline{OE}}$ = 100 kHz.

Fig.5 Timing diagram and test conditions of 3-state output delay time.

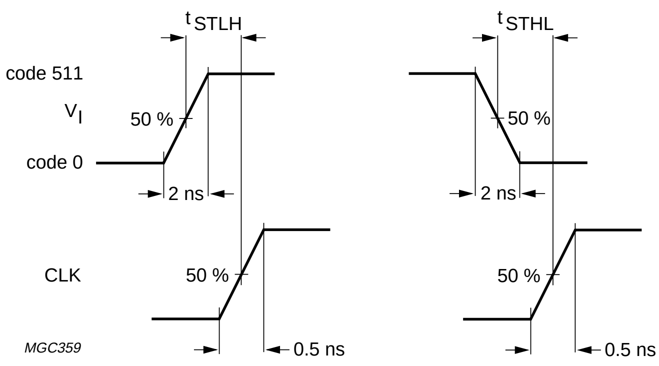
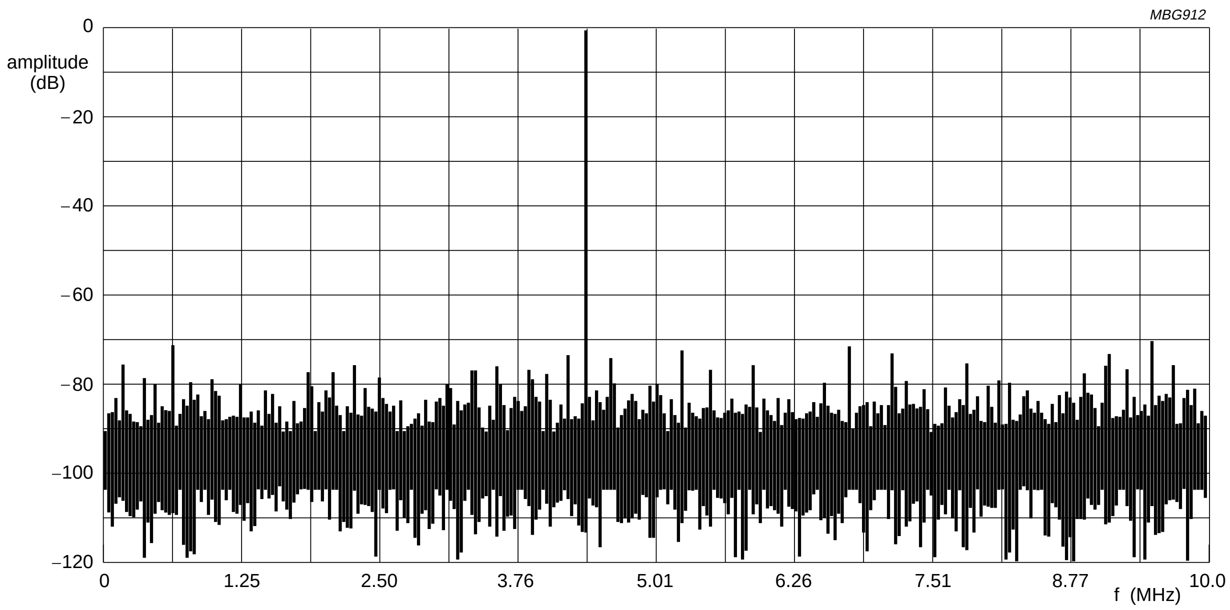
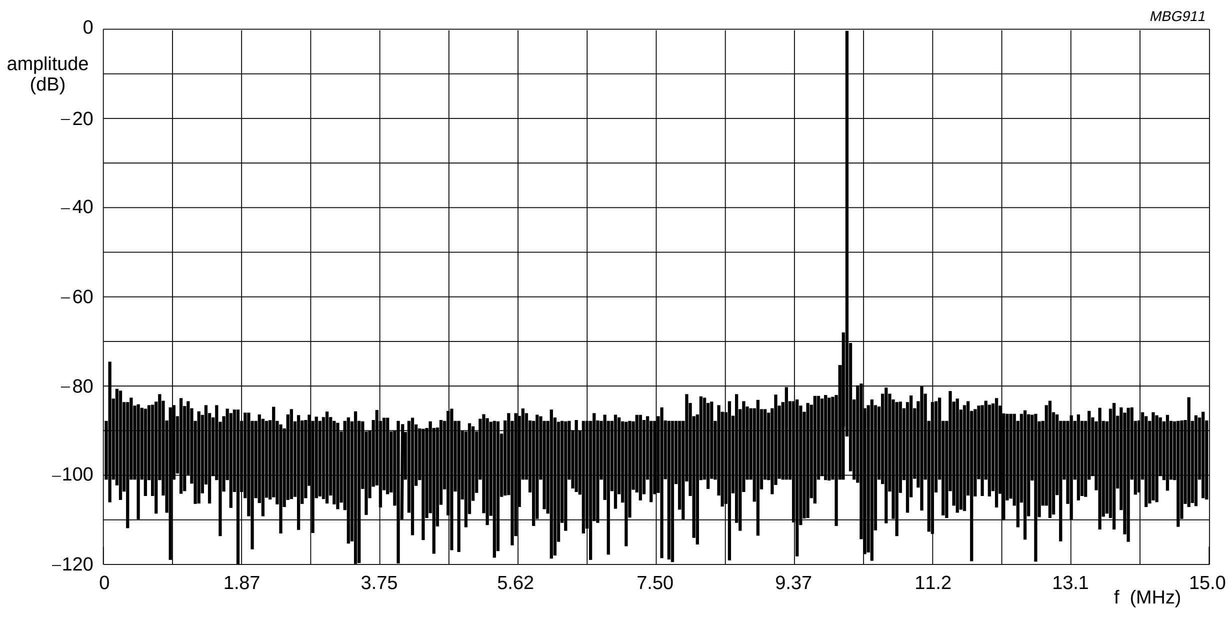


Fig.6 Analog input settling-time diagram.



Effective bits: 8.70; THD = –68.68 dB.
Harmonic levels (dB): 2nd = –78.40; 3rd = –72.08; 4th = –75.85 dB; 5th = –76.26; 6th = –80.23.

Fig.7 Typical Fast Fourier Transform (f_{clk} = 30 MHz; f_i = 4.43 MHz).



Effective bits: 8.25; THD = –56.72 dB.
Harmonic levels (dB): 2nd = –62.21; 3rd = –58.58; 4th = –80.29; 5th = –71.71; 6th = –72.04.

Fig.8 Typical Fast Fourier Transform (f_{clk} = 30 MHz; f_i = 10 MHz).

INTERNAL PIN CONFIGURATIONS

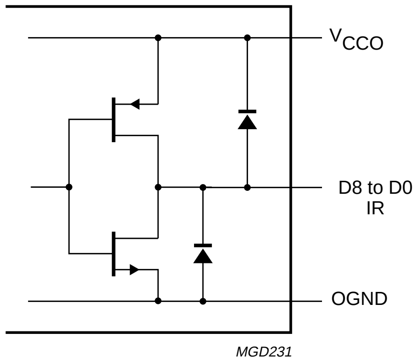


Fig.9 CMOS data and in range outputs.

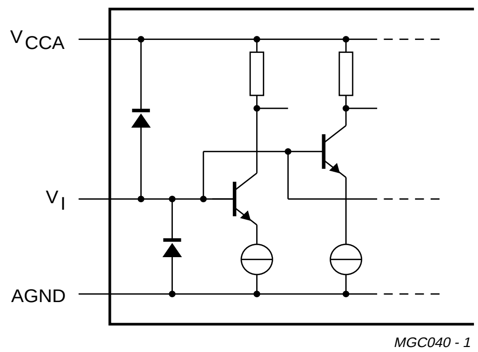


Fig.10 Analog inputs.

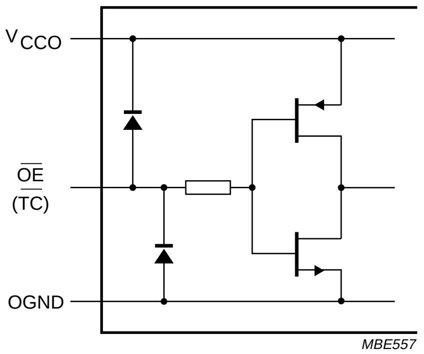


Fig.11 $\overline{OE}$ ($\overline{TC}$) input.

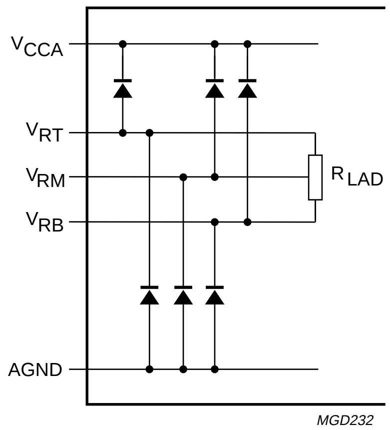


Fig.12 V_{RB}, V_{RM} and V_{RT}.

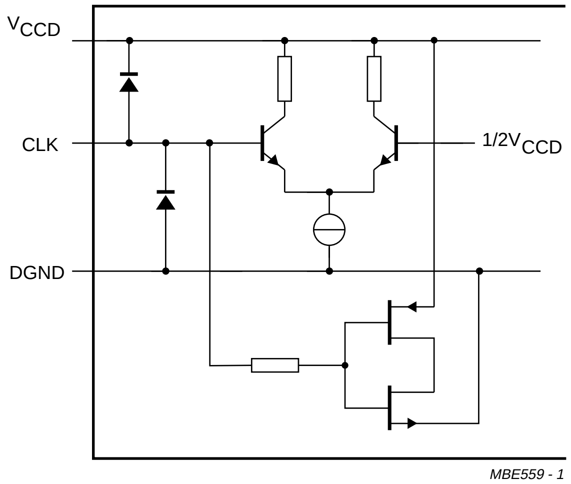
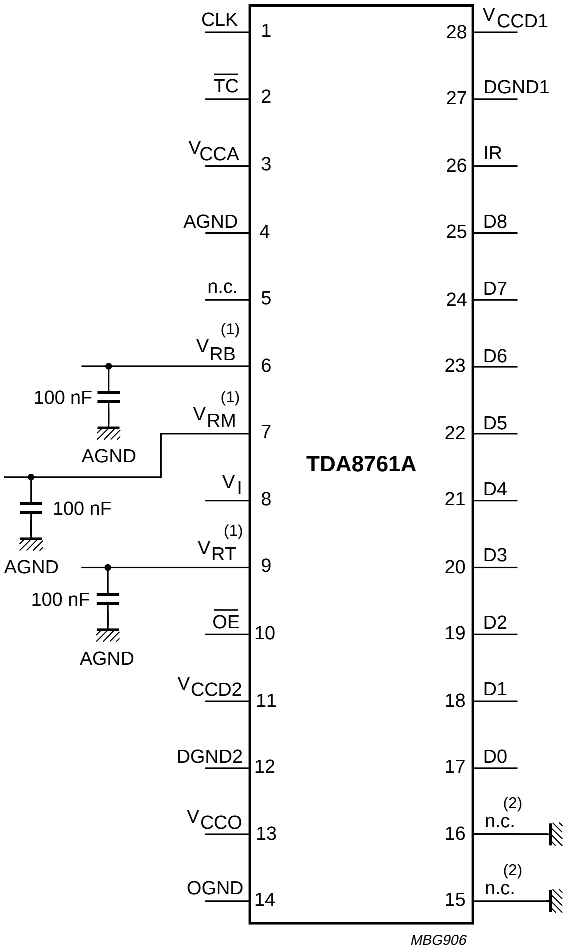


Fig.13 CLK input.

APPLICATION INFORMATION



The analog and digital supplies should be separated and decoupled.

The external voltage regulator must be built such that a good supply voltage ripple rejection is achieved with respect to the LSB value. Eventually, the reference ladder voltages can be derived from a well regulated V_{CCA} supply through a resistor bridge and a decoupled capacitor.

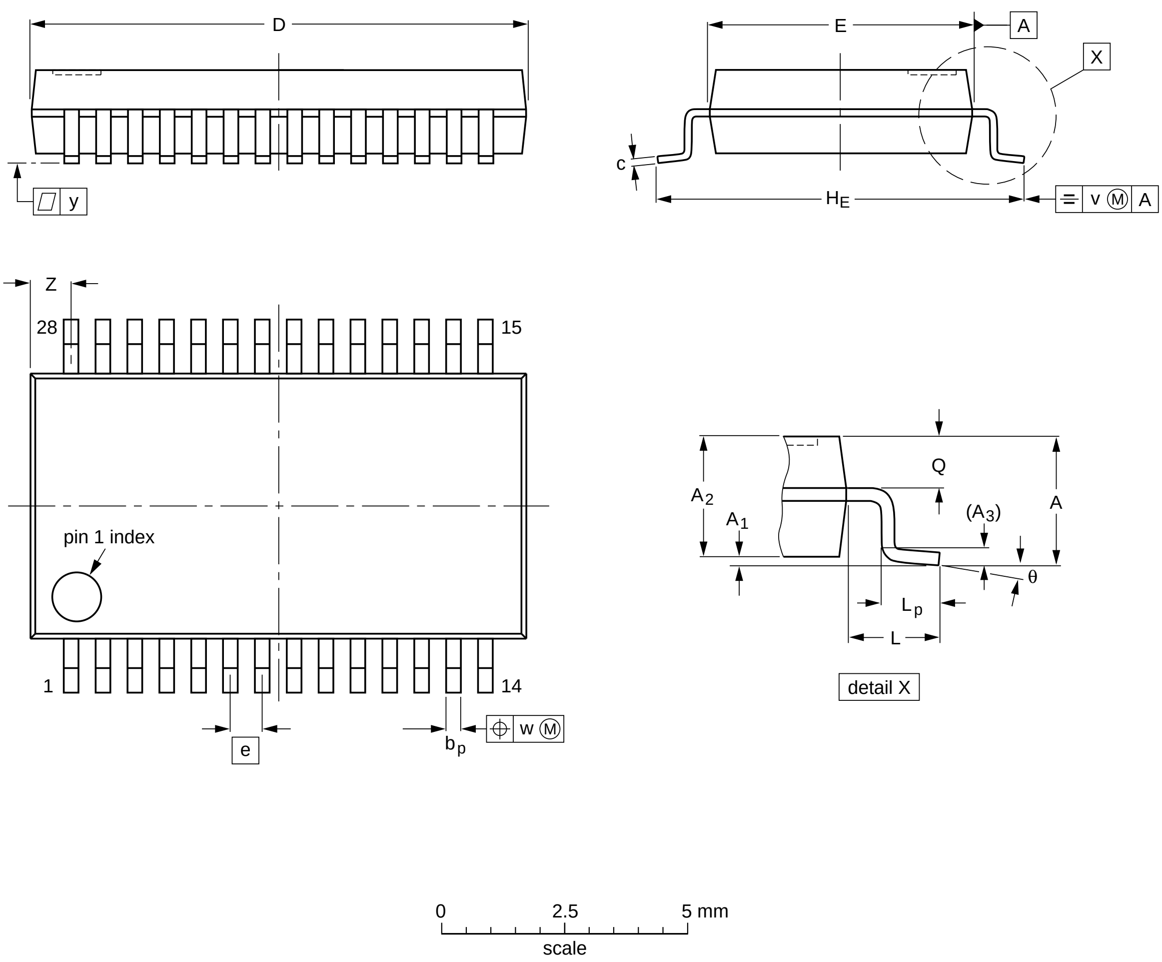
(1) V_{RB}, V_{RM} and V_{RT} are decoupled to AGND.

(2) Pins 15 and 16 should be connected to DGND in order to prevent noise influence.

Fig.14 Application diagram.

PACKAGE OUTLINE

SSOP28: plastic shrink small outline package; 28 leads; body width 5.3 mm **SOT341-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	10.4 10.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.1 0.7	8^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT341-1		MO-150AH				~~93-09-08~~ 95-02-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for SSOP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.**

Even with these conditions, only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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