DATA SHEET

TDA8779
10-bit converter interface (ADC/DAC) for quadrature transceiver

Objective specification
Supersedes data of 1996 Sep 05
File under Integrated Circuits, IC02

1996 Sep 18

Philips Semiconductors

PHILIPS

10-bit converter interface (ADC/DAC) for quadrature transceiver

TDA8779

FEATURES

- Two 10-bit ADCs with multiplexed outputs
- Two 10-bit DACs with multiplexed inputs
- Sampling rate for the ADCs and DACs up to 20 MHz
- Digital outputs (for the ADC) and inputs (for the DAC) are TTL/CMOS compatible (2.7 to 5.5 V)
- Internal reference voltage regulator
- Power dissipation 520 mW
- Standby mode.

APPLICATIONS

Wireless communication.

GENERAL DESCRIPTION

The TDA8779 contains two 10-bit high speed ADCs and two 10-bit DACs for wireless communication (for use in transceiver modules). This device converts two analog input signals (channels I and Q) and digital inputs (D0 to D9) at a maximum sampling rate of 20 MHz. The input bias voltages for the analog input voltages are provided internally at the middle code. The analog input and output voltages are AC coupled.

The data sampling is performed on the rising edge of the clock for ADCs and DACs.

All reference voltages are generated internally.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA1}	analog supply voltage for the ADC part		4.75	5.0	5.5	V
V_{CCD1}	digital supply voltage for the ADC part		4.75	5.0	5.5	V
V_{CCA2}	analog supply voltage for the DAC part		4.75	5.0	5.5	V
V_{CCD2}	digital supply voltage for the DAC part		4.75	5.0	5.5	V
V_{CCO}	output stage supply voltage		2.7	3.0	5.5	V
I_{CCA}	analog supply current		–	71	–	mA
I_{CCD}	digital supply current		–	31	–	mA
I_{CCO}	output stage supply current	ramp input; f_{CLK} = 20 MHz	–	2	–	mA
$f_{CLK(ADC)max}$	maximum clock frequency for the ADC part		20	–	–	MHz
INLA	integral non linearity for the ADC part	full-scale; ramp input; f_{CLK} = 20 MHz	–	±2	–	LSB
DNLA	differential non linearity for the ADC part	50% full-scale; ramp input; f_{CLK} = 20 MHz	–	±0.3	–	LSB
$f_{CLK(DAC)max}$	maximum clock frequency for the DAC part		20	–	–	MHz
INLD	integral non linearity for the DAC part	full-scale; ramp input; f_{CLK} = 20 MHz	–	±2	–	LSB
DNLD	differential non linearity for the DAC part	full-scale; ramp input; f_{CLK} = 20 MHz	–	±0.75	–	LSB
P_{tot}	total power dissipation		–	520	–	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8779H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

BLOCK DIAGRAM

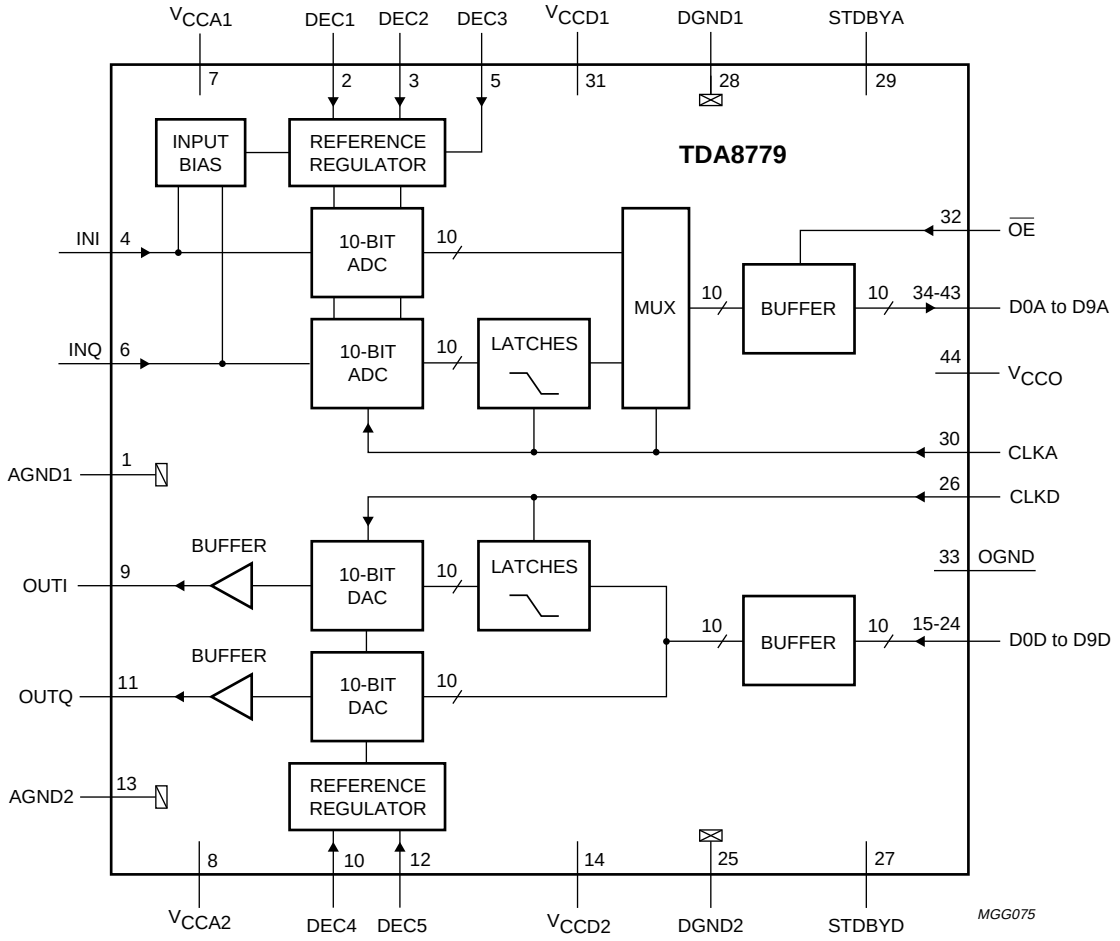


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
AGND1	1	analog ground 1
DEC1	2	decoupling input 1
DEC2	3	decoupling input 2
INI	4	I channel ADC input
DEC3	5	decoupling input 3
INQ	6	Q channel ADC input
V_{CCA1}	7	analog supply voltage 1 for ADC part (+5 V)
V_{CCA2}	8	analog supply voltage 2 for DAC part (+5 V)
OUTI	9	I channel DAC analog output
DEC4	10	decoupling input 4
OUTQ	11	Q channel DAC analog output
DEC5	12	decoupling input 5
AGND2	13	analog ground 2
V_{CCD2}	14	digital supply voltage 2 for DAC part (+5 V)
D0D	15	multiplexed input for the DACs; bit 0
D1D	16	multiplexed input for the DACs; bit 1
D2D	17	multiplexed input for the DACs; bit 2
D3D	18	multiplexed input for the DACs; bit 3
D4D	19	multiplexed input for the DACs; bit 4
D5D	20	multiplexed input for the DACs; bit 5
D6D	21	multiplexed input for the DACs; bit 6
D7D	22	multiplexed input for the DACs; bit 7
D8D	23	multiplexed input for the DACs; bit 8

SYMBOL	PIN	DESCRIPTION
D9D	24	multiplexed input for the DACs; bit 9
DGND2	25	digital ground 2
CLKD	26	transmission block clock
STDBYD	27	power standby for the DAC part (active HIGH)
DGND1	28	digital ground 1
STDBYA	29	power standby for the ADC part (active HIGH)
CLKA	30	reception block clock
V_{CCD1}	31	digital supply voltage 1 for ADC part (+5 V)
$\overline{OE}$	32	ADCs digital output enable (3-state output); (active LOW)
OGND	33	input/output ground
D0A	34	I and Q digital outputs; bit 0
D1A	35	I and Q digital outputs; bit 1
D2A	36	I and Q digital outputs; bit 2
D3A	37	I and Q digital outputs; bit 3
D4A	38	I and Q digital outputs; bit 4
D5A	39	I and Q digital outputs; bit 5
D6A	40	I and Q digital outputs; bit 6
D7A	41	I and Q digital outputs; bit 7
D8A	42	I and Q digital outputs; bit 8
D9A	43	I and Q digital outputs; bit 9
V_{CCO}	44	output supply voltage (2.7 to 5.5 V)

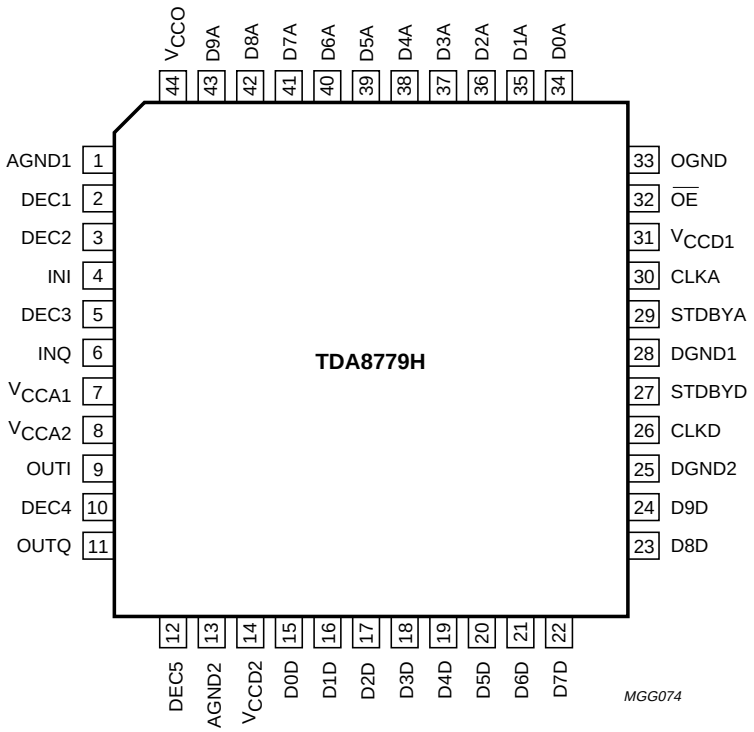


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA1}	analog supply voltage for ADC part		–0.3	+7.0	V
V_{CCA2}	analog supply voltage for DAC part		–0.3	+7.0	V
V_{CCD1}	digital supply voltage for ADC part		–0.3	+7.0	V
V_{CCD2}	digital supply voltage for DAC part		–0.3	+7.0	V
V_{CCO}	output stage supply voltage		–0.3	+7.0	V
ΔV_{CC}	voltage difference between:				
	$V_{CCA} - V_{CCD}$		–1.0	+1.0	V
	$V_{CCA} - V_{CCO}$		–1.0	+4.0	V
	$V_{CCD} - V_{CCO}$		–1.0	+4.0	V
I_o	output current		–	10	mA
V_i	input voltage	referenced to AGND	–0.3	+7.0	V
$V_{clk(p-p)}$	AC input switching voltage (peak-to-peak value)	referenced to DGND	–	V_{CCD}	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–20	+75	°C
T_j	junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	in free air	75	K/W

CHARACTERISTICS

$V_{CCA} = V_7$ and V_8 to V_1 and V_{13} = 4.75 to 5.5 V; $V_{CCD} = V_{31}$ and V_{14} to V_{28} and V_{25} = 4.75 to 5.5 V;
$V_{CCO} = V_{44}$ to V_{33} = 2.7 to 5.5 ; AGND1, AGND2, OGND, DGND1 and DGND2 are shorted together;
T_{amb} = –20 to +70 °C; measured typically at $V_{CCA} = V_{CCD}$ = 5 V and V_{CCO} = 3 V; C_L = 15 pF; T_{amb} = 25°C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA1}	analog supply voltage for ADC part		4.75	5.0	5.5	V
V_{CCD1}	digital supply voltage for ADC part		4.75	5.0	5.5	V
V_{CCA2}	analog supply voltage for DAC part		4.75	5.0	5.5	V
V_{CCD2}	digital supply voltage for DAC part		4.75	5.0	5.5	V
V_{CCO}	output stage supply voltage		2.7	3.0	5.5	V
ΔV_{CC}	voltage difference between					
	$V_{CCA} - V_{CCD}$		–0.2	–	+0.2	V
	$V_{CCA} - V_{CCO}$		–0.2	–	+2.5	V
	$V_{CCD} - V_{CCO}$		–0.2	–	+2.5	V
I_{CCA}	analog supply current		–	71	–	mA
I_{CCD}	digital supply current		–	31	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CCO}	output stage supply current	ramp input; f_{CLK} = 20 MHz	–	2	–	mA
$I_{CCA1(stb)}$	analog standby current for ADC part		–	5	–	mA
$I_{CCA2(stb)}$	analog standby current for DAC part		–	5	–	mA
ADC PART						
CLOCK INPUT						
V_{IL}	LOW level input voltage		0	–	0.6	V
V_{IH}	HIGH level input voltage		2.2	–	V_{CCD1}	V
I_{IL}	LOW level input current		–10	–	+10	μA
I_{IH}	HIGH level input current		–10	–	+10	μA
DIGITAL INPUTS: PINS $\overline{OE}$ AND STDBYA						
V_{IL}	LOW level input voltage		0	–	0.6	V
V_{IH}	HIGH level input voltage		2.2	–	V_{CCD1}	V
I_{IL}	LOW level input current		–1	0	+1	μA
I_{IH}	HIGH level input current		–	–	1	μA
ANALOG INPUTS						
I_{IL}	LOW level input current	for code 0	–	tbf	–	μA
I_{IH}	HIGH level input current	for code 1023	–	tbf	–	μA
$V_{i(p-p)}$	analog input voltage (peak-to-peak value)	full-scale	tbf	1.5	tbf	V
$V_{i(p-p)over}$	maximum analog input over voltage (peak-to-peak value)	overvoltage	–	–	4.5	V
Z_I	input impedance		–	10	–	kΩ
C_I	input capacitance		–	3	–	pF
DIGITAL OUTPUTS: D0A TO D9A						
V_{OL}	LOW level output voltage	I_o = 1 mA	0	–	0.5	V
V_{OH}	HIGH level output voltage	I_o = –1 mA	V_{CCO} – 0.5	–	V_{CCO}	V
I_{oZ}	output current in 3-state mode	0.5 V < V_o < V_{CCO} – 0.5 V	–20	–	+20	μA
SWITCHING CHARACTERISTICS (see Fig.3)						
f_{CLKmax}	maximum clock frequency		20	–	–	MHz
t_{CH}	clock pulse width HIGH		20	–	–	ns
t_{CL}	clock pulse width LOW		20	–	–	ns
t_r	clock rise time		–	4	–	ns
t_f	clock fall time		–	4	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ANALOG SIGNAL PROCESSING						
Linearity						
INLA	integral non linearity	ramp input; f_{CLK} = 20 MHz	–	±2	–	LSB
DNLA	differential non linearity	full-scale; ramp input; f_{CLK} = 20 MHz	–	±0.5	–	LSB
		50% full-scale; ramp input; f_{CLK} = 20 MHz	–	±0.3	–	LSB
Noise floor; note 2						
NF	noise floor	f_{in} = 5.1 MHz; 20 Msps	–	–60	–	dB
Harmonics; note 3						
THD	total harmonic distortion	f_i = 5.1 MHz; 20 Msps	–	–54	–	dB
Spurious free dynamic range						
SFDR	spurious free dynamic range	f_i = 5.1 MHz; 20 Msps	45	56	–	dB
Matching between the I and Q channels						
ΔV	amplitude matching	f_{in} = 5.1 MHz; f_{CLK} = 20 MHz; T_{amb} = 25°C	–	–	6	%
$\Delta\varphi$	phase matching	f_{in} = 5.1 MHz; f_{CLK} = 20 MHz; T_{amb} = 25°C	–	–	2	Deg
Bandwidth						
B	bandwidth maximum attenuation of –0.3 dB	full-scale sine wave; T_{amb} = 25°C;	5.5	–	–	MHz
		50% full-scale sine wave; T_{amb} = 25°C;	tbf	–	–	MHz
TIMING: (THE OUTPUT DATA IS AVAILABLE AFTER THE MAXIMUM DELAY TIME t_d); C_L = 15 pF; see Fig.3						
t_{ds}	sampling delay time		–	–	5	ns
t_h	output hold time		5	–	–	ns
t_d	output delay time	V_{CCO} = 4.75 V	–	12	15	ns
		V_{CCO} = 3.15 V	–	17	20	ns
		V_{CCO} = 2.7 V	–	21	24	ns
3-STATE OUTPUT DELAY TIMES; see Fig.4						
t_{dZH}	output delay enable HIGH		–	14	18	ns
t_{dZL}	output delay enable LOW		–	16	20	ns
t_{dHZ}	output delay disable HIGH		–	16	20	ns
t_{dLZ}	output delay disable LOW		–	14	18	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
STANDBY MODE OUTPUT DELAY TIMES; STDBYA						
$t_{d(stb)LH}$	standby (LOW-to-HIGH transition)		–	–	100	µs
$t_{d(stb)HL}$	start-up (HIGH-to-LOW transition)		–	–	100	µs
CROSSTALK ON THE ADC						
α_{ct}	crosstalk into the ADC	$f_{CLK(DAC)}$ = 16.384 MHz; $f_{CLK(ADC)}$ = 8.192 MHz; T_{amb} = 25°C; both DACs switching between input codes 0 and 1023; one ADC 1 V (p-p) sine wave at 4 MHz and the other ADC set at the middle code	–	–	–55	dB
DAC PART						
DIGITAL INPUTS: D0D TO D9D AND CLKD						
V_{IL}	LOW level input voltage		0	–	0.6	V
V_{IH}	HIGH level input voltage		2.2	–	V_{CCD2}	V
I_{IL}	LOW level input current		–200	–120	0	µA
I_{IH}	HIGH level input current		–10	–	+10	µA
DIGITAL INPUT; STDBYD						
V_{IL}	LOW level input voltage		0	–	0.6	V
V_{IH}	HIGH level input voltage		2.2	–	V_{CCD2}	V
I_{IL}	LOW level input current		–1	0	+1	µA
I_{IH}	HIGH level input current		–	–	1	µA
TIMING: see Fig.5						
$f_{CLK(max)}$	maximum clock frequency		20	–	–	MHz
t_{CH}	clock pulse width HIGH		20	–	–	ns
t_{CL}	clock pulse width LOW		20	–	–	ns
t_r	clock rise time		–	4	–	ns
t_f	clock fall time		–	4	–	ns
t_s	input data set-up time		10	tbf	–	ns
t_h	input data hold time		0	tbf	–	ns
ANALOG OUTPUTS; note 1						
$V_{o(p-p)}$	output voltage (peak-to-peak value)	full-scale	tbf	1	tbf	V
Z_{oL}	output load impedance	see Fig.6	–	15	–	pF
			–	0.3	–	kΩ
TRANSFER FUNCTION						
INLD	integral non linearity	ramp input; f_{CLK} = 20 MHz	–	±3	–	LSB
DNLD	differential non linearity	ramp input; f_{CLK} = 20 MHz;	–	±0.75	–	LSB
B	maximum bandwidth	full scale; T_{amb} = 25°C	5.5	–	–	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Matching between channel I and Q						
ΔV	amplitude matching	f_o = 5.1 MHz; f_{CLK} = 20 MHz; T_{amb} = 25°C	–	–	6	%
$\Delta\varphi$	phase matching	f_o = 5.1 MHz; f_{CLK} = 20 MHz; T_{amb} = 25°C	–	–	2	Deg
DYNAMIC RANGE; note 2						
NF	noise floor	f_o = 5.1 MHz; f_{CLK} = 20 MHz	–	–60	–	dB
SPURIOUS FREE DYNAMIC RANGE						
SFDR	spurious free dynamic range	f_o = 5.1 MHz; f_{CLK} = 20 MHz	–	50	–	dB
STANDBY MODE OUTPUT DELAY; STDBYD						
$t_{d(stb)LH}$	standby (LOW-to-HIGH transition)		–	–	100	µs
$t_{d(stb)HL}$	start-up (HIGH-to-LOW transition)		–	–	100	µs
CROSSTALK ON THE DAC						
α_{ct}	crosstalk into the DAC	$f_{CLK(DAC)}$ = 16.384 MHz; $f_{CLK(ADC)}$ = 8.192 MHz; T_{amb} = 25°C; one DAC switching between input codes 0 and 1023 the other DAC set at the middle code; both ADCs 1 V (p-p) sine wave at 4 MHz; incoherent	–	–	–55	dB

Notes

1. It is recommended that the DAC output voltage is AC coupled in order to achieve optimum performance.
2. The noise floor is the maximum value of the output spectrum without taking into account fundamental and harmonics of the input signal.
3. Harmonics are obtained via a Fast Fourier Transformer (FFT) treatment taking 8K acquisition points per period.

Table 1 Output coding and input voltage (typical value, referenced to AGND)

STEP	$V_i - V_{512}$ (V)	BINARY OUTPUT BITS									
		D9A	D8A	D7A	D6A	D5A	D4A	D3A	D2A	D1A	D0A
underflow	<–0.75	0	0	0	0	0	0	0	0	0	0
0	–0.75	0	0	0	0	0	0	0	0	0	0
...	...	...	...	...	...	...	...	...	...	...	...
512	0	1	0	0	0	0	0	0	0	0	0
...	...	...	...	...	...	...	...	...	...	...	...
1023	0.75	1	1	1	1	1	1	1	1	1	0
overflow	>0.75	1	1	1	1	1	1	1	1	1	1

Table 2 Input coding and output voltage (typical value, referenced to DGND)

STEP	BINARY INPUT BITS										$V_o - V_{512}$ (V)
	D9D	D8D	D7D	D6D	D5D	D4D	D3D	D2D	D1D	D0D	
0	0	0	0	0	0	0	0	0	0	0	–0.5
...	...	...	...	...	...	...	...	...	...	...	...
512	1	0	0	0	0	0	0	0	0	0	0
...	...	...	...	...	...	...	...	...	...	...	...
1023	1	1	1	1	1	1	1	1	1	0	0.5

Table 3 Mode selection

$\overline{OE}$	D0A TO D9A
1	high impedance
0	active; binary

Table 4 Standby selection

STDBYA	D0 TO D9	$I_{CCA} + I_{CCD}$ (typ.)
1	–	5 mA
0	active	64 mA

Table 5 Standby selection

STDBYD	OUTI AND OUTQ	$I_{CCA} + I_{CCD}$ (typ.)
1	–	5 mA
0	active	38 mA

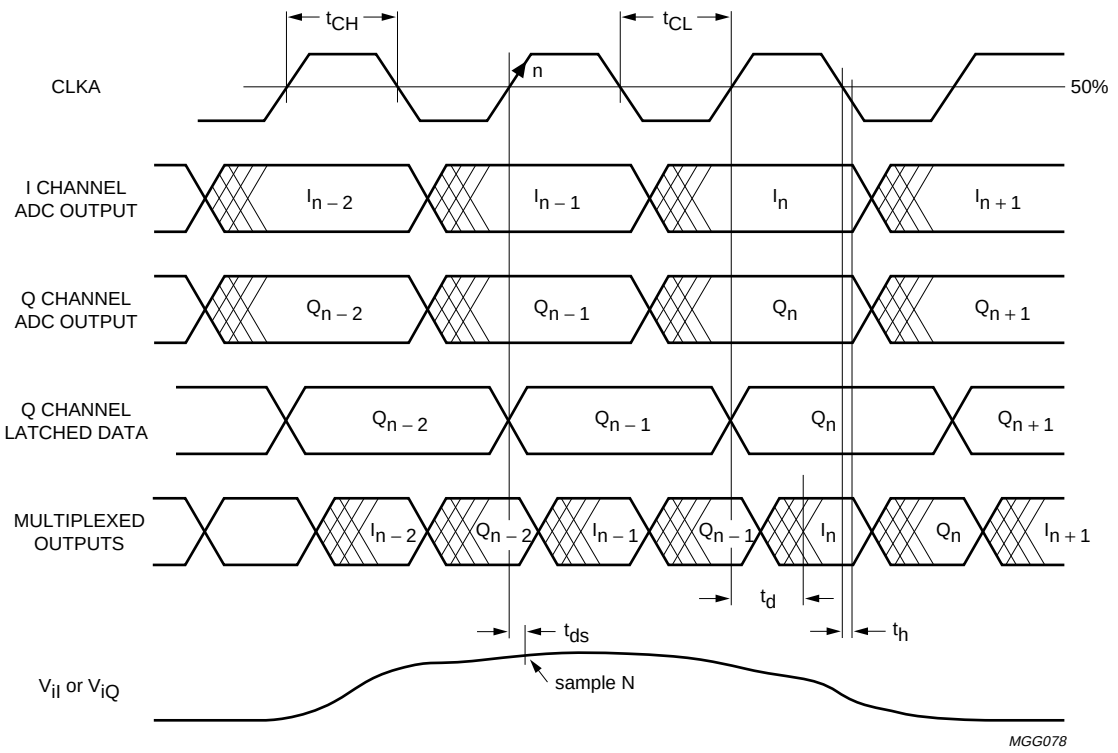
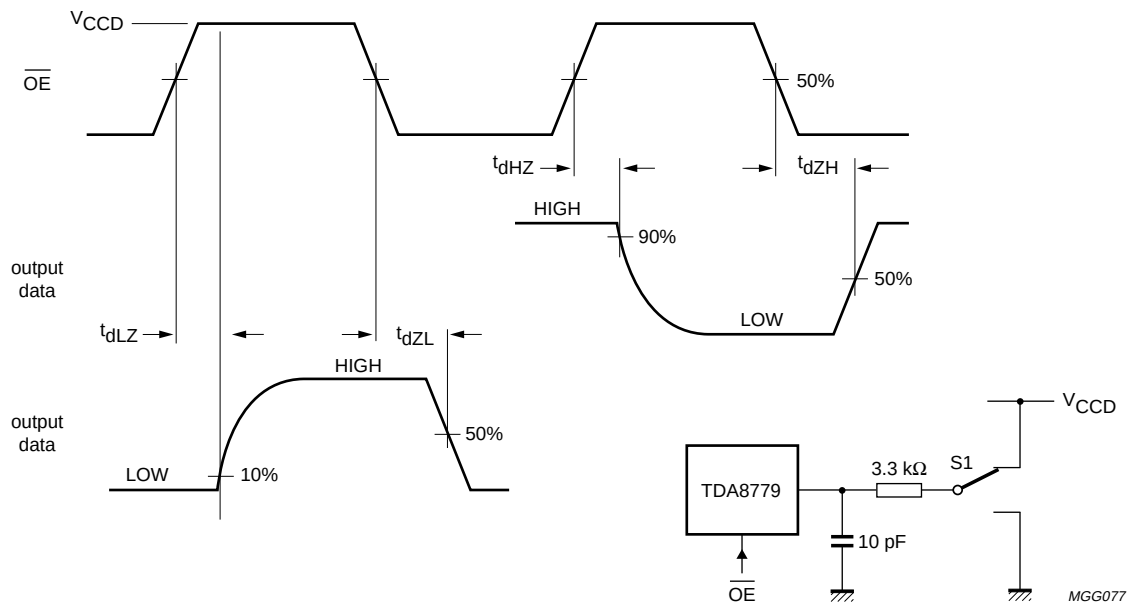


Fig.3 Timing diagram for the ADC.



$t_{\overline{OE}}$ = 100 kHz.

Fig.4 Timing diagram and test conditions of 3-state output delay time.

Table 6 Test conditions for Fig.4

TEST	SWITCH S1
t_{dLZ}	V_{CCD}
t_{dZL}	V_{CCD}
t_{dHZ}	DGND
t_{dZH}	DGND

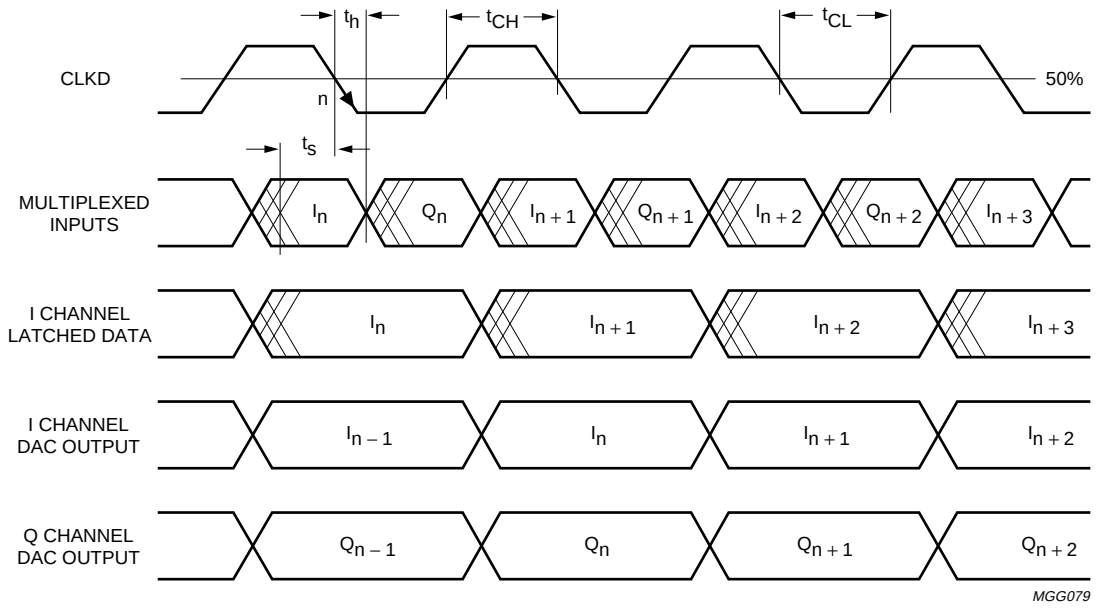


Fig.5 DACs multiplexed inputs timing diagram.

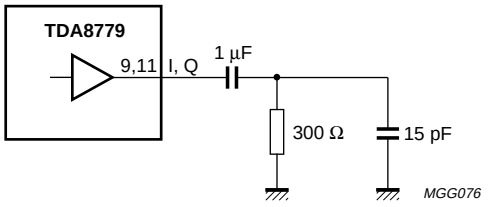


Fig.6 Equivalent DACs output load.

APPLICATION INFORMATION

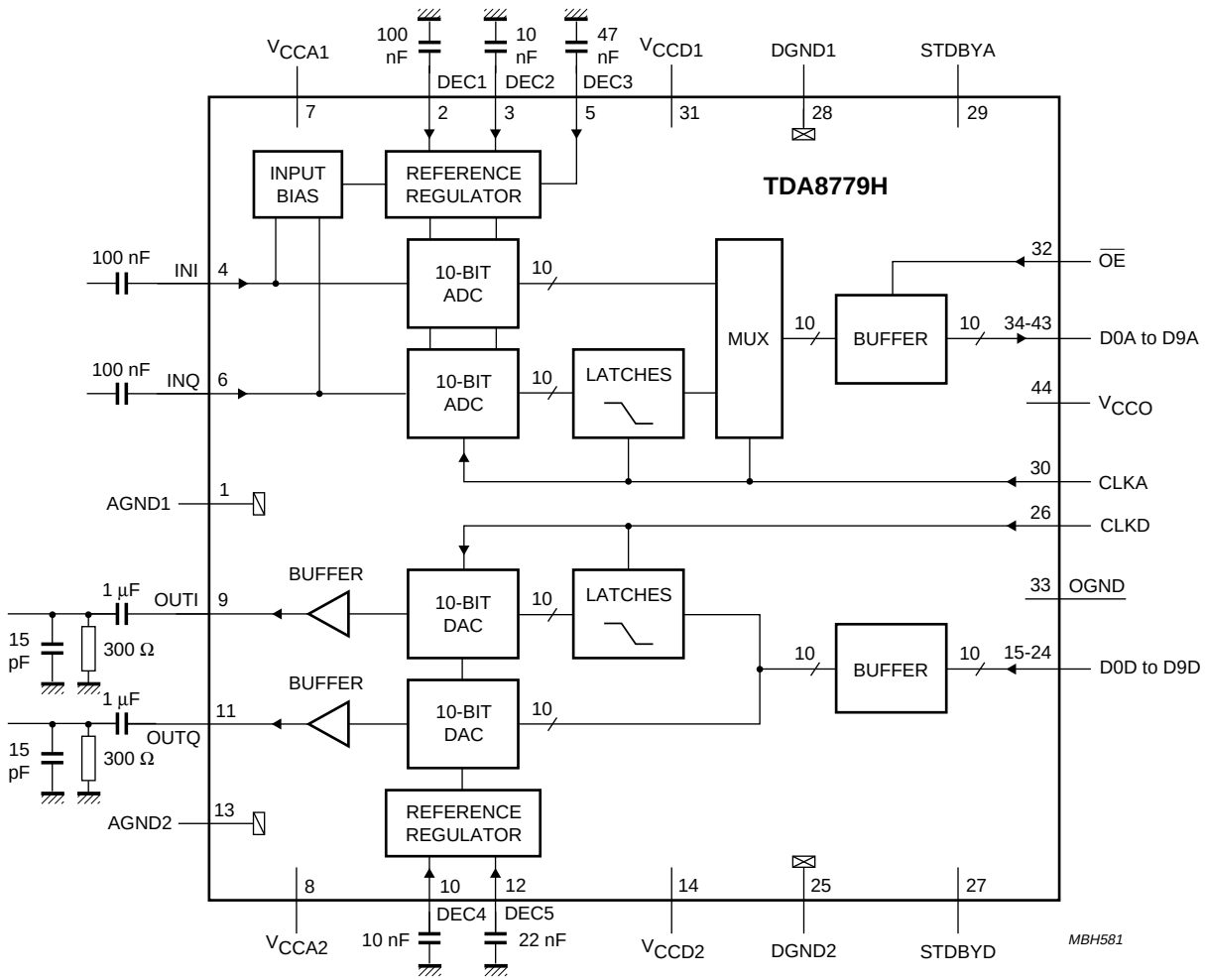
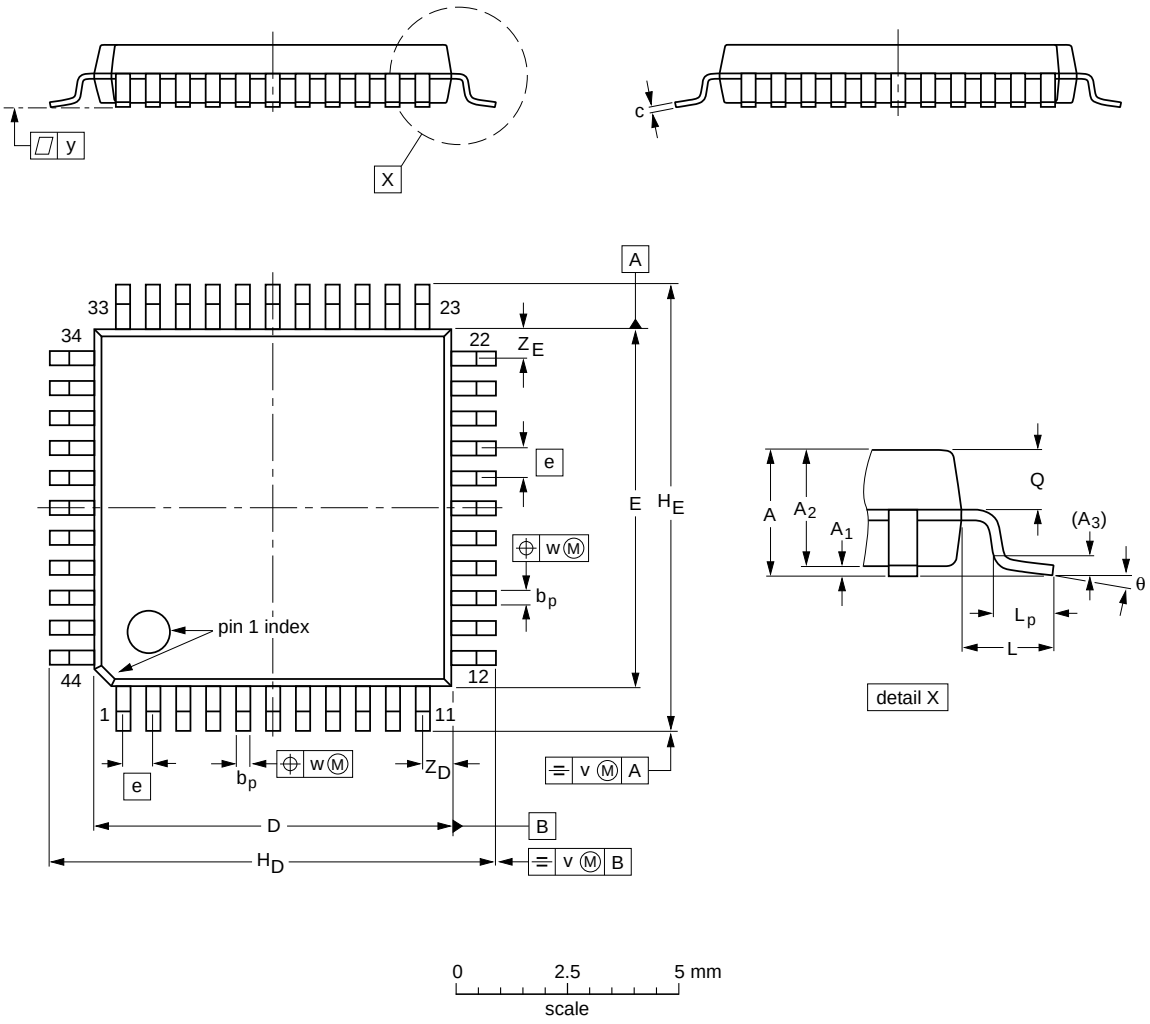


Fig.7 Application diagram.

PACKAGE OUTLINE

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm **SOT307-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.85 0.75	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						~~92-11-17~~ 95-02-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.