True logarithmic amplifier TDA8780M

FEATURES

- 72 dB true logarithmic dynamic range
- Small-signal gain-adjustment facility
- Constant limiting output voltage
- Temperature and DC power supply voltage independent
- Easy interfacing to analog-to-digital converters
- Output DC level shift facility.

APPLICATIONS

- Dynamic range compression
- IF signal dynamic range reduction in digital receivers
- Compression receivers.

GENERAL DESCRIPTION

The TDA8780M is a true logarithmic amplifier intended for dynamic range reduction of IF signals at 10.7 MHz in digital radio receivers. It offers true logarithmic characteristics over a 72 dB input dynamic range, has a small-signal gain-adjustment facility and a constant limiting output voltage for large input levels.

A unique feature is the smooth “changeover” from linear operation (inputs less than 60 μV) to logarithmic mode.

The device is manufactured in an advanced BiCMOS process which enables high performance being obtained with low DC power supply consumption. The true logarithmic amplifier can be driven by single-ended or differential inputs. The DC operating point is set by overall on-chip feedback decoupled by two off-chip capacitors, which define the low-frequency cut-off point.

The performance of the amplifier is stabilized against temperature and DC power supply variations. The differential output is converted internally to a single-ended output by an on-chip operational amplifier arrangement in which the DC output level is set by an externally-supplied reference voltage. A power-down facility allows the circuit to be disabled from a control input.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	4.5	5.0	5.5	V
I_P	supply current	–	–	6.7	mA
$I_{P(PD)}$	supply current in power-down mode	–	–	250	μA
f_{in}	operating input frequency	–	–	15	MHz
$V_{in(M)}$	dynamic logarithmic input voltage (peak value)	0.06	–	300	mV
T_{amb}	operating ambient temperature	–20	–	+75	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8780M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

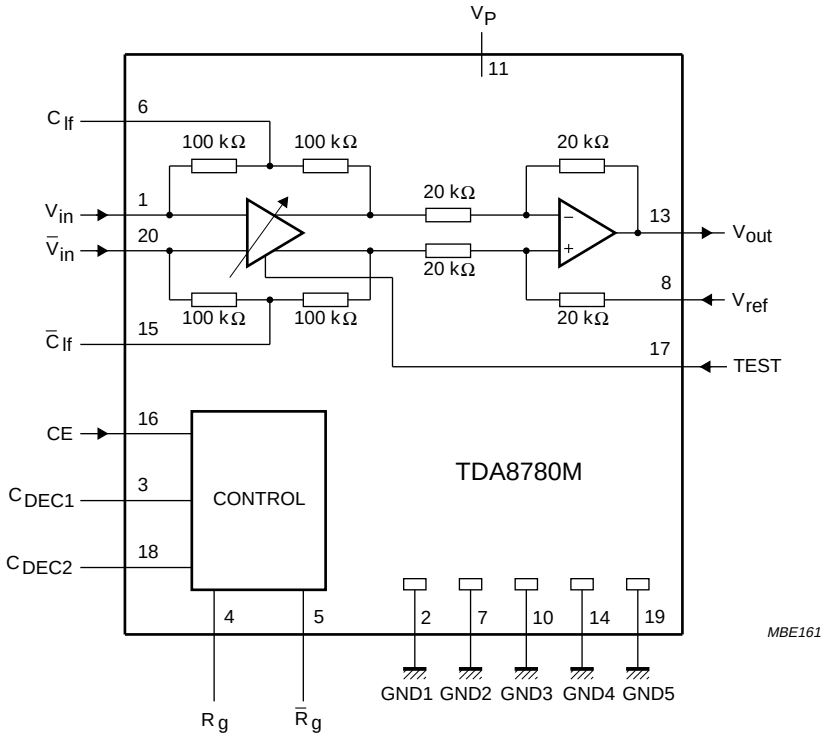


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{in}	1	signal voltage input
GND1	2	ground 1
C_{DEC1}	3	control circuit first decoupling and optional start-up capacitor connection
R_g	4	small-signal gain-setting resistor
$\overline{R}_g$	5	small-signal complementary gain-setting resistor
C_{lf}	6	low-frequency cut-off point setting capacitor
GND2	7	ground 2
V_{ref}	8	external reference voltage input
n.c.	9	not connected
GND3	10	ground 3 (main ground)
V_P	11	power supply
n.c.	12	not connected
V_{out}	13	true logarithmic voltage output
GND4	14	ground 4
$\overline{C}_{lf}$	15	complementary low-frequency cut-off point setting capacitor
CE	16	TTL-level-compatible circuit enable input (active HIGH)
TEST	17	test input; connected to ground in normal operation
C_{DEC2}	18	control circuit second decoupling and optional start-up capacitor
GND5	19	ground 5
$\overline{V}_{in}$	20	complementary signal voltage input

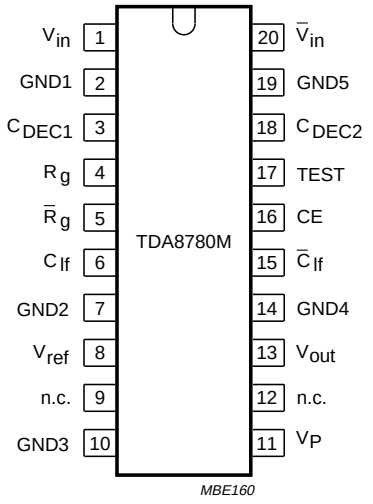


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

A true logarithmic amplifier can be realized from a cascade of similar stages each stage consisting of a pair of amplifiers whose inputs and outputs are connected in parallel. One of these amplifiers can be formed by an undegenerated long-tailed pair which provides high gain but limited linear input signal-handling capability. The other amplifier can be formed by a degenerated long-tailed pair which provides a gain of unity and a much larger linear input signal-handling capability.

The overall cascade amplifies very small input signals but, once these reach the level at which the undegenerated long-tailed pair in the last stage is at the limit of its linear signal-handling capability, the output voltage becomes logarithmically dependent on the input signal level. This behaviour continues until the input signal reaches the level at which undegenerated long-tailed pair in the first stage is at the limit of its linear input signal-handling capability. The transfer characteristic beyond this point then depends on the exact configuration of the degenerated long-tailed pair in the first stage.

Five stages are used in the TDA8780M to provide a 72 dB true logarithmic dynamic range. The DC bias current in the undegenerated long-tailed pair in the first stage is made externally adjustable, using an off-chip resistor, to provide a small-signal gain adjustment facility. The small signal gain defined by this resistor is valid when the IC is operating in the “linear” mode, for input signals typically less than 60 μV.

A high-level limiter is inserted between the first and second stages to provide a constant limiting output voltage which is essentially independent of the value of the gain setting resistor. These stages can be driven by single-ended or differential inputs. The DC operating point is set by overall on-chip feedback decoupled by two off-chip capacitors which define the low-frequency cut-off point. The performance is stabilized against temperature and DC power supply variations. The input to the true logarithmic amplifier is protected against damage due to excessive differential input signals by diodes.

The differential output from the true logarithmic amplifier is converted internally to a single-ended output by an on-chip operational amplifier arrangement in which the DC output level is set by an externally-supplied reference voltage. The output is capable of driving loads down to 10 kΩ. The limiting output voltage and the output drive capability have been chosen to facilitate interfacing to analog-to-digital converters. A major part of the DC power supply current consumption of the device is associated with provision of this output drive capability. The DC power supply consumption is significantly less when the device is driving smaller loads.

A power-down facility allows the circuit to be disabled from a TTL-level compatible control input.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage	–0.3	+6.0	V
V_i	input voltage all other pins referenced to ground	–0.3	V_P + 0.3	V
T_{amb}	operating ambient temperature	–20	+75	°C
T_{stg}	IC storage temperature	–55	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

ESD in accordance with *"MIL STD 883C" - "Method 3015"*.

CHARACTERISTICS

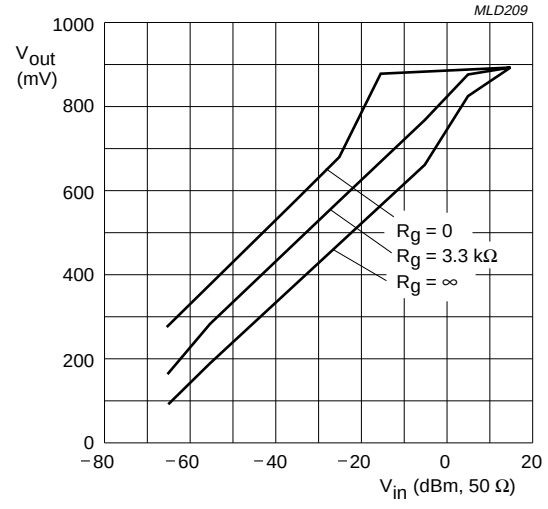
V_P = 5 V; T_{amb} = 25 °C; V_{ref} = 2.5 V; V_{in} at f_{in} = 10.7 MHz; R_g = 3.3 kΩ; output not loaded; unless otherwise specified. Signal values expressed as peak voltages mV (peak), μV (peak) or dBm (50 Ω).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		4.5	5.0	5.5	V
I_P	supply current	V_P = 5.5 V; V_{in} = 1 V	–	5.4	6.7	mA
		V_P = 5.0 V; V_{in} = 1 V	–	4.9	6.2	mA
$I_{P(PD)}$	supply current in power-down	output not loaded	–	40	200	μA
		R_L = 10 kΩ	–	100	250	μA
t_{sw}	switching time	see Fig.6	–	70	–	μs
Reference input (pin 8)						
V_{ref}	external reference voltage input		2.0	2.5	V_P – 2.0	V
R_{ref}	external reference resistance input		–	40	–	kΩ
Inputs (pins 1 and 20)						
f_{in}	input operating frequency	note 1	1.0	10.7	15	MHz
R_{diff}	differential small-signal input resistance	V_{in} = 10 mV	–	10	–	kΩ
C_{diff}	differential input capacitance		–	2	–	pF
$V_{in(min)}$	input voltage level at start of logarithmic characteristic		–	60	–	μV
$V_{in(top)}$	input voltage level at top end of logarithmic characteristic		–	300	–	mV
$V_{in(max)}$	maximum input signal voltage	input protection diodes not conducting	–	1	–	V
ΔV_{in}	input voltage level spread across logarithmic range	over whole T_{amb} and V_P range	–	±2.5	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output (pin 13)						
V_{os}	DC offset voltage (V_{out} to V_{ref})	no input signal	–60	+40	+140	mV
V_{out}	output voltage level across logarithmic range	V_{in} = 60 μV (–71.4 dBm)	45	80	115	mV
		V_{in} = 400 μV (–54.9 dBm)	200	245	290	mV
		V_{in} = 3 mV (–37.4 dBm)	365	440	495	mV
		V_{in} = 25 mV (–19.0 dBm)	530	610	690	mV
		V_{in} = 200 mV (–1.0 dBm)	680	780	880	mV
		V_{in} = 300 mV (+2.6 dBm)	710	820	930	mV
		R_g = 0; V_{in} = 3 mV; see Fig.3	–	530	–	mV
		R_g = ∞; V_{in} = 3 mV; see Fig.3	–	360	–	mV
$V_{out(lim)}$	limiting output voltage	V_{in} = 1 V (+13.0 dBm)	750	950	1050	mV
$\Delta\varphi$	spread in output phase transfer characteristic across logarithmic range		–	15	–	
f_{lf}	low frequency cut-off point (3 dB)	see Fig.6	–	–	0.1	MHz
G_{flat}	gain flatness at 1 to 15 MHz	V_{in} = 10 mV	–	0.5	1.5	dB
R_{13}	output resistance		–	150	–	Ω
Logic input (pin 16)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2	–	V_P	V
I_{LI}	input leakage current	V_{IL} = 0 to V_P	–1	–	+1	μA

Note

1. With some changes in application the lower input frequency limit can be lowered.



V_{CC} = 5 V; V_{ref} = 2.5 V; f_{in} = 10 MHz; T_{amb} = 25 °C.

Fig.3 Output voltage dependence on R_g.

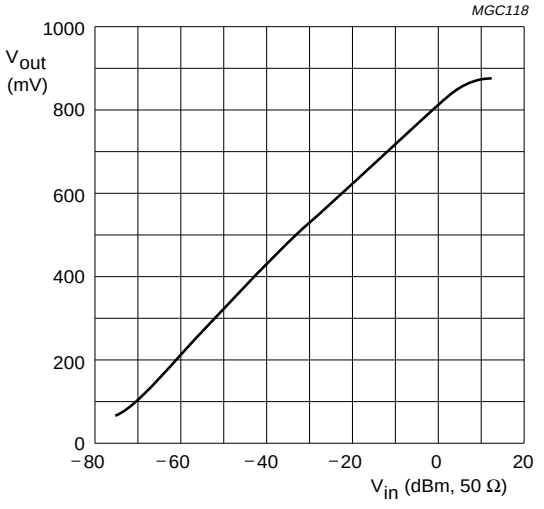


Fig.4 Typical transfer characteristics.

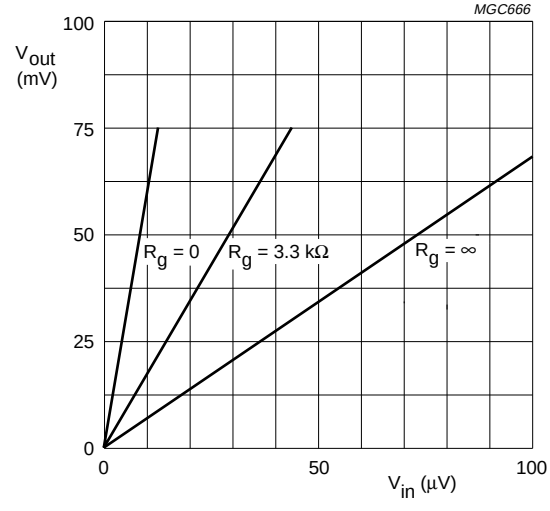


Fig.5 Typical small signal gain.

APPLICATION INFORMATION

The circuit is typically connected as shown in Fig.6. The single-ended 10.7 MHz input IF signal is applied (arbitrarily) to one of the two input pins via a ceramic filter. These inputs should not be DC coupled as this will disable the on-chip feedback which sets the DC operating point of the true logarithmic amplifier. The relatively high impedance of these inputs facilitates correct termination of the ceramic filter by an off-chip resistor.

The low-frequency cut-off point is determined by the value of capacitors connected to pins 6 and 15 which decouple the overall DC feedback and the value of the input coupling capacitors. The output is coupled to an analog-to-digital converter thus the value of the voltage fed to the reference voltage input is not critical. It could be useful in other applications, where the output may be DC coupled to an alternative analog-to-digital converter, to derive this reference voltage from the centre of the input resistor chain of the analog-to-digital converter.

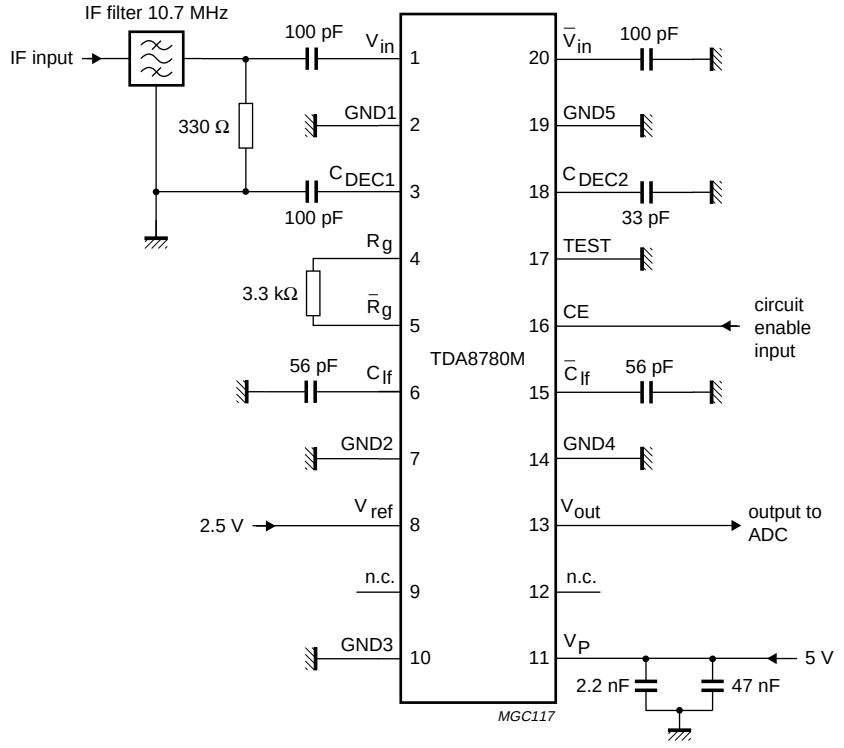


Fig.6 Typical application diagram.