DATA SHEET

TDA8798

Dual 8-bit, 80 Msps A/D converter with DPGA

Objective specification

File under Integrated Circuits, IC02

1998 Apr 15

Philips
Semiconductors

PHILIPS

Dual 8-bit, 80 Msps A/D converter with DPGA

TDA8798

FEATURES

- Dual 8 bit ADC
- Sampling rate up to 80 Msps
- 34 dB dual 6-bit DPGA
- External equalization filter and capacitive coupling between DPGA and ADC possible
- Serial interface for DPGA control featuring a parallel load mode and a counting mode
- TTL/CMOS compatible I/O
- Differential or single-ended TTL/CMOS clock interface
- AC or DC coupling for DPGA inputs.

APPLICATIONS

- High-dynamic range acquisition front-ends
- Digital data storage read channels.

GENERAL DESCRIPTION

The TDA8798 is a dual 8-bit Analog-to-Digital Converter (ADC) including a Digitally controlled Programmable Gain Amplifier (DPGA). The combination of the 80 Msps maximum sampling rate and the 34 dB DPGA gain range, optimizes the component for high dynamic range applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		3.15	3.3	3.45	V
V_{DDD}	digital supply voltage		3.0	3.3	3.6	V
V_{DDO}	output stages supply voltage		3.0	3.3	3.6	V
I_{DDA}	analog supply current		–	106	–	mA
I_{DDD}	digital supply current		–	30	–	mA
I_{DDO}	output stage supply current		–	3	–	mA
INL	integral non linearity	from IC analog input to digital output, including DPGA; ramp input; f_{CLK} = 80 MHz; DVGA gain = G_{min}	–	± 3.0	tbf	LSB
DNL	differential non linearity	from IC analog input to digital output, including DPGA; ramp input; f_{CLK} = 80 MHz; minimum DVGA gain	–	± 0.75	tbf	LSB
$V_{N(rms)}$	output referred noise (RMS value)	Z_i = 50 Ω; BN = 15 MHz; maximum gain	–	tbf	2	mV
B_{-3dB}	DPGA −3 dB bandwidth		30	tbf	–	MHz
f_{CLK}	maximum conversion rate		80	–	–	Msps
P_{tot}	total power consumption		–	460	500	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8798HL	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

Dual 8-bit, 80 Msps A/D converter with
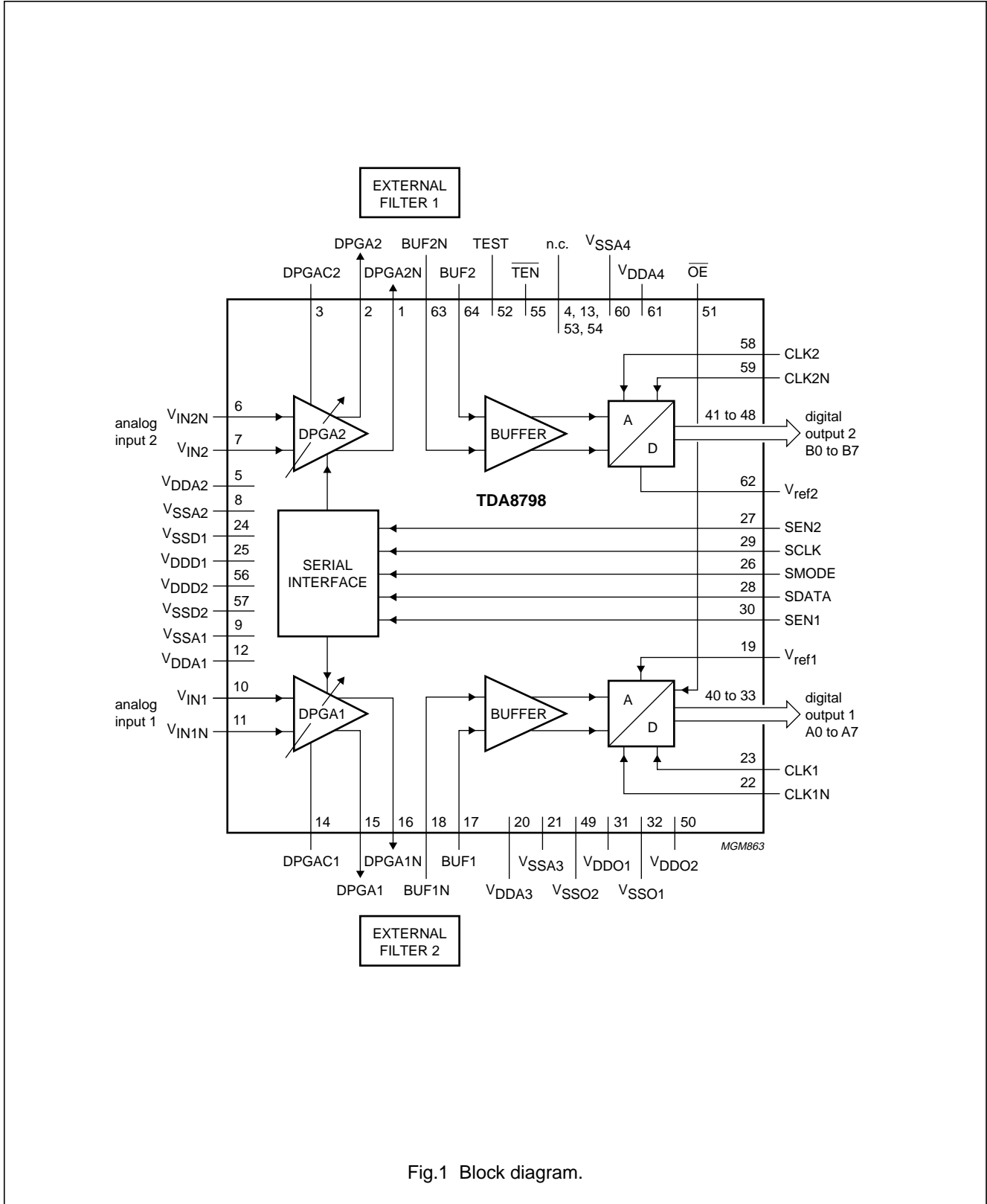DPGA

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BLOCK DIAGRAM

Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
DPGA2N	1	DPGA2 inverting output
DPGA2	2	DPGA2 non-inverting output
DPGAC2	3	bandwidth limitation DPGA2 gain control
n.c	4	not connected
V_{DDA2}	5	DPGA2 analog supply voltage 2
V_{IN2N}	6	DPGA2 inverting input voltage
V_{IN2}	7	DPGA2 non-inverting input voltage
V_{SSA2}	8	DPGA2 analog ground 2
V_{SSA1}	9	DPGA1 analog ground 1
V_{IN1}	10	DPGA1 non-inverting input voltage
V_{IN1N}	11	DPGA1 inverting input voltage
V_{DDA1}	12	DPGA1 analog supply voltage 1
n.c	13	not connected
DPGAC1	14	bandwidth limitation DPGA1 gain control
DPGA1	15	DPGA1 non-inverting output
DPGA1N	16	DPGA1 inverting output
BUF1	17	buffer1 non-inverting input
BUF1N	18	buffer1 inverting input
V_{ref1}	19	ADC1 reference voltage
V_{DDA3}	20	ADC1 analog supply voltage 3
V_{SSA3}	21	ADC1 analog ground 3
CLK1N	22	ADC1 inverting clock input
CLK1	23	ADC1 non-inverting clock input
V_{SSD1}	24	digital ground 1
V_{DDD1}	25	digital supply voltage 1
SMODE	26	serial interface mode input
SEN2	27	serial interface 2 enable not
SDATA	28	serial interface data input
SCLK	29	serial interface clock input
SEN1	30	serial interface 1 enable not
V_{DDO1}	31	digital output supply voltage 1
V_{SSO1}	32	digital output ground 1
A7	33	channel 1 output bit 7 (MSB)
A6	34	channel 1 output bit 6
A5	35	channel 1 output bit 5
A4	36	channel 1 output bit 4
A3	37	channel 1 output bit 3
A2	38	channel 1 output bit 2
A1	39	channel 1 output bit 1
A0	40	channel 1 output bit 0 (LSB)

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SYMBOL	PIN	DESCRIPTION
B0	41	channel 2 output bit 0 (LSB)
B1	42	channel 2 output bit 1
B2	43	channel 2 output bit 2
B3	44	channel 2 output bit 3
B4	45	channel 2 output bit 4
B5	46	channel 2 output bit 5
B6	47	channel 2 output bit 6
B7	48	channel 2 output bit 7 (MSB)
V_{SSO2}	49	digital output ground 2
V_{DDO2}	50	digital output supply voltage 2
$\overline{OE}$	51	output enable not (active LOW)
TEST	52	test (connected to ground)
n.c	53	non connected
n.c	54	non connected
$\overline{TEN}$	55	track-and-hold enable (active LOW)
V_{DDD2}	56	digital supply voltage 2
V_{SSD2}	57	digital ground 2
CLK2	58	ADC2 non-inverting clock input
CLK2N	59	ADC2 inverting clock input
V_{SSA4}	60	ADC2 analog ground 4
V_{DDA4}	61	ADC2 analog supply voltage 4
V_{ref2}	62	ADC2 input reference voltage 2
BUF2N	63	DPGA2 inverting input
BUF2	64	DPGA2 non-inverting input

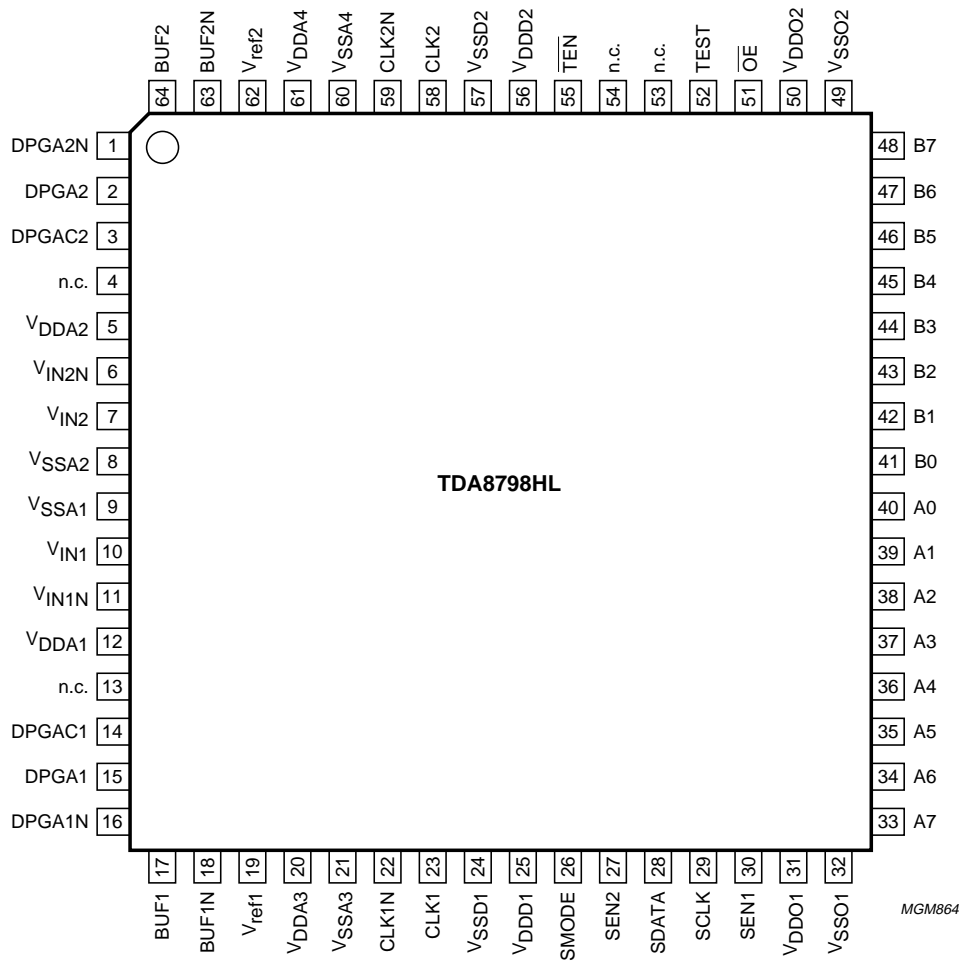Dual 8-bit, 80 Msps A/D converter with DPGA

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Fig.2 Pin configuration.

Dual 8-bit, 80 Msps A/D converter with DPGA

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FUNCTIONAL DESCRIPTION

The TDA8798 comprises of two independent fully differential acquisition chains. Each acquisition chain contains a Digitally controlled Programmable Gain Amplifier (DPGA) and a high-speed Analog-to-Digital Converter (ADC). The gain of the two DPGAs can be controlled independently by means of a serial interface (SI). Further the TDA8798 allows to connect an external filter with AC coupling between the DPGA and ADC in order to provide improved signal conditioning.

Digitally controlled Programmable Gain Amplifier (DPGA)

The fully differential DPGA can be programmed between 0 dB and 34 dB gain in 63 equidistant gain steps. The 6-bit gain setting is controlled by the serial interface. The signal bandwidth of the DPGA exceeds 30 MHz for all gain settings. The bandwidth of the gain control can be adapted using an external decoupling capacitor connected to the pins DPGAC1 and/or DPGAC2 for both DPGAs.
The analog input signals can be provided by means of AC or DC coupling.

Analog-to-Digital Converter (ADC)

The 8-bit ADC converts the differential analog input signal into a binary output format at a maximum conversion rate of 80 Msps. All digital input and output signals are TTL/CMOS compatible. The full-scale input-range of the ADC can be controlled by means of the regulator inputs V_{ref1} and V_{ref2}. The clock interface can be driven either differentially or single-ended. In the latter case, the non-used pin will be decoupled externally. The analog input of the ADC will be provided by means of an AC coupling.

Serial Interface (SI)

Using the SI the gain of the two DPGAS can be controlled independently. The timing diagram given in Fig.3 illustrates the implementation of the VGA gain control function. In this diagram, the SMODE line sets the chip into either the parallel load mode or the count up/count down mode.

Parallel load mode

When performing a parallel load, the operation is a simple shift register function. Note however, that the output of the gain control register does not change during the shifting operation but only after the load is complete and the SEN line goes inactive.

Count-up/count-down mode

The count-up/count-down operation is performed when the MODE line is in the opposite state to that above. In this mode, SEN selects the track to be operated on and the SDATA signal determines the count direction (up or down). SCLK causes the action to occur. It should be noted that the gain control register output is allowed to change as soon as SCLK goes active. In normal operation, gain changes during tracking will be asynchronous and intermittent.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage		−0.3	+7.0	V
V_{DDD}	digital supply voltage		−0.3	+7.0	V
V_{DDO}	output stages supply voltage		−0.3	+7.0	V
ΔV_{DDD}	supply voltage differences between				
	V_{DDA} and V_{DDD}		−1.0	+1.0	V
	V_{DDO} and V_{DDD}		−1.0	+1.0	V
	V_{DDA} and V_{DDO}		−1.0	+1.0	V
$V_{VIN1,2}$	input voltage range pins 10 and 7	referenced to V_{SSA}	−0.3	+7.0	V
I_O	output current		−	+10	mA
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		0	70	°C
T_j	junction temperature		−	104	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\,j-a}$	thermal resistance from junction to ambient in free air	68	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

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CHARACTERISTICS

$V_{DDA} = V_5$ (or V_{12} or V_{20} or V_{61}) to V_8 (or V_9 or V_{21} or V_{60}) = 3.15 to 3.45 V; $V_{DDD} = V_{25}$ (or V_{56}) to V_{24} (or V_{57}) = 3.0 to 3.6 V; $V_{DDO} = V_{31}$ (or V_{50}) to V_{32} (or V_{49}) = 3.0 to 3.6 V; V_{SSA}, V_{SSD} and V_{SSO} shorted together; V_{DDA} to V_{DDD} = −0.25 to 0.25 V; V_{DDD} to V_{DDO} = −0.25 to 0.25 V; V_{DDA} to V_{DDO} = −0.25 to +0.25 V; T_{amb} = 0 to 70 °C; typical values measured at $V_{DDA} = V_{DDD} = V_{DDO}$ = 3.3 V and T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDA}	analog supply voltage		3.15	3.3	3.45	V
V_{DDD}	digital supply voltage		3.0	3.3	3.6	V
V_{DDO}	output stages supply voltage		3.0	3.3	3.6	V
I_{DDA}	analog supply current		–	106	–	mA
I_{DDD}	digital supply current		–	30	–	mA
I_{DDO}	output stage supply current	f_s = 80 Msps; ramp input	–	3	–	mA
Digital programmable gain amplifiers						
ANALOG INPUTS: PINS VIN1, VIN1N, VIN2 AND VIN2N						
$V_{i(max)(p-p)}$	maximum input voltage (peak-to-peak value)	at minimum gain	–	0.5	–	V
		at maximum gain	–	10	–	mV
$V_{i(cm)}$	common mode input voltage		–	2.8	–	V
R_i	input resistance		1	–	–	kΩ
C_i	input capacitance		–	–	5	pF
Analog outputs: pins DPGA1, DPGA1N, DPGA2 and DPGA2N						
$V_{o(max)}$	maximum differential output voltage	at minimum gain	–	0.5	–	V
		at maximum gain	–	0.5	–	V
$V_{o(cm)}$	common mode output voltage		–	3.1	–	V
R_o	output resistance		–	100	160	Ω
C_o	output capacitance		–	–	5	pF
Bandwidth and settling						
B_{-3dB}	−3 dB bandwidth	acquisition channel bandwidth	30	tbf	–	MHz
t_{set}	settling time	full-scale transition	40	–	–	ns
$t_{d(g)}$	group delay	up to f_i = 15 MHz; at minimum gain	–	tbf	–	ps
		up to f_i = 15 MHz; at maximum gain	–	tbf	–	ps

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Gain						
G_{min}	minimum gain setting		tbf	0	tbf	dB
G_{max}	maximum gain setting		tbf	34	tbf	dB
G_{step}	gain step size		–	0.54	–	dB
G_{DNL}	gain step size linearity (actual gain step/average −1)		−0.75	–	+0.75	–
G_f	gain flatness	DC to 15 MHz	–	tbf	–	dB
GE	channel-to-channel gain matching	at minimum gain	–	tbf	–	dB
		at maximum gain	–	tbf	–	dB
$\Delta G_{amp}/\Delta T$	amplifier gain stability as a function of temperature	at minimum gain	–	8	tbf	mdB/°C
		at maximum gain	–	8	tbf	mdB/°C
$\Delta G_{amp}/\Delta V_{CC}$	amplifier gain stability as a function of power supply	at minimum gain	–	0.4	tbf	dB/V
		at maximum gain	–	0.8	tbf	dB/V
Gain switching; T_{amb} = 25 °C						
$t_{st(gain)}$	settling time between two consecutive gain settings	C_L = 470 pF	–	160	–	ns
t_{pd}	propagation delay time		–	–	20	ns
Rejection						
PSRR	power supply rejection ratio	DC to 15 MHz at minimum gain	40	–	–	dB
CMRR	common mode rejection ratio	DC to 15 MHz at maximum gain	40	–	–	dB
Harmonics; T_{amb} = 25 °C						
HD_2	second harmonic distortion at maximum output voltage	f_o = 1 MHz	40	tbf	–	dB
		f_o = 5 MHz	40	tbf	–	dB
		f_o = 10 MHz	40	tbf	–	dB
		f_o = 15 MHz	40	tbf	–	dB
HD_3	third harmonic distortion at maximum output voltage	f_o = 1 MHz	tbf	50	–	dB
		f_o = 5 MHz	tbf	50	–	dB
		f_o = 10 MHz	tbf	50	–	dB
		f_o = 15 MHz	tbf	50	–	dB
Noise						
$V_{n(o)(rms)}$	output referred noise (RMS value)	at maximum gain; Z_i = 50 Ω; 15 MHz noise bandwidth	–	tbf	2	mV

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ADCs (f_{clock} = 80 MHz; from buffer input to digital output, excluding DPGA)						
ANALOG INPUTS: PINS BUF1, BUF1N, BUF2 AND BUF2N						
$V_{i(p-p)}$	input voltage full-scale amplitude	differential (peak-to-peak value)	–	500	–	mV
$R_{BUF(cm)}$	common mode input		–	tbf	–	V
R_i	input impedance		–	20	–	kΩ
C_i	input capacitance		–	3	–	pF
Static linearity						
INL	DC integral non linearity	ramp input	–	±1.0	tbf	LSB
DNL	DC differential non linearity	ramp input	–	±0.75	tbf	LSB
Dynamic performance						
THD	total harmonic distortion	f_i = 4.43 MHz	–	–55	–	dB
SNR	signal-to-noise ratio	without harmonics	–	–46	–	dB
Bandwidth						
$B_{A(-3dB)}$	–3 dB analog bandwidth		–	120	–	MHz
Crosstalk between ADCs						
α_{cc}	crosstalk between channels		–	–	–40	–
Clock inputs: CLK1, CLK1N, CLK2 and CLK2N; note 1						
V_{IL}	LOW-level input voltage		–	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	V_{DDD}	V
I_{IH}	HIGH-level input current		–	–	100	µA
I_{IL}	LOW-level input current		–100	–	–	µA
Digital inputs: OEN and TEN						
V_{IL}	LOW-level input voltage		–	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	V_{DDD}	V
I_{IH}	HIGH-level input current		–5	–	+5	µA
I_{IL}	LOW-level input current		–5	–	+5	µA
Digital outputs: A0 to A7 and B0 to B7						
V_{OL}	LOW-level output voltage		–	–	0.4	V
V_{OH}	HIGH-level output voltage		V_{DDO} – 0.4	–	–	V
I_{OZ}	output current in 3-state mode		–20		+20	µA
Clock timing						
$f_{CLK(max)}$	maximum clock frequency		80	–	–	MHz
t_{CPL}	clock pulse width LOW		5.25	–	–	ns
t_{CPH}	clock pulse width HIGH		5.25	–	–	ns
t_r	clock pulse rise time		–	–	2	ns
t_f	clock pulse fall time		–	–	2	ns

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data timing; f_{CLK} = 80 MHz; C_L = 10 pF; see Fig.4						
t_{ds}	sampling delay time		–	–	tbf	ns
t_d	output delay time		tbf	–	–	ns
t_h	output hold time		–	–	tbf	ns
3-State output delay times; see Fig.5						
t_{dHZ}	output delay enable HIGH		–	tbf	tbf	ns
t_{dZL}	output delay enable LOW		–	tbf	tbf	ns
t_{dHZ}	output delay disable HIGH		–	tbf	tbf	ns
t_{dLZ}	output delay disable LOW		–	tbf	tbf	ns
Reference inputs (V_{ref1} and V_{ref2})						
V_{ref}	control voltage for ADC reference		–	1.24	–	V
R_{ref}	input resistance of ADC reference		–	tbf	–	Ω
C_{ref}	input capacitance of ADC reference		–	–	3	pF
Serial Interface						
DIGITAL INPUTS: PINS SEN1, SEN2, SCLK, SDATA AND SMODE						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	V_{DDD}	V
I_{IH}	HIGH-level input current		–5	0	+5	μA
I_{IL}	LOW-level input current		–5	0	+5	μA
Timing: see Fig.3						
$f_{SCLK(max)}$	maximum clock frequency		5	20	–	MHz
t_{SCLKH}	clock pulse width high		20	–	–	ns
t_{SCLKL}	clock pulse width low		20	–	–	ns
t_{SENS}	SEN to SCLK set-up time		–	–	5	ns
t_{SENH}	SEN to SCLK hold time		–	–	5	ns
t_{SDS}	SDATA to SCLK set-up time		–	–	5	ns
t_{SDH}	SMODE to SCLK hold time		–	–	5	ns
t_{SMODEH}	SMODE to SEND hold time		–	–	5	ns
t_{DSEN}	control register value from SEN rising edge		–	–	5	ns
t_{DSCLK}	control register value from SCLK rising edge		–	–	5	ns

Note

1. Single-ended clock signals are allowed. The non-used clock input is internally biased at the logical threshold (e.g. 1.65 V for nominal supply conditions). This pin should be properly decoupled.
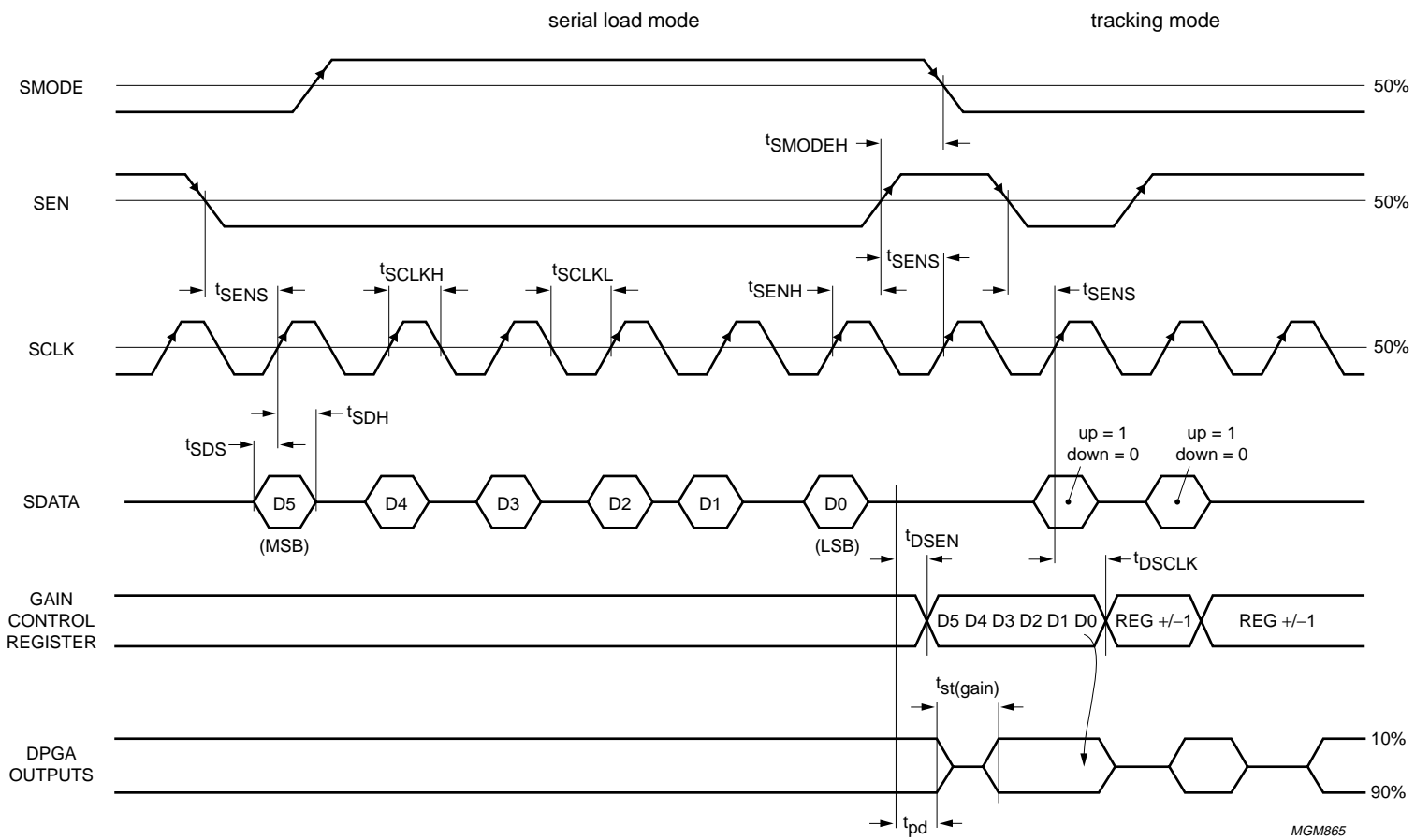
Fig.3 Timing diagram of serial interface.

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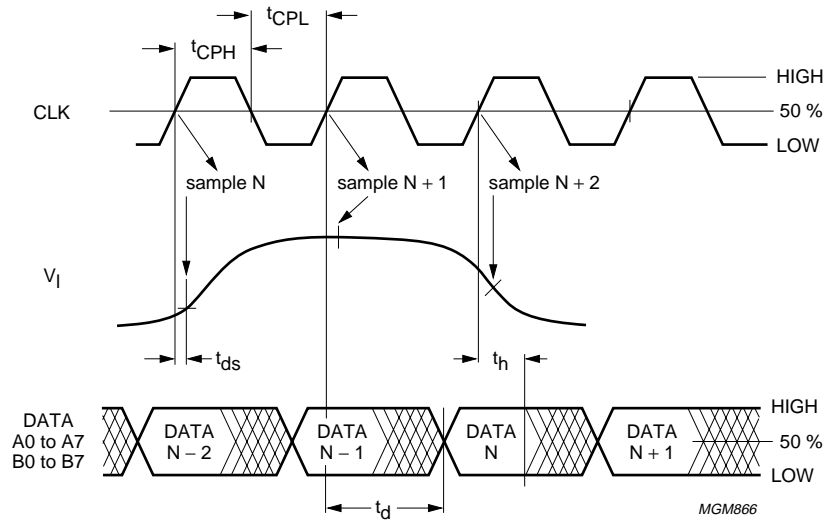
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Fig.4 Timing diagram for the ADC.
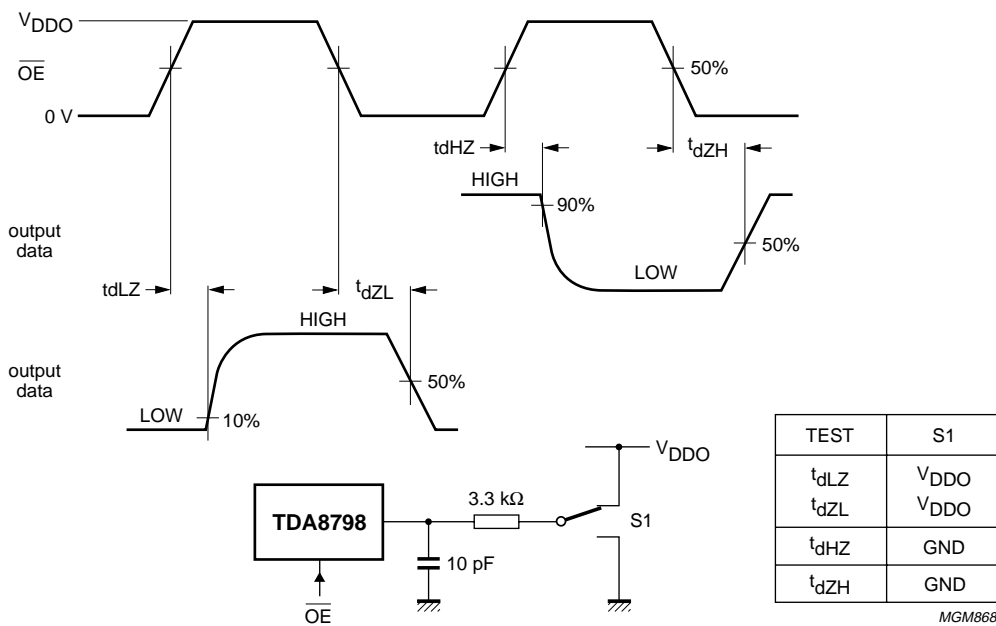
Fig.5 Timing diagram and test conditions of 3-state output delay time.

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TEST AND APPLICATION INFORMATION

TDA8798HL
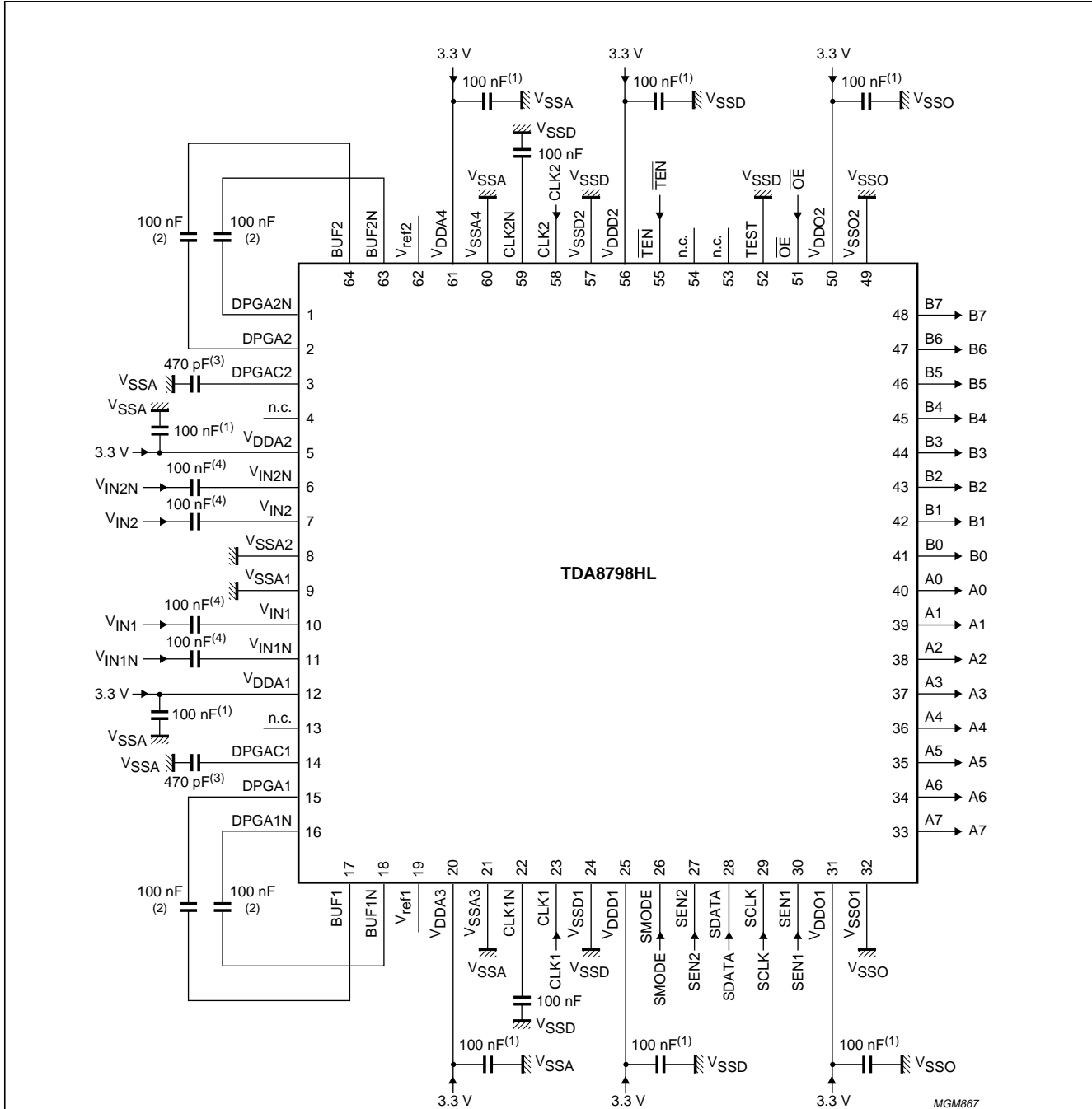
The analog and digital supplies should be separated and decoupled.

(1) Supply decoupling capacitance should be placed as closed as possible to the chip's pin.
 Value may need adjustment depending on the external folting characteristics.

(2) Capacitances may be replaced by an external filter with AC coupling.

(3) Gain settings may be adjusted to other values.

(4) Input capacitances may need adjustment depending on the high pass input filter bandwidth.

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Fig.6 Application diagram.

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Serial interface

Table 1   Serial interface truth table; see notes 1 and 2

SMODE	SCLK	SEN1	SEN2	SDATA	ACTION
0	X, ⎍	1	1	U	WAIT
0	⌐ (rising)	1	1	DI	DEC: DEC ← Di
0	⌐ (rising)	0	1	1	DEC: DEC ← 1 REG1: REG1+1
0	⌐ (rising)	0	1	0	DEC: DEC ← 0 REG1: REG1-1
0	⌐ (rising)	1	0	1	DEC: DEC ← 1 REG2: REG2+1
0	⌐ (rising)	1	0	0	DEC: DEC ← 0 REG2: REG2-1
0	⌐ (rising)	0	0	1	DEC: DEC ← 1 REG1: REG1+1 REG2: REG2+1
0	⌐ (rising)	0	0	0	DEC: DEC ← 0 REG1: REG1-1 REG2: REG2-1
1	X, ⎍	X, ⎍	X, ⎍	U	WAIT
1	⌐ (rising)	X, ⎍	X, ⎍	DI	DEC: DEC ← Di
1	X, ⎍	⌐ (rising)	X, ⎍	U	REG1: DEC
1	X, ⎍	X, ⎍	⌐ (rising)	U	REG2: DEC
1	X, ⎍	⌐ (rising)	⌐ (rising)	U	REG1: DEC REG2: DEC

Notes

1. 'Di←': shift of LSB, loading new LSB with value Di.

2. The up-date of the gain control registers are clipping at the minimum (0) and maximum (63) values.

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Table 2 Abbreviations

SYMBOL	DESCRIPTION
REG1	gain control register value of DPGA1
REG2	gain control register value of DPGA2
DEC	shift register value
X	logic state 0 or logic state 1
⌐ʟ	rising edge
⌐	falling edge
U	undefined logic state X or ⌐ʟ or ⌐

Table 3 Cadre

GAIN CONTROL REGISTER VALUE	GAIN (dB)
000000	0.00
000001	0.54
000010	1.08
...	...
...	...
...	...
111110	33.46
111111	34.00

Table 4 TE truth table

TE	TRACK-AND-HOLD MODE
0	track mode
1	track-and-hold in active mode

INTERNAL PIN CONFIGURATIONS

Fig.7 DPGA1 analog input.

Fig.8 DPGA2 analog input.
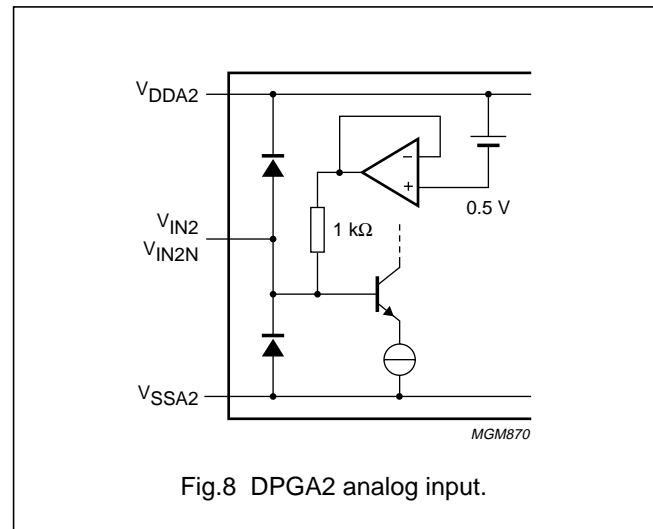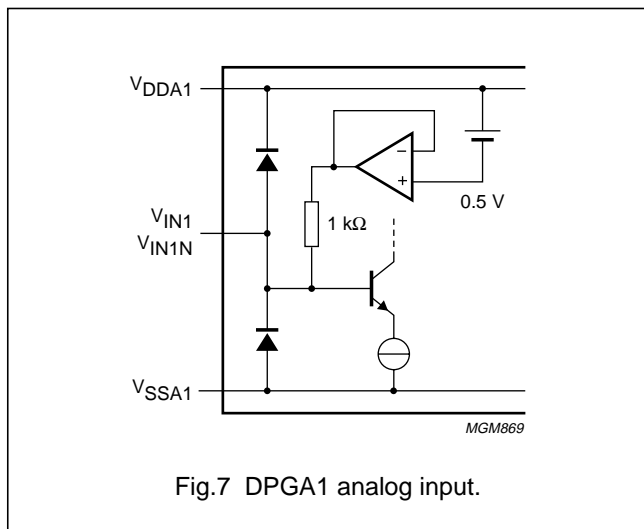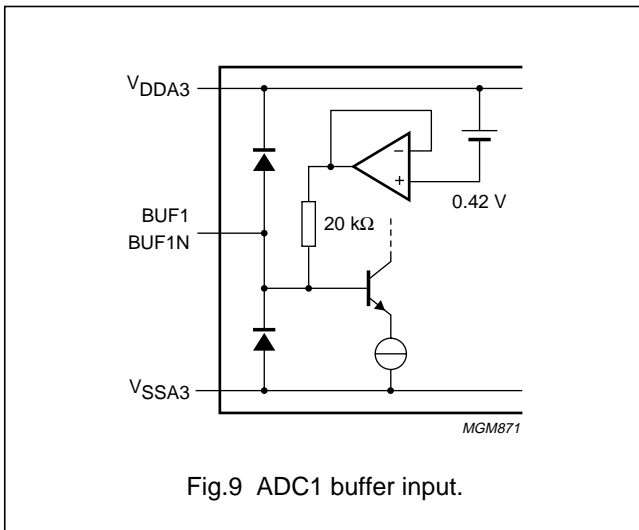
Fig.9 ADC1 buffer input.
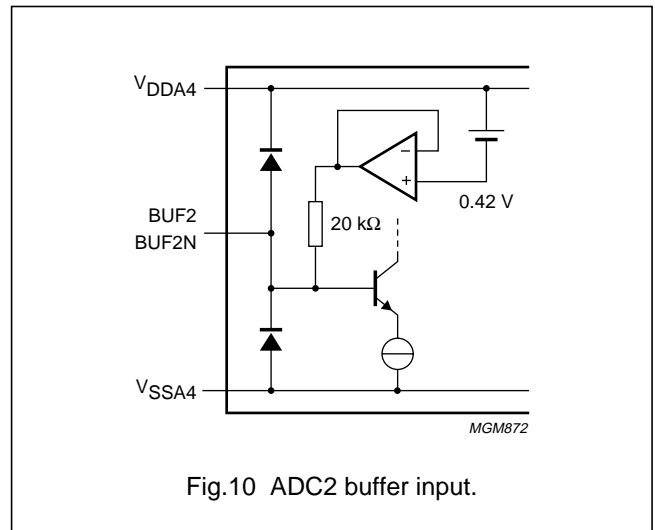
Fig.10 ADC2 buffer input.
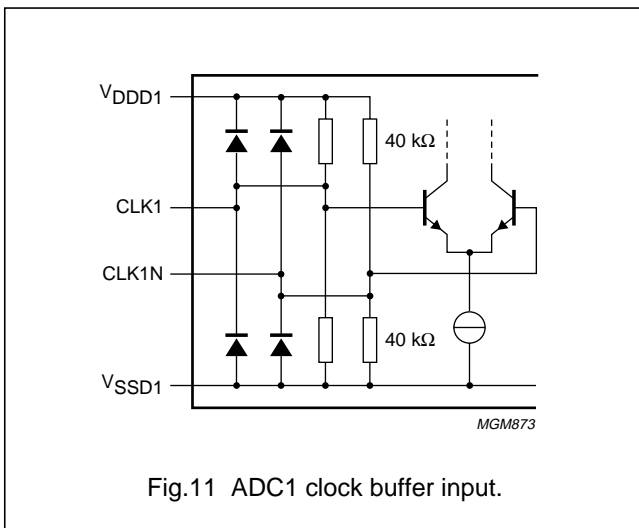
Fig.11 ADC1 clock buffer input.
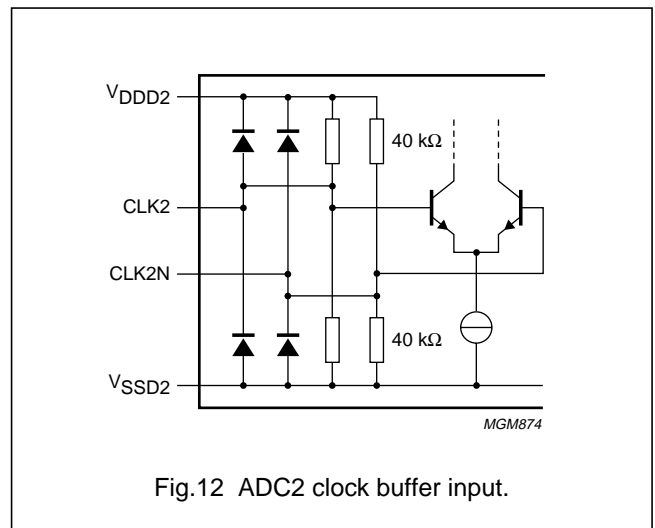
Fig.12 ADC2 clock buffer input.
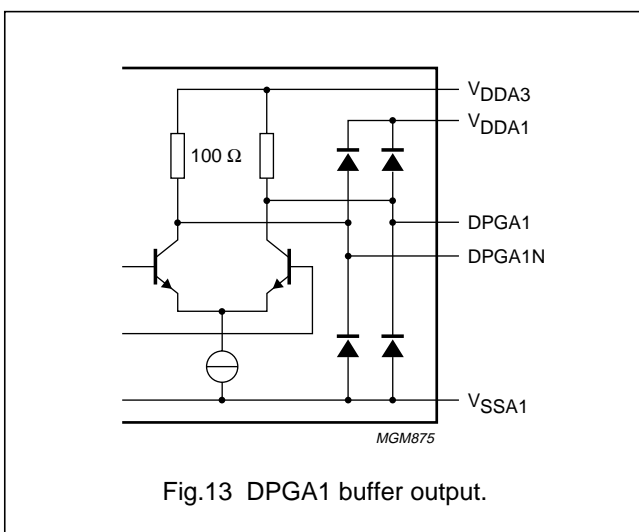
Fig.13 DPGA1 buffer output.
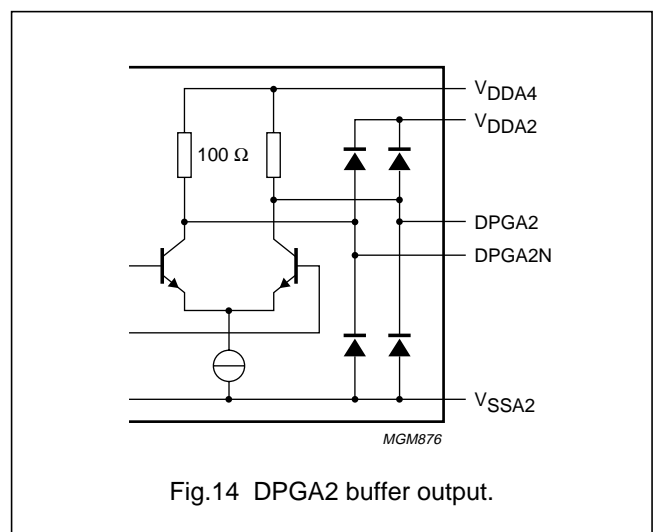
Fig.14 DPGA2 buffer output.
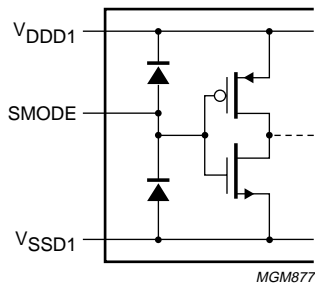
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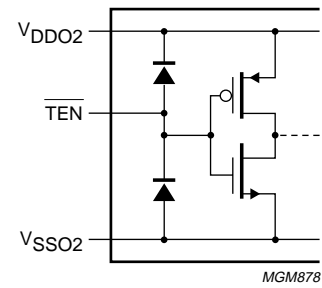Fig.15 SI, SMODE, SEN1, SEN2, SDATA and
SCLK inputs.

Fig.16 $\overline{TEN}$ input.

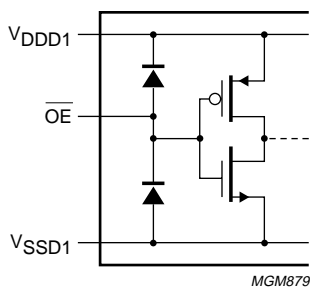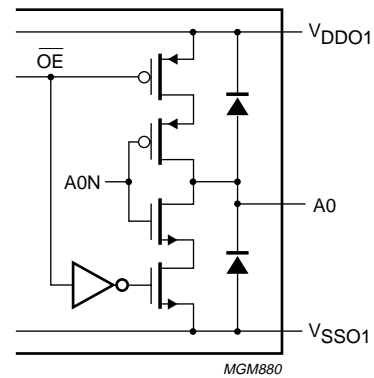Fig.17 $\overline{OE}$ input.

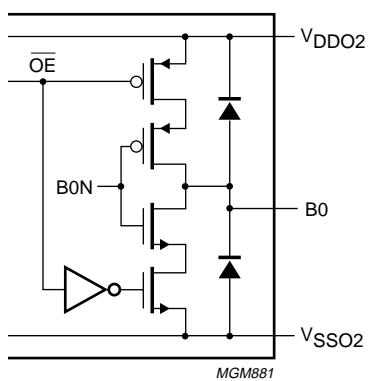Fig.18 ADC1 A0 to A7 outputs.
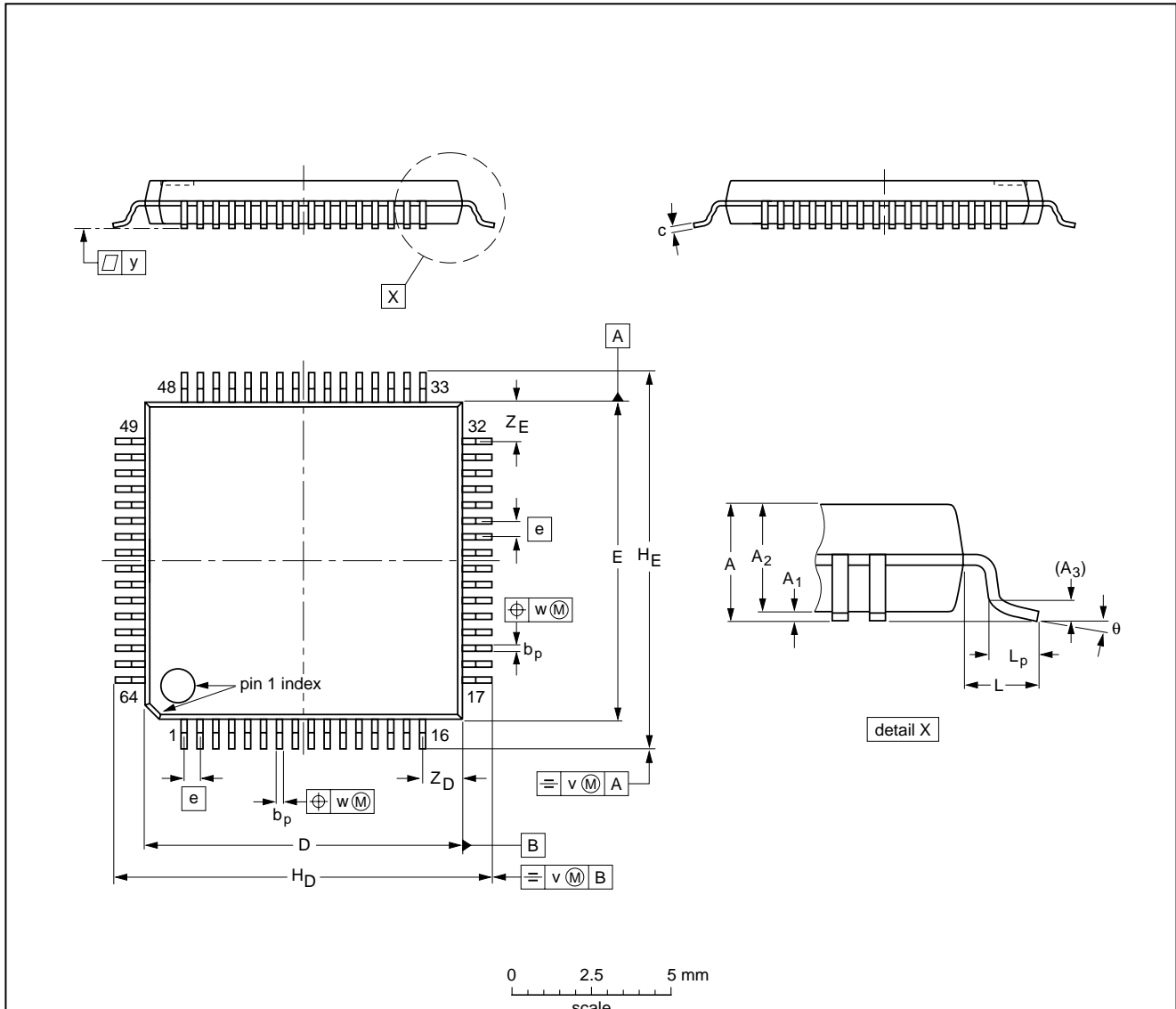
Fig.19 ADC2 B0 to B7 outputs.

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PACKAGE OUTLINE

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm   **SOT314-2**

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A₁	A₂	A₃	bₚ	c	D(1)	E(1)	e	H_D	H_E	L	Lₚ	v	w	y	Z_D(1)	Z_E(1)	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1.0	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT314-2						95-12-19 97-08-01

Dual 8-bit, 80 Msps A/D converter with DPGA

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SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all LQFP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for LQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering LQFP packages LQFP48 (SOT313-2), LQFP64 (SOT314-2) or LQFP80 (SOT315-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 160 1010,
Fax. +43 160 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 0044

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 2233 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 625 344, Fax.+381 11 635 777

For all other countries apply to: Philips Semiconductors,
International Marketing & Sales Communications, Building BE-p, P.O. Box 218,
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