DATA SHEET

TDA9171
YUV picture improvement processor based on histogram modification and blue stretch

Preliminary specification
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Philips Semiconductors

PHILIPS

YUV picture improvement processor based on histogram modification and blue stretch

TDA9171

FEATURES

- Picture content dependent non-linear Y and U,V processing by luminance histogram analysis
- TV standard independent
- Incredible blue stretch
- Optional YC-processing.

GENERAL DESCRIPTION

The TDA9171 is a transparent analog video processor with YUV input and output interfaces.

The luminance transfer is controlled in a non-linear way by the distribution, in 5 discrete histogram sections, of the luminance values measured in a picture. As a result, the contrast ratio of the most important parts of the scene will be improved.

So as to maintain a proper colour reproduction the saturation of the –U and –V colour difference signals are also controlled as a function of the actual non-linearity in the luminance channel.

Optionally, the YUV blue stretch circuitry can be activated which offsets colours near white towards blue.

The supply voltage is 8 V.

The device is contained in a 20 lead dual in-line package.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	7.2	–	8.8	V

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9171	DIP20	plastic dual in-line package; 20 leads; (300 mil); no heat spreader	SOT146-1

BLOCK DIAGRAM

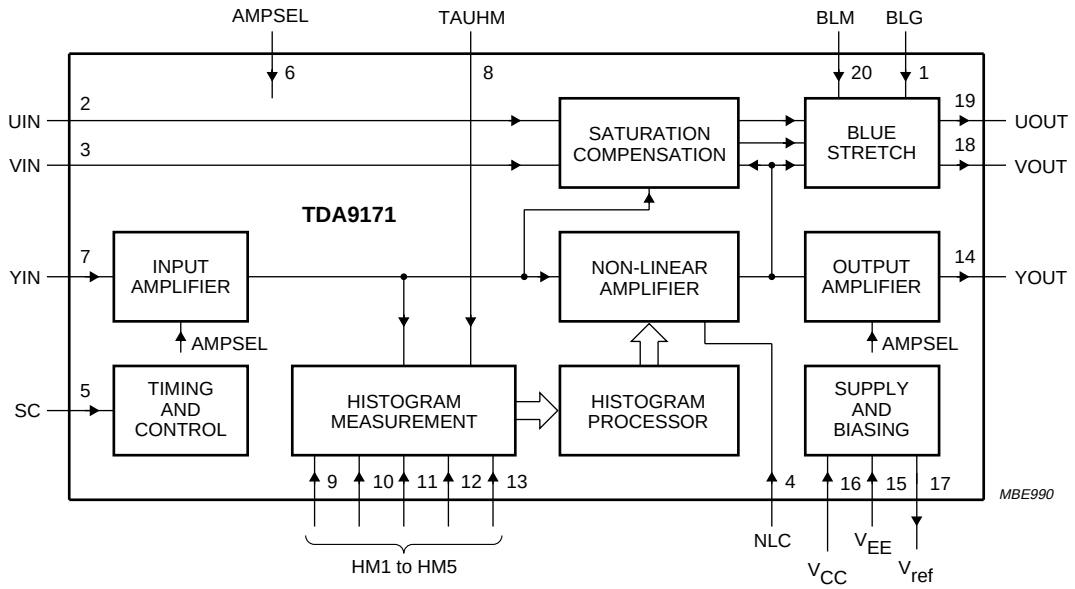


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
BLG	1	blue stretch gain input
UIN	2	U colour difference input –UIN
VIN	3	V colour difference input –VIN
NLC	4	non-linear gain control input
SC	5	sandcastle input
AMPSEL	6	amplitude select input
YIN	7	luminance input
TAUHM	8	time constant histogram input
HM1	9	histogram segment memory 1 input
HM2	10	histogram segment memory 2 input
HM3	11	histogram segment memory 3 input
HM4	12	histogram segment memory 4 input
HM5	13	histogram segment memory 5 input
YOUT	14	luminance output
V_{EE}	15	ground
V_{CC}	16	supply voltage
V_{ref}	17	reference voltage output
VOUT	18	colour difference output –VOUT
UOUT	19	colour difference output –UOUT
BLM	20	activation level blue stretch input

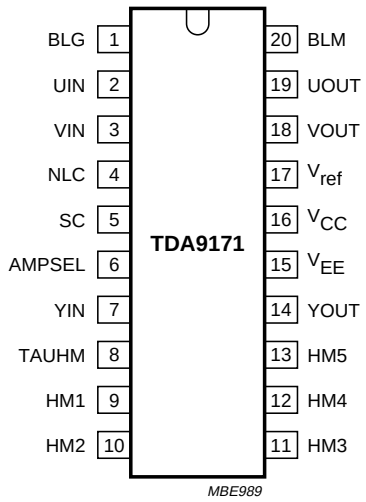


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Input selection and amplification

The dynamic range of the luminance input amplifier is 0.3 or 1 V (excluding sync) typically, depending on the logic level at pin AMPSEL (pin 6). Amplitudes which extend the corresponding specified range will be clipped smoothly, however, the sync is processed to the output transparently. The non-linear gain setting will have minimum effect.

Optionally, in the 1 V input mode, the Y output can be attenuated by a factor of 0.7 by means of an intermediate level at pin AMPSEL. This option is meant for correctly interfacing the combed CVBS signal to the video processor in a YC-application.

The input is clamped during the logic HIGH period of the CLP, defined by the sandcastle reference, and should be DC-decoupled with an external capacitor.

Histogram measurement

For the luminance signal the histogram distribution is measured in real-time over five segments (HM1 to HM5) in each field. During the period that the luminance is in one segment, a corresponding external capacitor HMx is loaded via a current source. At the end of the field five segment voltages are stored from the external capacitors into on-board memories. The external capacitors are discharged and the measurements are repeated.

Parts in the scene that do not contribute to the information in that scene should be omitted from the histogram measurement. No measurements are performed during the blanking period defined by the sandcastle.

The miscount detector disables measurements until it detects changing parts. Additionally, luminance values close to full scale (or white) do not contribute as well in order to maintain the absolute light output. This procedure is allowed because the eye is less sensitive to detail in white.

As the miscount detector shortens the effective measurement period and, because of spreads of internal and external components, the current source is controlled in a closed-loop to provide a constant value of the sum of the segment voltages. The dominant time constant of the closed-loop is external and can be tuned with an appropriate capacitor value at pin TAUHM (pin 8).

Processing of the measured histogram value

FIELD AVERAGING OF HISTOGRAM VALUES

With very rapid picture changes, also related to the field interlace, flicker might result. The histogram values are averaged at the field rate thus reducing the flicker effects. The time constant of the averaging process is adapted to the speed of the histogram changes.

ADAPTIVE WHITE-POINT STRETCHING

For dominant HM4 and HM5 voltages, or large white parts, the histogram conversion procedure makes a transfer with large gain in the white parts, however the amount of light coming out of the scene is considerably reduced. The white stretcher introduces additional overall gain for increased light production and, as a result, violates the principle of having a full scale reference.

STANDARD DEVIATION

For scenes, in which segments of the histogram distribution are very dominant with respect to the others, the non-linear amplification should be reduced in comparison to scenes with a flat histogram distribution. The standard deviation detector measures the spread of the histogram distribution in the segments HM1 to HM5 and modulates the user setting of the non-linear amplifier.

Non-linear amplifier

The stored segment voltages relative to their average value, averaged over two fields, determine the individual gain of each segment in such a way that continuity is guaranteed for the complete range. The maximum and minimum gain of each segment is limited. Apart from the adaptive white-point stretching the black and white references are not affected by the non-linear processing. The amount of linearity can be controlled externally by the NLC pin (Non Linearity Control).

Colour compensation

Non-linear luminance processing influences the colour reproduction, mainly the colour saturation. Therefore, the U and V signals are also processed for saturation compensation.

By convention –U and –V signals must be supplied to the TDA9171. The –U and –V input signals are clamped during the logic HIGH period of CLP, defined by the sandcastle reference. In YC-applications just one colour difference channel is required for processing the chroma signal. However, external decoupling capacitors should be applied to both inputs UIN and VIN. The external coupling capacitor value should be such that the burst period of the chroma signal is very softly clamped.

The processing is dependent on the amplitude and sign of the colour difference signals whenever the blue stretch circuitry is activated. Therefore, both the polarity and the nominal amplitude of the colour difference signals are relevant when using the blue stretch facility.

Blue stretch

The blue stretch circuit is intended to shift colours near white, with sufficient contrast values, towards more blue coloured white to give a brighter impression. The chromaticity shift is proportional to the excess of the contrast value of a white video signal with respect to a user adjustable minimum level, defined by a voltage at pin BLM. In this way blue shift in, for instance, human faces can be prevented. The global amount of blue shift is defined by the voltage level at pin BLG. The direction of shift in the colour triangle is fixed by hardware.

It should be noted that the colour shift is different with a wrong polarity of the colour difference signals. The preferred BLG and BLM settings will be related to the actual nominal amplitudes of the colour difference signals.

The blue stretch facility must be disabled in YC-applications by setting both BLG and BLM to ground.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); all voltages referenced to ground.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	−0.5	+8.8	V
$V_{I/O}$	supply voltage at any other input or output	−0.5	V_{CC} + 0.5	V
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	−10	+70	°C

HANDLING

All pins are protected against ESD by means of internal clamping diodes. The protection circuit meets the following specification:

Human body model: C = 100 pF; R = 1.5 kΩ; all pins >3000 V.

Machine model: C = 200 pF; R = 0 Ω; all pins >300 V.

At an ambient temperature of 90 °C, all pins meet the following specification:

$I_{trigger} > 100$ mA or $V_{pin} > 1.5\ V_{CC(max)}$

$I_{trigger} < -100$ mA or $V_{pin} < -0.5\ V_{CC(max)}$

Except for pins 4, 7, 8 and 17 at positive trigger currents:

Pin 4 (NLC): $I_{trigger} > 90$ mA or $V_{pin} > 1.5V_{CC(max)}$

Pin 7 (YIN): $I_{trigger} > 90$ mA or $V_{pin} > 1.5V_{CC(max)}$

Pin 8 (TAUHM): $I_{trigger} > 90$ mA or $V_{pin} > 1.5V_{CC(max)}$

Pin 17 (V_{ref}): $I_{trigger} > 90$ mA or $V_{pin} > 1.5V_{CC(max)}$

QUALITY SPECIFICATION

In accordance with SNW-FQ-611 part E. The numbers of the quality specification can be found in the *“Quality Reference Handbook”*. The handbook can be ordered using the code 9398 510 63011.

CHARACTERISTICS

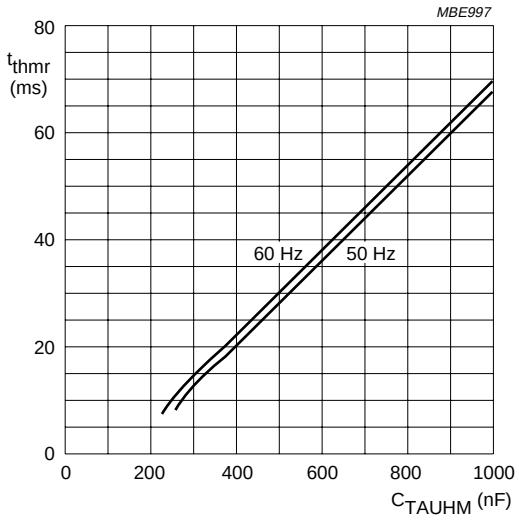
V_{CC} = 8 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CC}	supply voltage		7.2	–	8.8	V
I_{CC}	supply current		–	35	–	mA
V_{ref}	reference voltage		–	5.0	–	V
I_{load}	load current		–	–	1	mA
Luminance input and output selection						
LUMINANCE INPUT (PIN 7)						
$V_{iY(es)}$	input voltage (excluding sync)	$V_{iAMPSEL}$ = low	–	0.3	0.45	V
		$V_{iAMPSEL}$ = middle or high	–	1.0	1.5	V
$V_{iY(cl)}$	input voltage level during clamping		–	1.5	–	V
$I_{Y(bias)}$	input bias current		–	–	0.1	µA
LUMINANCE INPUT VOLTAGE RANGE SELECTION (PIN 6)						
$V_{iAMPSEL(l)}$	input voltage for lower range	$V_{iAMPSEL}$ = low	–	–	0.5	V
$V_{iAMPSEL(h)}$	input voltage for higher range	$V_{iAMPSEL}$ = high	3.5	5.0	5.5	V
$V_{iAMPSEL(m)}$	input voltage for higher range including 0.7 attenuation	$V_{iAMPSEL}$ = middle	1.5	–	2.5	V
$I_{AMPSEL(bias)}$	input bias current		–	–	15	µA
LUMINANCE OUTPUT (PIN 14)						
$V_{oY(es)}$	output voltage (excluding sync)	$V_{iAMPSEL}$ = low	–	0.3	–	V
		$V_{iAMPSEL}$ = high	–	1.0	–	V
$V_{oY(is)}$	output voltage (including sync)	$V_{iAMPSEL}$ = middle	–	1.0	–	V
$V_{oY(cl)}$	output voltage level during clamping	$V_{iAMPSEL}$ = low	–	2.8	–	V
		$V_{iAMPSEL}$ = high	–	1.7	–	V
		$V_{iAMPSEL}$ = middle	–	2.2	–	V
V_{oN}	output voltage noise	with respect to peak white	–	–	–52	dB
B_Y	bandwidth	minimum NLC gain	8	10	–	MHz
$B_{Y(nl)}$	bandwidth non-linear processing		10	–	–	MHz
E_{bl}	black level error	minimum NLC gain	–	–	1.0	%
$E_{G(n)}$	nominal gain error	minimum NLC gain; $V_{iAMPSEL}$ = low	–	–	7	%
		minimum NLC gain; $V_{iAMPSEL}$ = middle or high	–	–	5	%
C_L	load capacitance	f_i = 5 MHz	–	–	25	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Histogram measurement						
HISTOGRAM UPDATES AT HMX (PINS 9 TO 13)						
Q_{HMb}	segment bleeder accuracy		–	–	2	%
$V_{HM(av)}$	average voltage level for 5 segments		–	1.0	–	V
$V_{HM(min)}$	minimum segment voltage level		0	–	–	V
$V_{HM(max)}$	maximum segment voltage level		–	5.0	–	V
I_{HMbias}	input bias current		–	–	0.1	µA
TIME CONSTANT CONTROL TAUHM (PIN 8)						
t_{thmr}	response speed	see Fig.3	–	–	–	
Q_{thms}	static error	see Fig.4	–	–	–	
$I_{thm(bias)}$	input bias current		–	–	0.1	µA
$V_{thm(l)}$	control voltage lower limit		–	1.0	–	V
$V_{thm(h)}$	control voltage upper limit		–	2.0	–	V
MISCOUNT DETECTION						
$Q_{mc(d)}$	miscount detection level		–	4	–	%
$t_{d(mcp)}$	miscount propagation delay	20% step	–	25	–	ns
$t_{mcd(o)}$	miscount detection on-time each event		–	0.36	–	µs
t_{mcY}	mismatch propagation delay and luminance delay		–	–	20	ns
$Q_{mc(aW)}$	miscount activation level at white	no miscount	–	90	–	%
$Q_{mc(dW)}$	miscount deactivation level at white	miscount	–	87	–	%
Processing of measured histogram values						
WHITE POINT STRETCH						
G_{WP}	maximum gain luminance for white stretch (HM pattern = 00113)	maximum NLC gain	–	1.1	–	
Non-linear amplifier						
NON-LINEAR GAIN SET BY HMX (PINS 9 TO 13)						
$Q_{nl(b)}$	segment bleeder accuracy		–	–	3	%
$G_{nlc(min)}$	minimum gain segment (HM pattern = 31100)	maximum NLC gain	–	0.36	–	
$G_{nlc(max)}$	maximum gain segment (HM pattern = 31100)	maximum NLC gain	–	2.28	–	
NON-LINEAR SETTING NLC (PIN 4)						
G_{nlc}	non-linear control curve	see Fig.5	–	–	–	
$V_{iNLC(l)}$	control voltage lower limit		–	0	–	V
$V_{iNLC(h)}$	control voltage upper limit		–	5.0	–	V
$I_{iNLC(bias)}$	input bias current		–	–	0.5	µA

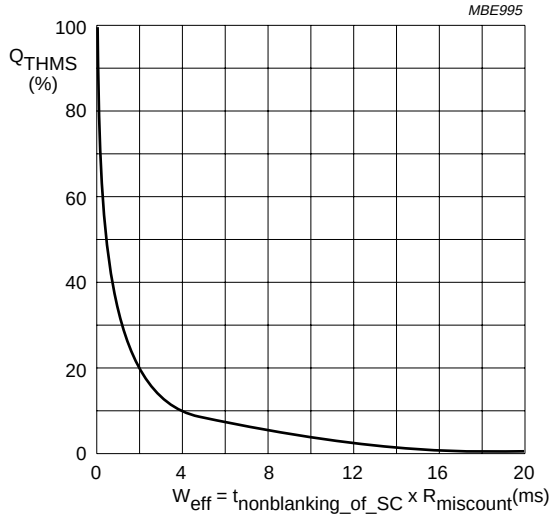
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Colour difference processing						
COLOUR DIFFERENCE INPUTS UIN AND VIN (PINS 2 AND 3)						
$V_{iU(p-p)}$	input voltage (pin 2) (peak-to-peak value)		–	1.33	1.8	V
$V_{iV(p-p)}$	input voltage (pin 3) (peak-to-peak value)		–	1.05	1.8	V
$I_{UV(bias)}$	input bias current (pins 2 and 3)		–	–	0.1	µA
$V_{iUV(cl)}$	input voltage level during clamping		–	1.5	–	V
COLOUR DIFFERENCE OUTPUTS UOUT AND VOUT (PINS 19 AND 18)						
V_{oU}	output voltage with respect to pin 2		150	–	–	%
V_{oV}	output voltage with respect to pin 3		150	–	–	%
$V_{oUV(cl)}$	output voltage level during clamping		–	2.3	–	V
$E_{os(UV)}$	offset error	minimum BLG and BLM; minimum NLC gain	–	–	1	%
$G_{E(UV)}$	gain error	minimum BLG and BLM; minimum NLC gain	–	–	10	%
$G_{M(UV)}$	gain mismatch	minimum BLG and BLM; minimum NLC gain	–	–	5	%
B_{UV}	bandwidth	minimum BLG and BLM; minimum NLC gain	10	–	–	MHz
Blue stretch						
CHROMATICITY SHIFT						
ΔV_{oU}	variation of U output voltage in white part of 100% colour bar	BLM = 4.06 V	–	–0.375	–	V
ΔV_{oV}	variation of V output voltage in white part of 100% colour bar	BLG = 3.25 V	–	0.150	–	V
BLUE STRETCH ACTIVATION AREA (PIN 20)						
	minimum contrast level range	see Fig.6	–	–	–	
$V_{iBLM(l)}$	input control voltage lower limit		–	0	–	V
$V_{iBLM(h)}$	input control voltage upper limit		–	5.0	–	V
$I_{BLM(bias)}$	input bias current		–	–	0.5	µA
BLUE STRETCH GAIN (PIN 1)						
G_{BLG}	blue stretch gain range	see Fig.7	–	–	–	
$V_{iBLG(l)}$	input voltage lower limit		–	0	–	V
$V_{iBLG(h)}$	input voltage upper limit		–	5.0	–	V
$I_{BLG(bias)}$	input bias current		–	–	0.5	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing						
SANDCASTLE INPUT (PIN 5)						
V_{iSC}	input voltage detection level blanking	no clamp	1.0	1.25	1.5	V
		with clamp	3.5	3.8	4.2	V
$t_{SC(sw)}$	input sync width	for no vertical sync	–	–	15	µs
		for vertical sync	35	–	–	µs
CLP PULSE WIDTH RESTORATION						
$t_{CLP(diff)}$	internal CLP pulse width difference		–	–30	–	%
Overall output performance						
TRANSPARENT MODE (NO BLUE STRETCH; NO NON-LINEAR GAIN)						
$t_{d(YUV)}$	delay from input to output of YUV signals	minimum BLG and BLM; minimum NLC gain	–	50	100	ns
$t_{d(YUV)m}$	matching of YUV delay	minimum BLG and BLM; minimum NLC gain	–	10	20	ns



$R_{miscount}$ = ratio of effective histogram measuring time and active video in one field defined by the non-blanking periods of the sandcastle signal in one field.

Fig.3 Response speed of average histogram amplitude control loop as a function of C_{TAUHM} at both 50 and 60 Hz field rate ($R_{miscount}$ = 1; C_{HMx} = 10 nF).



$R_{miscount}$ = ratio of effective histogram measuring time and active video in one field defined by the non-blanking periods of the sandcastle signal in one field.

Fig.4 Static error on average histogram amplitude (pin TAUHM) as a function of effective histogram measuring time in a field (C_{HMx} = 10 nF).

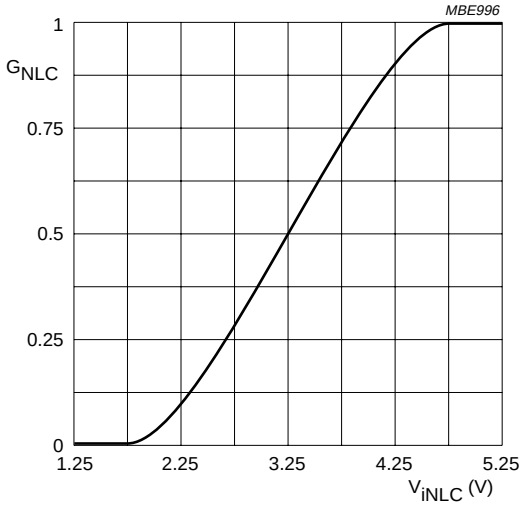
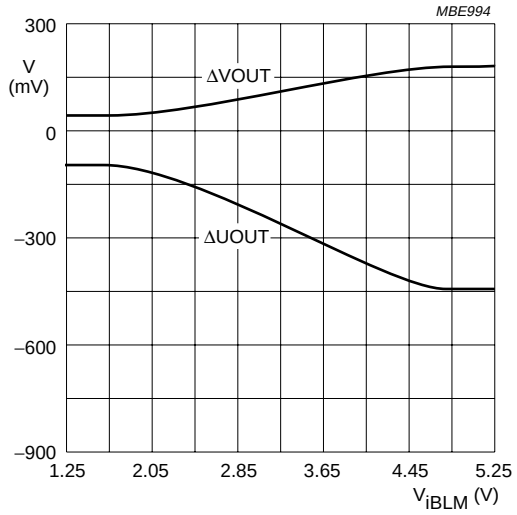
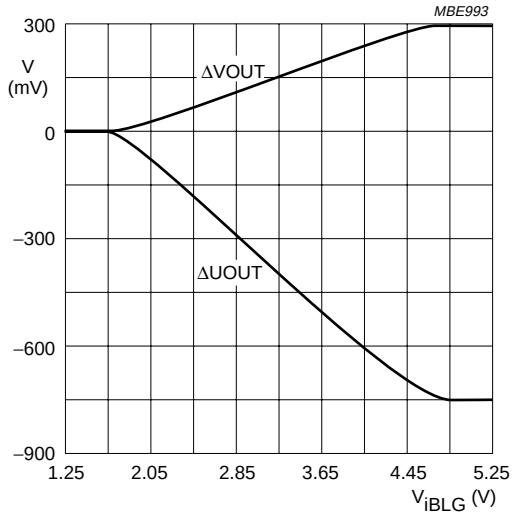


Fig.5 Non-linear amplifier gain as a function of input voltage at pin NLC.



UIN = VIN = 0; YIN = 100%; V_{iBLG} = 3.25 V.

Fig.6 Blue stretch activation area as a function of input voltage at pin BLM.



UIN = VIN = 0; YIN = 100%; V_{iBLM} = 4.06 V.

Fig.7 Blue stretch gain as a function of input voltage at pin BLG.

TEST AND APPLICATION INFORMATION

The TDA9171 is especially designed for YUV applications. A typical application diagram is shown in Fig.8. Jumpers J1 and J2 can be used to select the appropriate luminance amplitude mode. Potentiometers BLG, BLM and NLC can be used to apply proper blue stretch and non-linear amplifier control voltages.

The TDA9171 is also prepared for YC-processing. A typical application diagram is shown in Fig.9. Jumpers J1 and J2 can be used to select the appropriate luminance amplitude mode. Potentiometer NLC can be used to apply the proper non-linear amplifier control voltage. For the chroma processing either the U- or V-channel can be used, however both channels need to be DC-decoupled and the DC-decoupling capacitor value should be such that the burst period of the chroma signal C_{in} is very softly clamped. The blue stretch circuitry cannot be used in YC-applications and should be switched off by connecting both blue stretch adjustments (BLG and BLG) to ground.

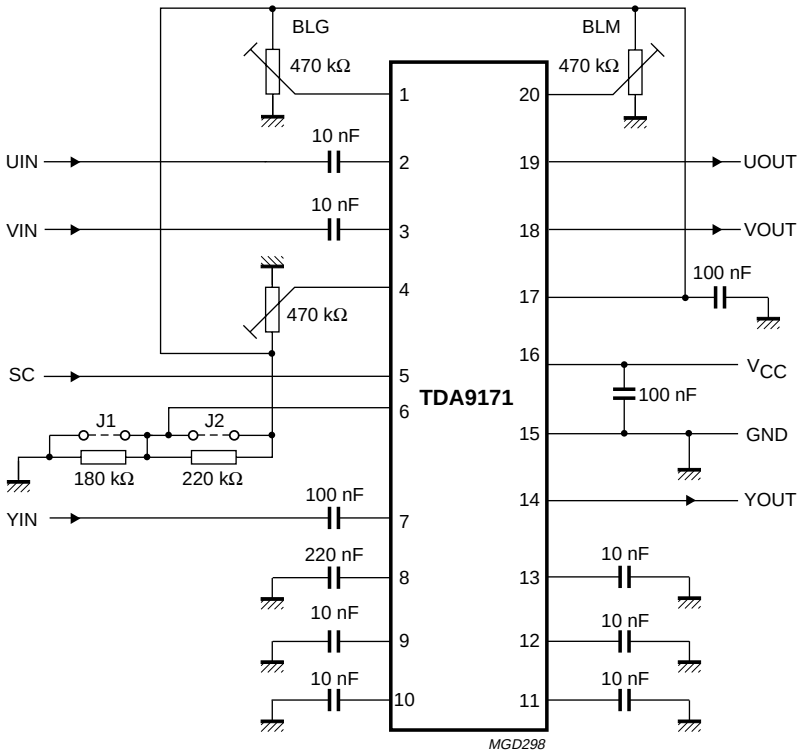


Fig.8 YUV application.

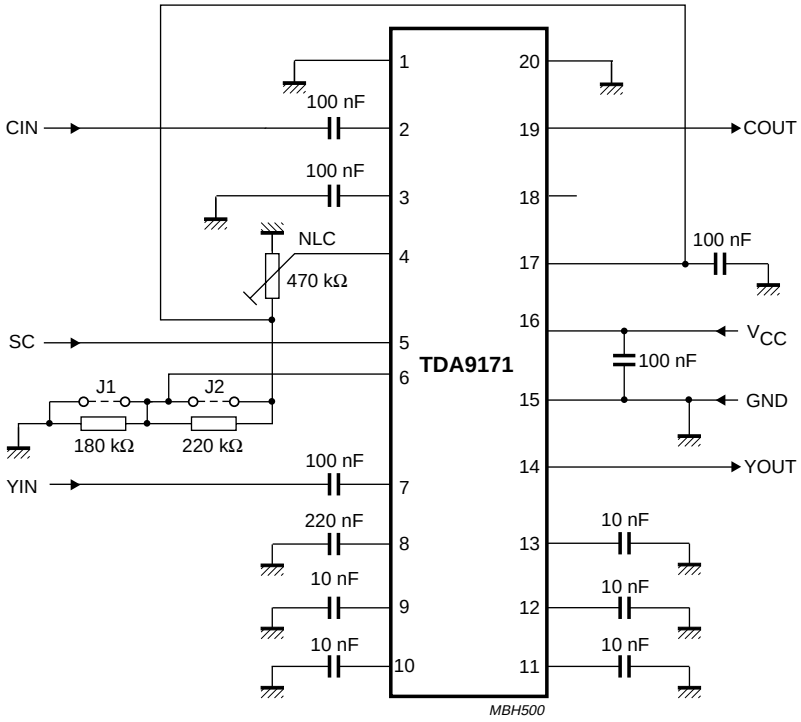
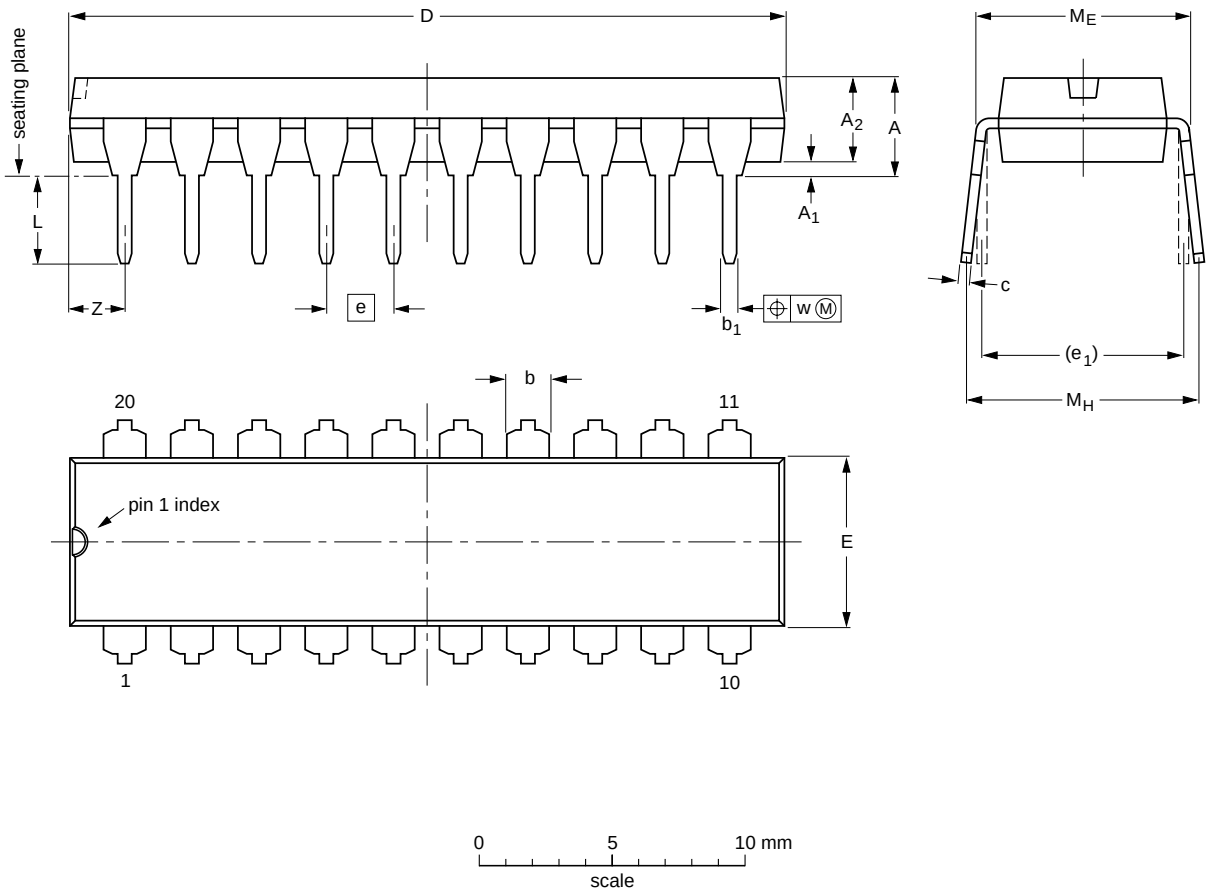


Fig.9 YC application.

PACKAGE OUTLINE

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

SOLDERING DIP, SDIP, HDIP, DBS and SIL

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these cases reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dip or wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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