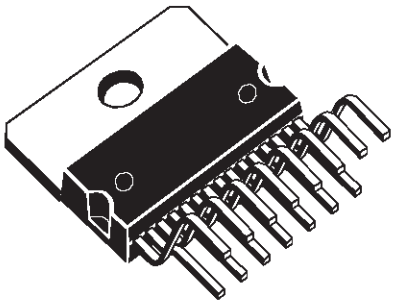
TDA9533

7.5NS TRIPLE-CHANNEL HIGH VOLTAGE VIDEO AMPLIFIER INCLUDING CUT-OFF INPUTS

FEATURES

- Triple-Channel Video Amplifier
- Supports DC or AC coupling applications
- Built-in Voltage Gain: 19.3
- Rise and Fall Times: 7.5ns (Typ.)
- Bandwidth: 50MHz (Typ.)
- Supply Voltage: 110V
- Cut-off Inputs



MULTIWATT 15
(Plastic Package)

ORDER CODE: TDA9533

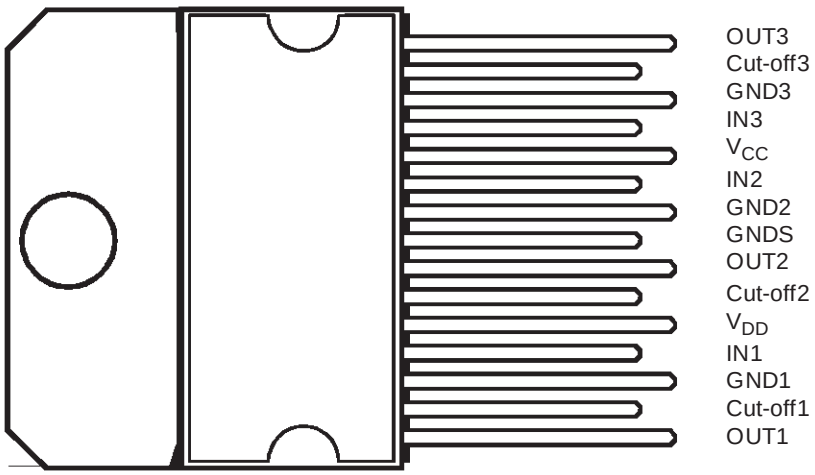
DESCRIPTION

The TDA9533 is a triple-channel video amplifier designed in BCD technology (Bipolar/CMOS/DMOS) able to drive the 3 cathodes of a CRT monitor in DC or AC coupling mode.

In DC coupling, the cut-offs are adjusted either by the cut-off inputs (controlled for example by the TDA9207 from ST) or directly by the video inputs via the TDA9207/9209/9210 Preamplifiers.

The TDA9533 is embedded in a Multiwatt 15 plastic package.

PIN CONNECTIONS

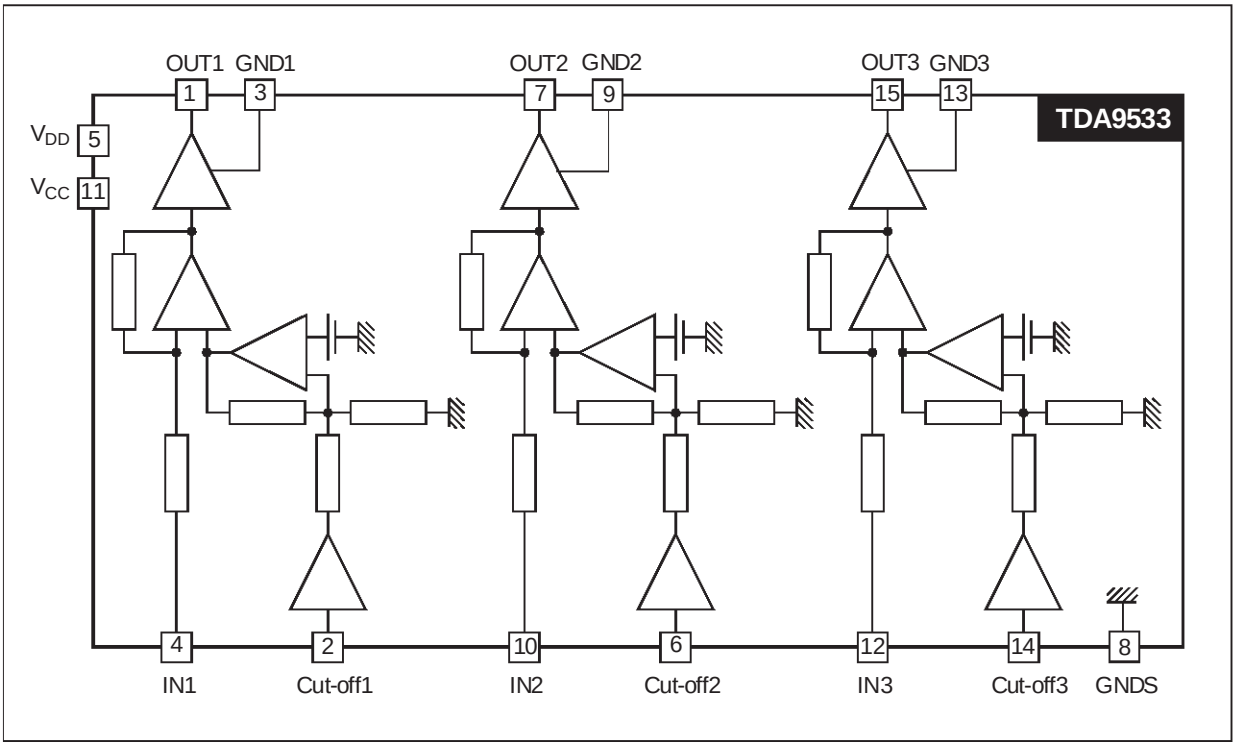


Revision 4.1

Table of Contents

1 - BLOCK DIAGRAM 3
2 - PIN CONNECTIONS 3
3 - ABSOLUTE MAXIMUM RATINGS 4
4 - THERMAL DATA 4
5 - ELECTRICAL CHARACTERISTICS 5
6 - THEORY OF OPERATION 7
6.1 - General 7
6.2 - How to choose the high supply voltage (VDD) 7
6.3 - Amplifier gain and cut-off adjustment 8
7 - ARCING PROTECTION 9
8 - VIDEO RESPONSE OPTIMIZATION 10
8.1 - Supply decoupling 10
8.2 - Tracks 10
8.3 - Network adjustment 10
9 - POWER DISSIPATION 11
10 - TYPICAL PERFORMANCE CHARACTERISTICS 12
11 - PACKAGE MECHANICAL DATA 15

1 - BLOCK DIAGRAM OF THE TDA9533



2 - PIN CONNECTIONS

Pin	Name	Function
1	OUT1	Output-Channel 1
2	Cut-off1	Cut-off Output/ Feedback Input-Channel 1
3	GND1	Power Ground-Channel 1
4	IN1	Video Input-Channel 1
5	V_{DD}	Amplifier High Supply Voltage
6	Cut-off2	Cut-off Output/ Feedback Input Channel 2
7	OUT2	Output-Channel 2
8	GNDS	Ground Substrat
9	GND2	Power Ground-Channel 2
10	IN2	Video Input-Channel 2
11	V_{CC}	Low Supply Voltage
12	IN3	Video Input-Channel 3
13	GND3	Power Ground-Channel 3
14	Cut-off3	Cut-off Output/ Feedback Input-Channel 3
15	OUT3	Output-Channel 3

3 - ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	High supply voltage	120	V
V_{CC}	Low supply voltage	17	V
V_{ESD}	ESD susceptibility Human Body Model (100pF discharged through 1.5KΩ) EIAJ norm (200pF discharged through 0Ω)	 2 300	 kV V
I_{OD}	Output source current (pulsed < 50µs)	80	mA
I_{OG}	Output sink current (pulsed < 50µs)	80	mA
$V_{IN\ Max}$	Maximum Input Voltage	15	V
$V_{IN\ Min}$	Minimum Input Voltage	- 0.5	V
$V_{Cut\text{-}off\ Max}$	Maximum Cut-off Input Voltage	V_{CC} + 0.5	V
$V_{Cut\text{-}off\ Min}$	Minimum Cut-off Input Voltage	- 0.5	V
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-20 + 150	°C

4 - THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ (j\text{-}c)}$	Max. Junction-Case Thermal Resistance	3	°C/W
$R_{th\ (j\text{-}a)}$	Typical Junction-Ambient Thermal Resistance	35	°C/W

5 - ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ	Max	Unit
SUPPLY parameters (V_{CC} = 12V, V_{DD} = 110V, $V_{Cut-off}$ = 2.5V, Tamb = 25 °C, unless otherwise specified)						
V_{DD}	High supply voltage (Pin 5)		20	110	115	V
V_{CC}	Low supply voltage (Pin 11)		10	12	15	V
I_{DD}	V_{DD} supply current	V_{OUT} = 50V		25		mA
I_{DDS}	V_{DD} stand-by supply current	V_{CC} : switched off (<1.5V) V_{OUT}: high (Note 1)		12		mA
I_{CC}	V_{CC} Internal DC current	V_{OUT} = 50V		60		mA
STATIC parameters (V_{CC} = 12V, V_{DD} = 110V, $V_{Cut-off}$ = 2.5V, Tamb = 25 °C)						
dV_{OUT}/dV_{DD}	High Voltage supply rejection	V_{OUT} = 50V		0.5		%
dV_{OUT}/dT	Output Voltage drift versus temperature	V_{OUT} = 80V		15		mV/°C
$d\Delta V_{OUT}/dT$	Output voltage matching versus temperature (Note 3)	V_{OUT} = 80V		5		mV/°C
$\Delta V_{OUT}/\Delta V_{Cut-off}$	Cut-off Control Gain	V_{OUT} = 80V 1V < $V_{Cut-off}$< 4V		14		
$I_{Cut-off}$	Cut-off Control Bias Current	V_{OUT} = 80V			10	µA
R_{IN}	Video Input Resistor	V_{OUT} = 50V		2		kΩ
V_{SATH}	Output Saturation Voltage to Supply	I_0 =-60mA (Note 2)		V_{DD} - 6.5		V
V_{SATL}	Output Saturation Voltage to GND	I_0 =60mA (Note 2)		11		V
VG	Video Gain	V_{OUT} = 50V		19.3		
LE	Linearity Error	17<V_{OUT}<V_{DD}-15V		5	8	%

Note 1: The TDA9533 goes into stand-by mode when Vcc is switched off (<1.5V). In stand-by mode, Vout is set to high level.

Note 2: Matching measured between each channel

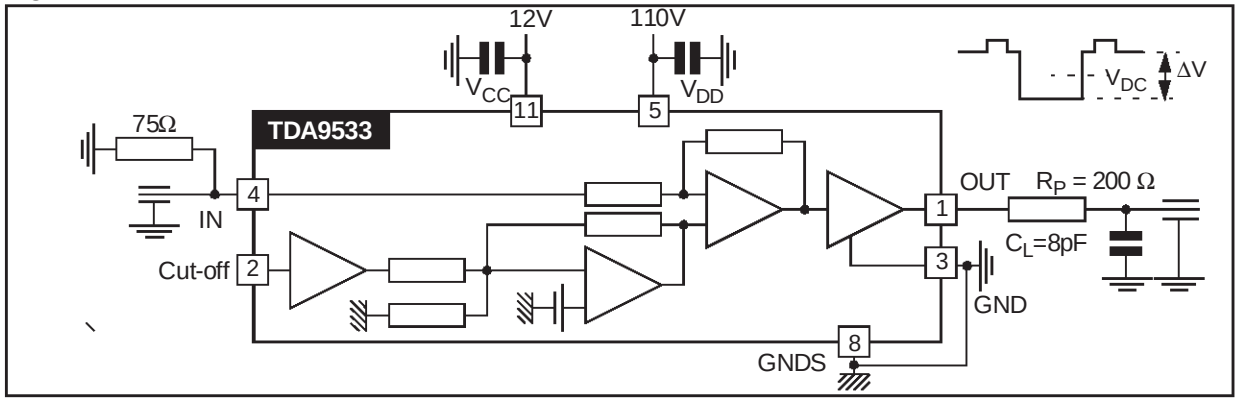
Note 3: Pulsed current width < 50µs

Electrical characteristics (continued)

Symbol	Parameter	Test Conditions	Min.	Typ	Max	Unit
DYNAMIC parameters (see Figure 1)						
OS1	Overshoot, White to Black transition			5		%
OS2	Overshoot, Black to White transition			1		%
ΔVG	Low frequency gain matching (Note 4)	V_{DC} = 50V, f=1MHz			5	%
BW	Bandwidth at -3dB	V_{DC}=50V, ΔV=20V_{PP}		50		MHz
t_R	Rise time	V_{DC}=50V, ΔV=40V_{PP}		7.2		ns
t_F	Fall time	V_{DC}=50V, ΔV=40V_{PP}		7.9		
t_{SET}	2.5% Settling time	V_{DC}=50V, ΔV=40V_{PP}		15		ns
CT_L	Low frequency Crosstalk	V_{DC}=50V,ΔV=20V_{PP} f = 1 MHz		50		dB
CT_H	High frequency Crosstalk	V_{DC}=50V,ΔV=20V_{PP} f = 20MHz		32		dB

Note 4: Matching measured between each channel

Figure 1. AC test circuit



6 - THEORY OF OPERATION

6.1 - General

The TDA9533 is a three-channel video amplifier supplied by a low supply voltage: V_{CC} (typ.12V) and a high supply voltage: V_{DD} (up to 115V).

The high values of V_{DD} supplying the amplifier output stage allow direct control of the CRT cathodes (DC coupling mode).

In DC coupling mode, the application schematic is very simple and only a few external components are needed to drive the cathodes. In particular, there is no need of the DC-restore circuitry which is used in classical AC coupling applications.

The output voltage range is wide enough (Figure 2) to provide simultaneously :

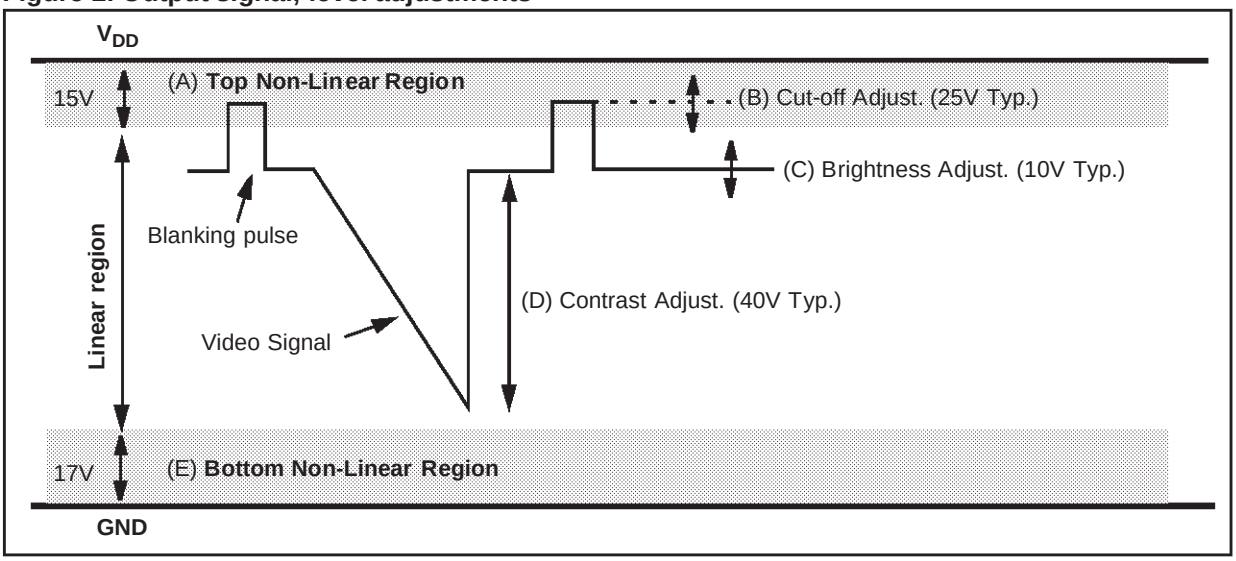
– Cut-off adjustment (typ. 25V)

– Video contrast (typ. up to 40V),

– Brightness (with the remaining voltage range).

In normal operation, the output video signal must remain inside the linear region whatever the cut-off / brightness / contrast adjustment is.

Figure 2. Output signal, level adjustments



6.2 - How to choose the high supply voltage value (V_{DD})

The V_{DD} high supply voltage must be chosen carefully. It must be high enough to provide the necessary video adjustment but set to minimum value to avoid unecessary power dissipation.

Example:

The following example shows how the optimum V_{DD} voltage value is determined:

– Cut-off adjustment range (B) : 25V

– Max contrast (D) : 40V

Case 1:

10V Brightness (C) adjusted by the preamplifier :

V_{DD} = A + B + C + D + E

V_{DD} = 15V + 25V + 10V + 40V + 17V = 107V

Case 2:

10V Brightness (C) adjusted by the G1 anode:

V_{DD} = A + B + D + E

V_{DD} = 15V + 25V + 40V + 17V = 97V

6.3 - Amplifier gain and cut-off adjustment

A very simplified schematic of each TDA9533 channel is shown in Figure 3.

The feedback net of each channel is integrated with a built-in voltage gain of 19.3 (40k/2k).

The cut-off level of each channel is controlled by the cut-off input. Vref is adjustable from 1 to 6V according to the formula:

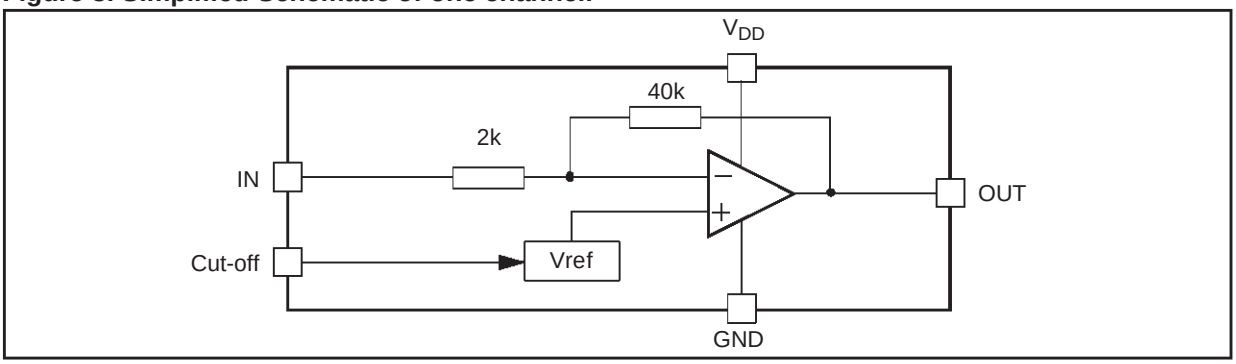
$$Vref = \frac{10 - V_{Cut-off}}{1.5}$$

The total gain of the amplifier related to $V_{Cut-off}$ is 14. Consequently we have:

$V_{OUT} = 140 - (14 \times V_{Cut-off}) - (19.3 \times V_{IN})$

Caution: If not used, the cut-off inputs have to be set to DC voltage. The value of this DC voltage is chosen to reach the optimum value of cut-off output (see Figure 7).

Figure 3. Simplified Schematic of one channell



7 - ARCING PROTECTION

As the amplifier outputs are connected to the CRT cathodes, special attention must be given to protect them against possible arcing inside the CRT.

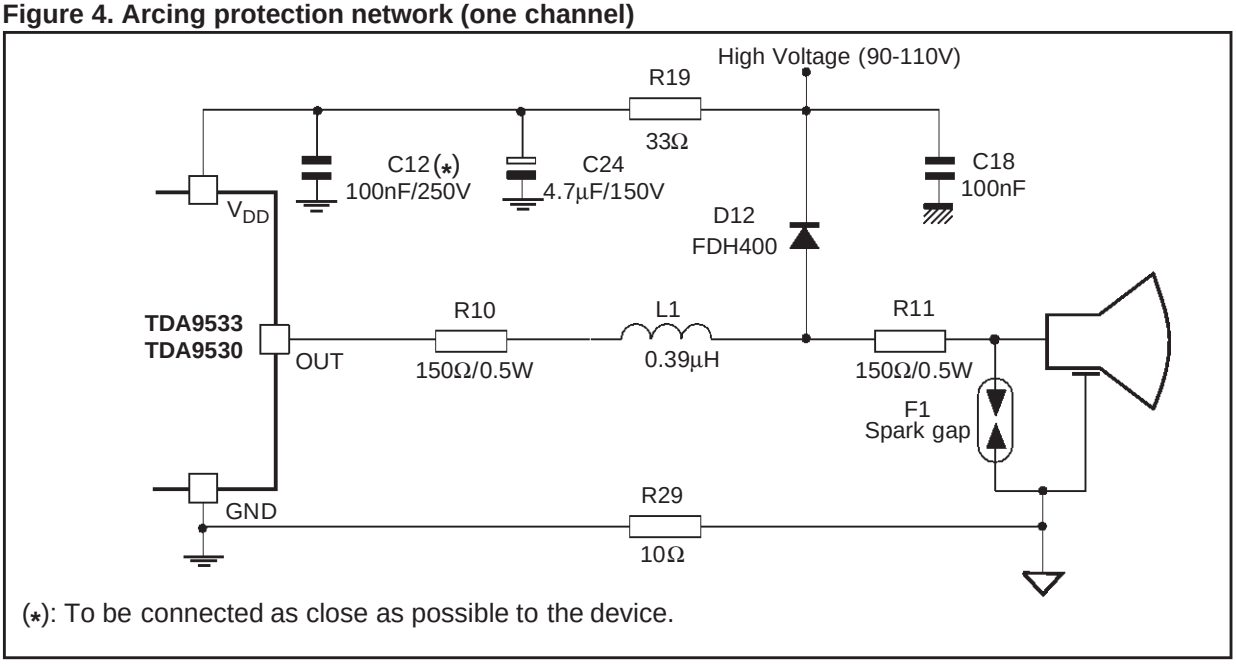
Protection must be considered when starting the design of the video CRT board. It should always be implemented before starting to adjust the dynamic video response of the system.

The arcing network that we recommend (see Figure 4) provides efficient protection without deteriorating the amplifier video performances.

The total resistance value between the amplifier and the CRT cathode (R10+R11) should not be less than 300 Ω.

Spark gap diodes are strongly recommended.

Figure 4. Arcing protection network (one channel)



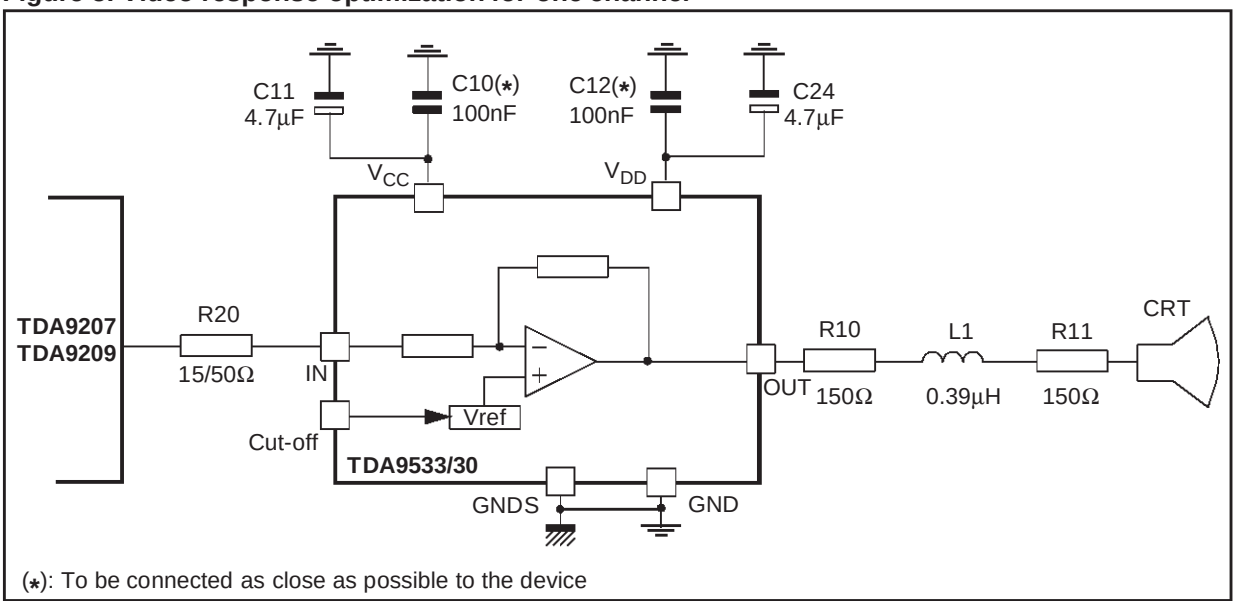
(*): To be connected as close as possible to the device.

8 - VIDEO RESPONSE OPTIMIZATION

The dynamic video response is optimized by carefully designing the supply decoupling of the video board (see 8.1), the tracks (see 8.2), then by adjusting the input/output component network (see 8.3).

For dynamic measurements such as rise/fall time and bandwidth, a 8pF load is used (total load including the parasitic capacitance of the PC board and CRT Socket).

Figure 5. Video response optimization for one channel



(*): To be connected as close as possible to the device

8.1 - Supply decoupling

The decoupling of V_{CC} and V_{DD} through good quality HF capacitors (respectively C10 and C12) close to the device is necessary to improve the dynamic performance of the video signal.

8.2 - Tracks

Careful attention must be given to the three output channels of the amplifier.

– Capacitor: The parasitic capacitive load on the amplifier outputs must be as small as possible. Figure 11 clearly shows the deterioration of the t_R/t_F when the capacitive load increases. Reducing this capacitive load is achieved moving away the output tracks from the other tracks (especially ground) and by using thin tracks (<0.5mm), see Figure 12.

– Cross talk: Output and input tracks must be set apart.

– Length: Connection between amplifier output and cathode must be as short and direct as possible.

8.3 - Network adjustment

Video response is always a compromise between several parameters. An improvement of the rise/fall time leads to a deterioration of the overshoot.

The recommended way to optimize the video response is:

1 To set R10+R11 for arcing protection (min. 300 Ω)

2 To adjust R20 and R10+R11.
Increasing their value increases the t_R/t_F values and decrease the overshoot

3 To adjust L1
Increasing L1 speeds up the device and increases the overshoot.

We recommend our customers to use the schematic shown on Figure 5 as a starting point for the video board design and then to apply the optimization they need.

9 - POWER DISSIPATION

The total power dissipation is the sum of the static DC and the dynamic dissipation:

$P_{TOT} = P_{STAT} + P_{DYN}$.

The static DC power dissipation is approximately:

$P_{STAT} = V_{DD} \times I_{DD} + V_{CC} \times I_{CC}$

The dynamic dissipation is, in the worst case (1 pixel On/ 1 pixel Off pattern):

$P_{DYN} = 3\ V_{DD} \times C_L \times V_{OUT(PP)} \times f \times K$

where f is the video frequency and K the ratio between the active line and the total horizontal line duration.

Example:

for V_{DD} = 110V, V_{CC} = 12V,
I_{DD} = 25mA, I_{CC} = 60mA,
V_{OUT} = 40 V_{PP}, f = 40MHz,
C_L = 8pF and K = 0.72.

We have:

P_{STAT} = 3.47W, P_{DYN} = 3.04W

Therefore:

P_{TOT} = 6.51W.

Note 5: This worst thermal case must only be considered for TJmax calculation. Nevertheless, during the average life of the circuit, the conditions are closer to the white picture conditions.

10 - TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD}=110V, V_{CC}=12V, C_L=8pF, R_P=300Ω, ΔV=40V_{PP}, unless otherwise specified - see Figure 1

Figure 6. TDA9533 pulse response

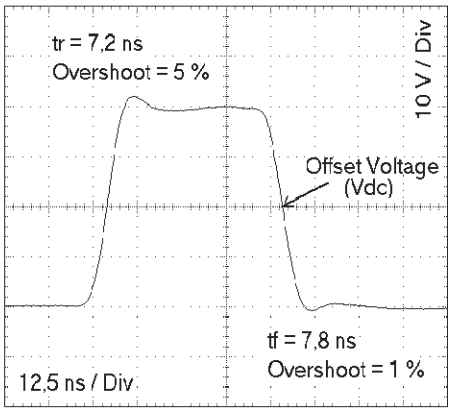


Figure 7. V_{OUT} versus V_{IN}

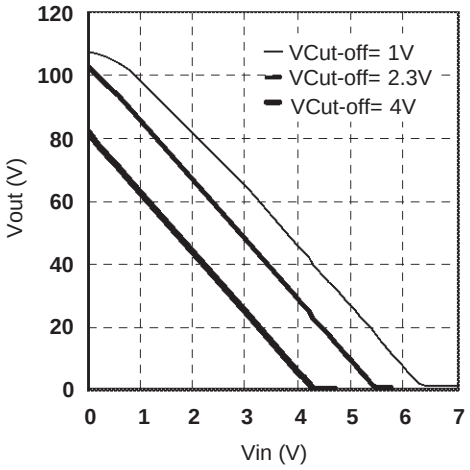


Figure 8. Power dissipation versus frequency

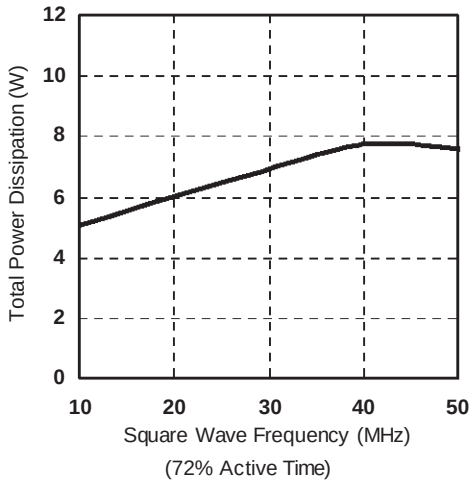


Figure 9. Speed versus temperature

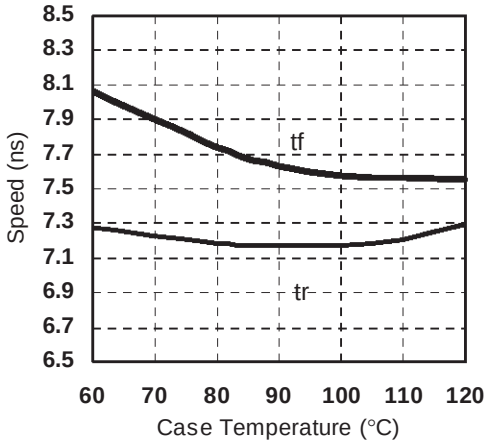


Figure 10. Speed versus offset

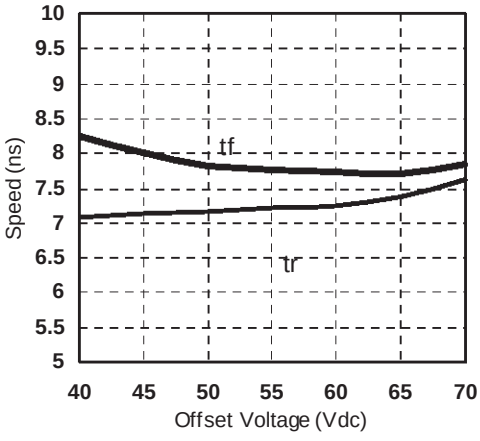


Figure 11. Speed versus load capacitance

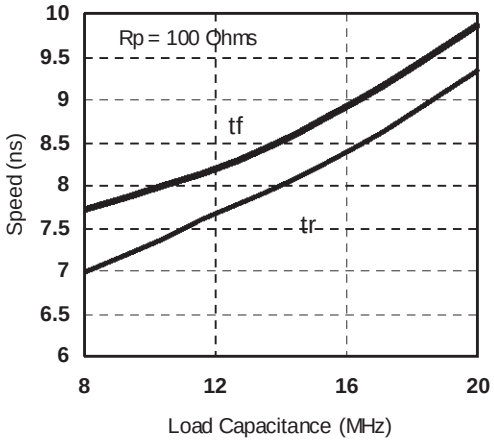


Figure 12. TDA9207/9209 - TDA9533/9530 Demonstration Board: Silk Screen and Trace (scale 1:1)

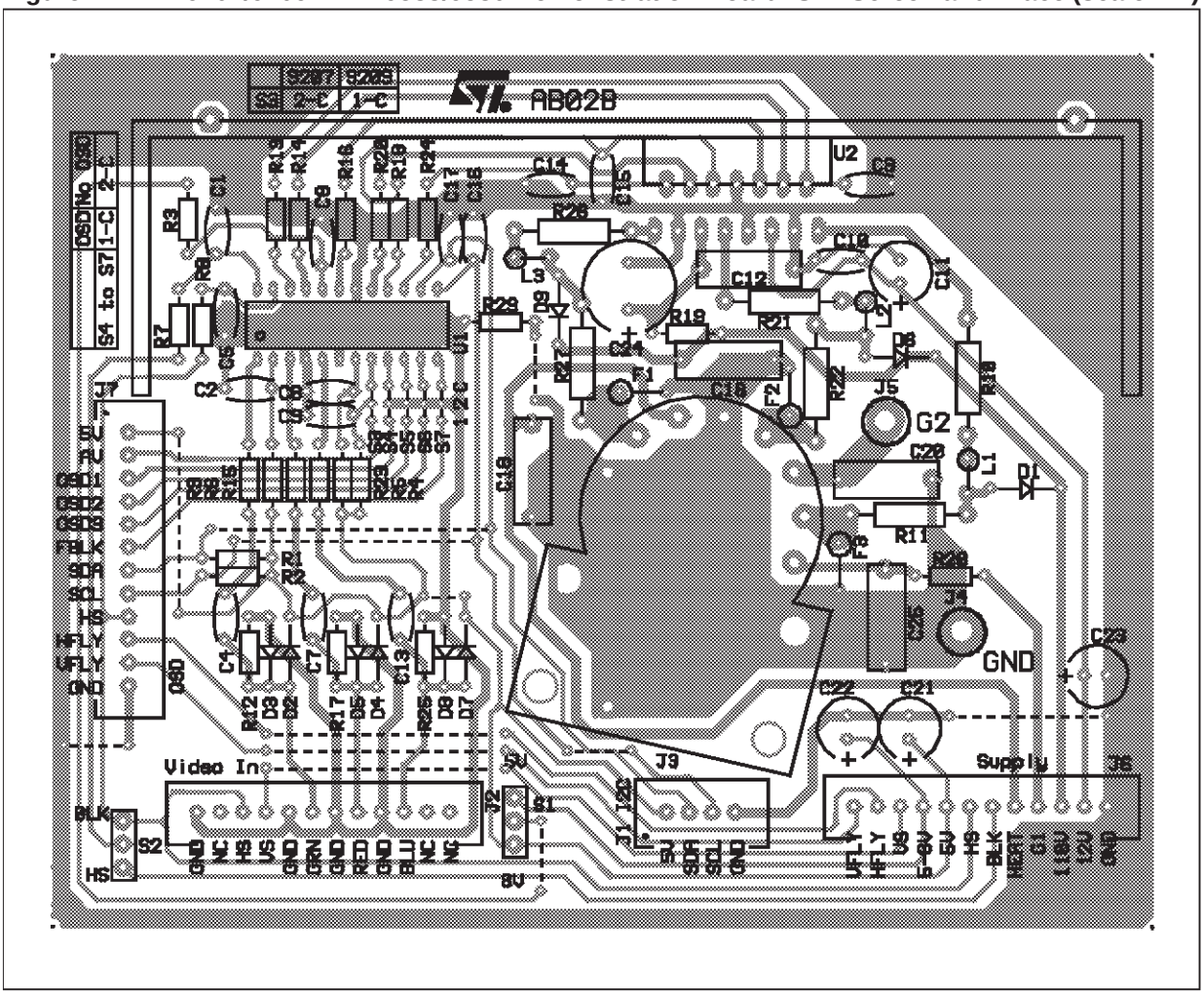
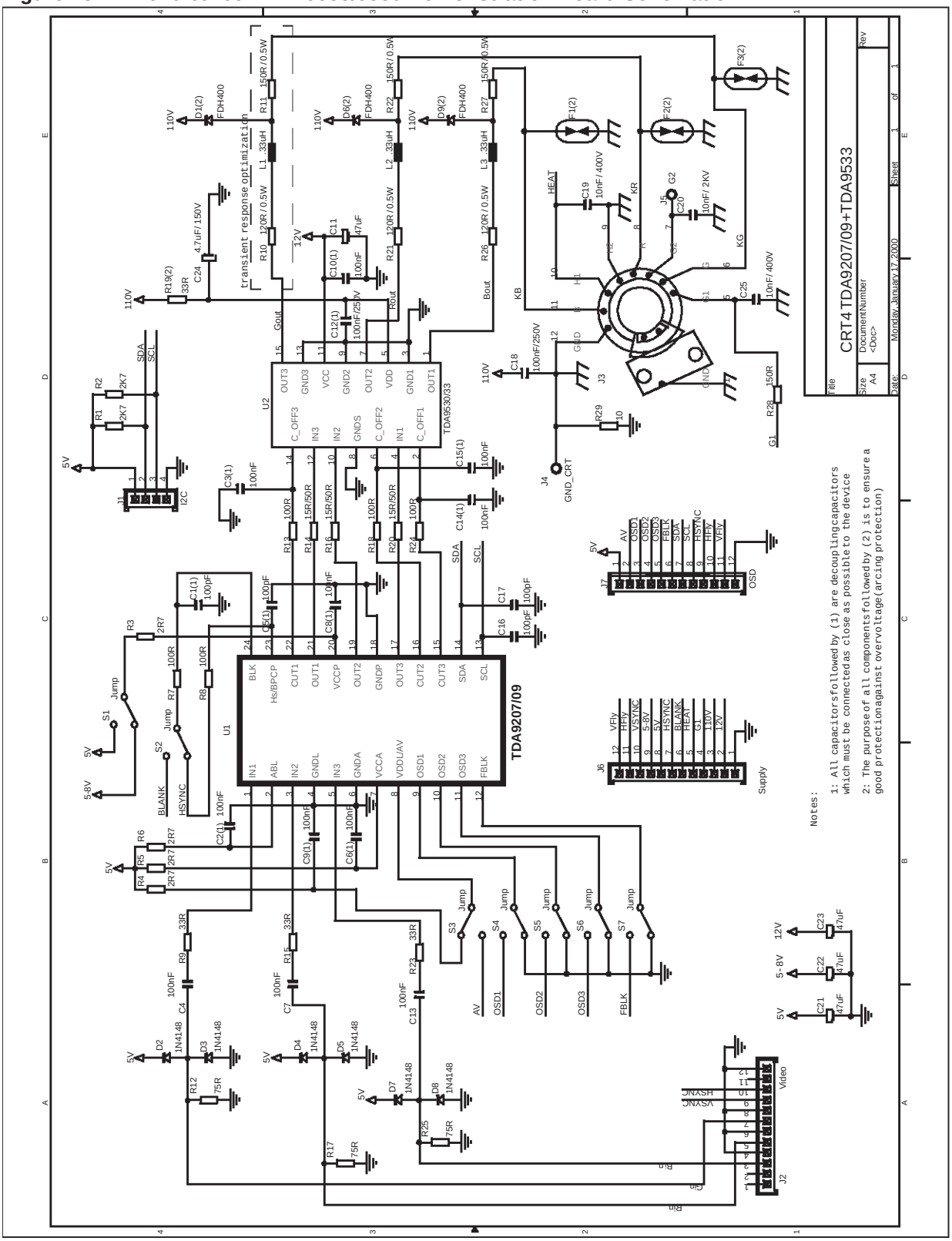
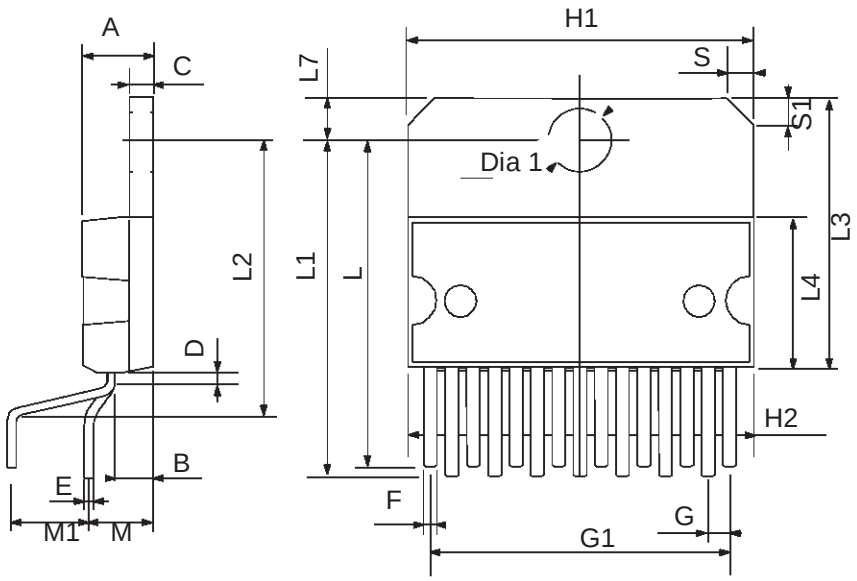


Figure 13. TDA9207/9209 - TDA9533/9530 Demonstration Board Schematic



11 - PACKAGE MECHANICAL DATA

15 PIN - PLASTIC MULTIWATT



Dimensions	Millimetres			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
D		1			0.039	
E	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.02	1.27	1.52	0.040	0.050	0.060
G1	17.53	17.78	18.03	0.690	0.700	0.710
H1	19.6			0.772		
H2			20.2			0.795
L	21.9	22.2	22.5	0.862	0.874	0.886
L1	21.7	22.1	22.5	0.854	0.870	0.886
L2	17.65		18.1	0.695		0.713
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
M	4.25	4.55	4.85	0.167	0.179	0.191
M1	4.63	5.08	5.53	0.182	0.200	0.218
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia. 1	3.65		3.85	0.144		0.152

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