DATA SHEET

TEA1202TS
0.95 V starting power unit

Preliminary specification
Supersedes data of 2000 Jun 08

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Philips
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CONTENTS

1 FEATURES

- Fully integrated battery power unit, including complete DC-to-DC converter circuit, two Low Drop-Out voltage regulators (LDOs) and a battery low detector
- Configurable for 1, 2 or 3-cell Nickel-Cadmium (NiCd) or Nickel Metal Hybrid (NiMH) batteries and 1 Lithium Ion (Li-Ion) battery
- Guaranteed DC-to-DC converter start-up from 1-cell NiCd or NiMH battery, even with a load current
- Upconversion or downconversion
- Internal power MOSFETs featuring a low R_{DSon} of approximately 0.1 Ω
- Synchronous rectification for high efficiency
- Soft start
- PWM-only operating option
- LDO drop-out voltage of 30 mV at 50 mA
- Both LDOs can also be used as low-ohmic power switches
- Stable LDO performance with ceramic capacitors
- At start-up, LDO1 can be loaded
- Stand-alone low battery detector requires no additional supply voltage
- Low battery detection level at 0.90 V, externally adjustable to a higher level
- Adjustable output voltages
- Shut-down function
- Small outline package
- Advanced 0.6 μm BICMOS process.

2 APPLICATIONS

- Cellular phones
- Cordless phones
- Personal Digital Assistants (PDAs)
- Portable audio players
- Pagers
- Mobile equipment.

3 GENERAL DESCRIPTION

The TEA1202TS is a fully integrated battery power unit including a high efficiency DC-to-DC converter which runs from a single-cell NiCd or NiMH battery, two low drop-out voltage regulators and a low battery detector. The circuit can be arranged in many ways to optimize the application circuit of a power supply system. Therefore, most inputs and outputs are separated, the DC-to-DC converter can be arranged for upconversion or downconversion and the regulators can also be used as power switches. One regulator can be used completely independent of the rest of the system, and the low battery detector can be configured for several types of batteries. Accurate low battery detection is possible while all other blocks are switched off.

The DC-to-DC converter features efficient, compact and dynamic power conversion using a digital control concept comparable with Pulse Width Modulation (PWM) and Pulse Frequency Modulation (PFM), integrated CMOS power switches with a very low R_{DSon} and fully synchronous rectification.

The device operates at a switching frequency of 600 kHz which enables the use of external components with minimum size. The switching frequency can be synchronized to an external high frequency clock signal. Optionally, the device can be kept in PWM control mode only. Deadlock is prevented by an on-chip undervoltage lockout circuit.

Active current limiting enables efficient conversion in pulsed-load systems such as Global System for Mobile communication (GSM) and Digital Enhanced Cordless Telecommunications (DECT).

Both LDOs show a low drop-out voltage and are inherently stable, even when ceramic capacitors with a low ESR value are applied at the outputs. Usage of the LDOs as low-ohmic switches is also possible.

LDO1 can be loaded at start-up.

The low battery detector has a built-in detection level which is optimum for a single-cell NiCd or NiMH battery. Higher battery voltages can be translated to this single-cell level by an additional built-in LDO circuit.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1202TS	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

5 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC-to-DC converter						
UPCONVERSION						
$V_{I(up)}$	input voltage		$V_{I(start)}$	–	5.50	V
$V_{O(up)}$	output voltage		$V_{O(uvlo)}$	–	5.50	V
$V_{I(start)}$	start-up input voltage	I_L < 10 mA	0.93	0.96	1.00	V
$V_{O(uvlo)}$	undervoltage lockout voltage	note 1	2.0	2.2	2.4	V
DOWNCONVERSION						
$V_{I(dwn)}$	input voltage		$V_{O(uvlo)}$	–	5.50	V
$V_{O(dwn)}$	output voltage		1.30	–	5.50	V
CURRENT LEVELS						
$I_{q(DCDC)}$	quiescent current at pin UPOUT/DNIN		–	110	–	µA
I_{shdwn}	current in shut-down mode	$V_{LBI1} = V_{I(up)} = 1.2$ V	–	65	–	µA
$I_{LX(max)}$	maximum continuous current at pins LX1 and LX2	T_{amb} = 80 °C	–	–	1.0	A
ΔI_{lim}	current limit deviation	I_{lim} set to 1.0 A				
		upconversion	–12	–	+12	%
		downconversion	–12	–	+12	%
POWER MOSFETS						
$R_{DSon(N)}$	drain-to-source on-state resistance	NFET; I_{DS} = 100 mA; T_j = 27 °C	–	110	200	mΩ
$R_{DSon(P)}$	drain-to-source on-state resistance	PFET; I_{DS} = –100 mA; T_j = 27 °C	–	125	250	mΩ
EFFICIENCY						
η	efficiency upconversion	see Fig.10; V_O up to 3.3 V				
		V_I = 1.2 V; I_L = 100 mA	–	84	–	%
		V_I = 2.4 V; I_L = 200 mA	–	92	–	%
TIMING						
f_{sw}	switching frequency	PWM mode	480	600	720	kHz
$f_{i(sync)}$	synchronization clock input frequency		6	13	20	MHz
t_{start}	start-up time		–	10	–	ms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Low drop-out voltage regulators						
V_{LDO}	output voltage range	$V_{LDO} < V_4 + 0.3$ V	1.30	–	5.50	V
$V_{dropout}$	drop-out voltage	$I_{LDO} = 50$ mA	–	30	45	mV
I_{LDO}	output current	in regulation	–	–	250	mA
$R_{DSon(LDO1)}$	LDO1 drain-to-source on-state resistance	$V_{I(LDO1)} = 5$ V; $V_{FB1} < 0.4$ V; $I_{LDO1} = 50$ mA	–	500	750	mΩ
General characteristics						
V_{ref}	reference voltage		1.165	1.190	1.215	V

Note

1. The undervoltage lockout level shows wide specification limits since it decreases at increasing temperature. When the temperature increases, the minimum supply voltage of the digital control part of the IC decreases and therefore the correct operation of this function is guaranteed over the whole temperature range. The undervoltage lockout level is measured at pin UPOUT/DNIN.

6 BLOCK DIAGRAM

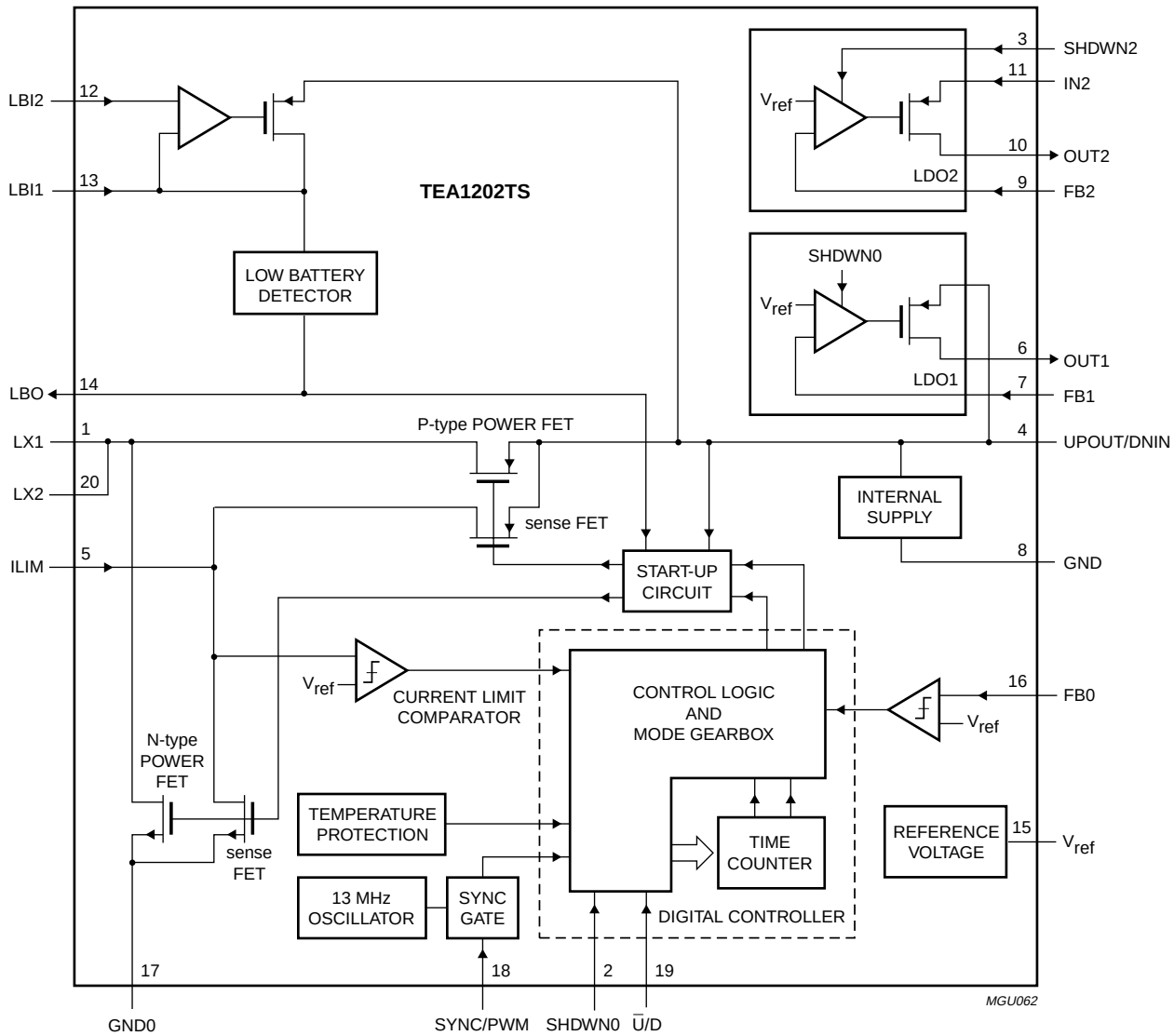


Fig.1 Block diagram.

7 PINNING

SYMBOL	PIN	DESCRIPTION
LX1	1	inductor connection 1
SHDWN0	2	DC-to-DC shut-down input
SHDWN2	3	LDO2 shut-down input
UPOUT/DNIN	4	up mode DC-to-DC output; down mode DC-to-DC input
ILIM	5	current limiting resistor connection
OUT1	6	LDO1 output
FB1	7	LDO1 feedback input
GND	8	internal supply ground
FB2	9	LDO2 feedback input
OUT2	10	LDO2 output
IN2	11	LDO2 input
LBI2	12	low battery detector input 2
LBI1	13	low battery detector input 1
LBO	14	low battery detector output
V_{ref}	15	reference voltage
FB0	16	DC-to-DC feedback input
GND0	17	DC-to-DC converter ground
SYNC/PWM	18	synchronization clock input or PWM-only selection input
$\overline{U}$/D	19	conversion mode selection input
LX2	20	inductor connection 2

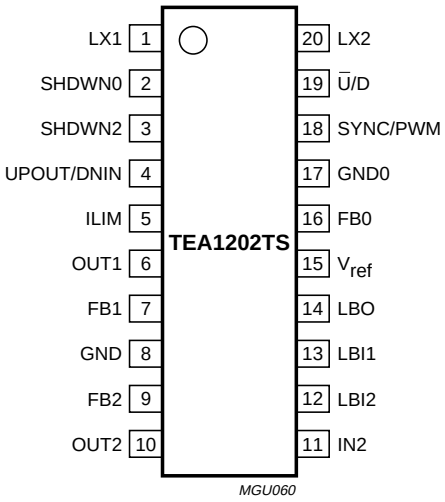


Fig.2 Pin configuration.

8 FUNCTIONAL DESCRIPTION

8.1 Control mechanism

The DC-to-DC converter of the TEA1202TS is able to operate in PFM (discontinuous conduction) or PWM (continuous conduction) operating mode. All switching actions are completely determined by a digital control circuit which uses the output voltage level as its control input. This novel digital approach enables the use of a new pulse width and frequency modulation scheme, which ensures optimum power efficiency over the complete range of operation of the converter.

When high output power is requested, the device will operate in PWM (continuous conduction) operating mode. This results in minimum AC currents in the circuit components and hence optimum efficiency, minimum costs and low EMC. In this operating mode, the output voltage is allowed to vary between two predefined voltage levels. As long as the output voltage stays within this so-called window, switching continues in a fixed pattern.

When the output voltage reaches one of the window borders, the digital controller immediately reacts by adjusting the pulse width and inserting a current step in such a way that the output voltage stays within the window with higher or lower current capability. This approach enables very fast reaction to load variations. Figure 3 shows the response of the converter to a sudden load increase. The upper trace shows the output voltage.

The ripple on top of the DC level is a result of the current in the output capacitor, which changes in sign twice per cycle, times the internal Equivalent Series Resistance (ESR) of the capacitor. After each ramp-down of the inductor current, i.e. when the ESR effect increases the output voltage, the converter determines what to do in the next cycle. As soon as more load current is taken from the output the output voltage starts to decay.

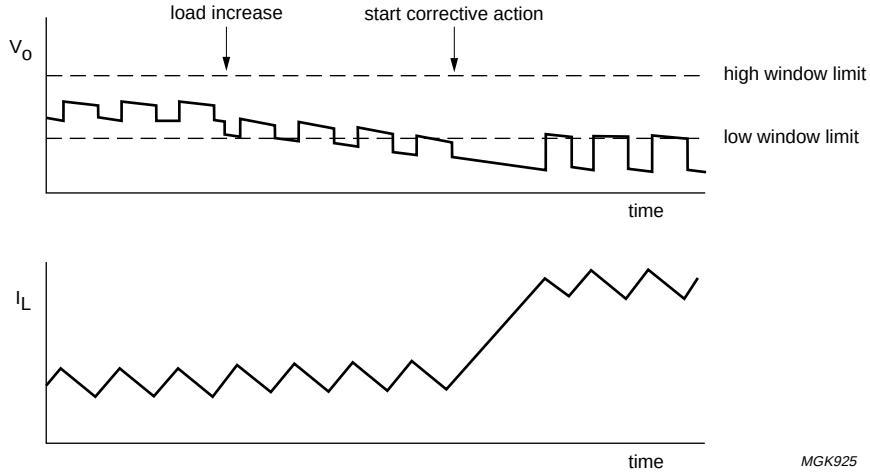


Fig.3 Response to load increase.

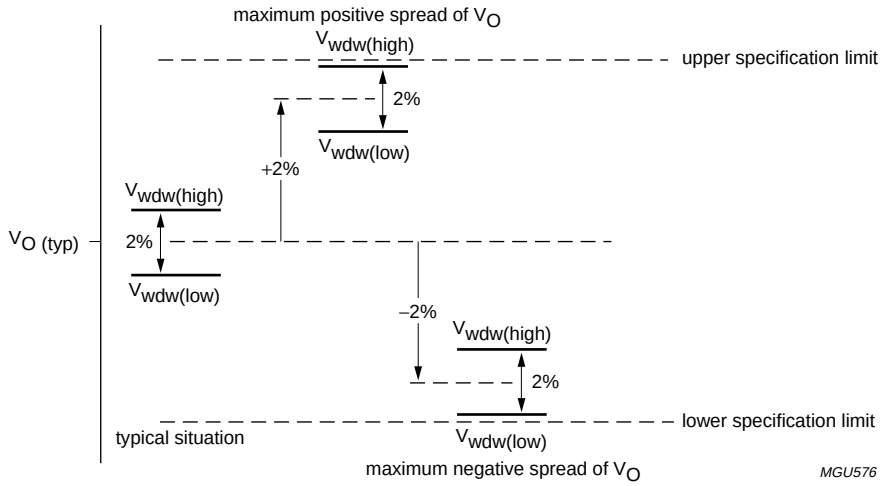


Fig.4 Output voltage window spread.

When the output voltage becomes lower than the low limit of the window, a corrective action is taken by a ramp-up of the inductor current during a much longer time. As a result, the DC current level is increased and normal PWM control can continue. The output voltage (including ESR effect) is again within the predefined window.

Figure 4 shows the spread of the output voltage window. The absolute value is mostly dependent on spread, while the actual window size [$V_{wdw(high)} - V_{wdw(low)}$] is not affected. For one specific device, the output voltage will not vary more than 2% (typical value).

In low output power situations, the TEA1202TS will switch over to PFM (discontinuous conduction) operating mode. In this mode, regulation information from an earlier PWM operating mode is used. This results in optimum inductor peak current levels in the PFM mode, which are slightly larger than the inductor ripple current in the PWM mode. As a result, the transition between PFM and PWM mode is optimum under all circumstances. In the PFM mode the TEA1202TS regulates the output voltage to the high window limit as shown in Fig.3.

8.2 Synchronous rectification

For optimum efficiency over the whole load range, synchronous rectifiers inside the TEA1202TS ensure that during the whole second switching phase, all inductor current will flow through the low-ohmic power MOSFETs. Special circuitry is included which detects when the inductor current reaches zero. Following this detection, the digital controller switches off the power MOSFET and proceeds with regulation.

8.3 Start-up

Start-up from low input voltage in the boost mode is realized by an independent start-up oscillator, which starts switching the N-type power MOSFET as soon as the low-battery detector detects a sufficiently high voltage. The inductor current is limited internally to ensure soft-starting. The switch actions of the start-up oscillator will increase the output voltage. As soon as the output voltage is high enough for normal regulation, the digital control system takes control over the power MOSFETs.

8.4 Undervoltage lockout

As a result of too high a load or disconnection of the input power source, the output voltage can drop so low that normal regulation cannot be guaranteed. In this event, the device switches back to start-up mode. If the output voltage drops even further, switching is stopped completely.

8.5 Shut-down

When the shut-down input is set HIGH, the DC-to-DC converter disables both switches and power consumption is reduced to a few microamperes.

8.6 Power switches

The power switches in the IC are one N-type and one P-type power MOSFET, both having a typical drain-to-source resistance of 100 mΩ. The maximum continuous current in the power switches is 1.0 A at T_{amb} = 80 °C.

8.7 Temperature protection

When the DC-to-DC converter operates in the PWM mode, and the die temperature gets too high (typical value is 160 °C), the converter and both LDOs stop operating. They resume operation when the die temperature falls below 90 °C again. As a result, low frequency cycling between the on and off state will occur. It should be noted that in the event of device temperatures at the cut-off limit, the application differs strongly from maximum specifications.

8.8 Current limiters

If the current in one of the power switches exceeds the programmed limit in the PWM mode, the current ramp is stopped immediately and the next switching phase is entered. Current limiting is required to keep power conversion efficient during temporary high loads. Furthermore, current limiting protects the IC against overload conditions, inductor saturation, etc.

The current limiting level is set by an external resistor which must be connected between pin ILIM and ground for downconversion, or between pins ILIM and UPOUT/DNIN for upconversion.

8.9 External synchronization and PWM-only mode

If an external high-frequency clock or a HIGH level is applied to pin SYNC/PWM, the TEA1202TS will use PWM regulation independent of the load applied.

In the event a high-frequency clock is applied, the switching frequency in the PWM mode will be exactly that frequency divided by 22. In the PWM mode the quiescent current of the device increases.

In the event that no external synchronization or PWM mode selection is necessary, pin SYNC/PWM must be connected to ground.

8.10 Behaviour at input voltage exceeding the specified range

In general, an input voltage exceeding the specified range is not recommended since instability may occur. There are two exceptions:

- Upconversion: at an input voltage higher than the target output voltage, but up to 5.5 V, the converter will stop switching and the external Schottky diode will take over. The output voltage will equal the input voltage minus the diode voltage drop. Since all current flows through the external diode in this situation, the current limiting function is not active.

  In the PWM mode, the P-type power MOSFET is always on when the input voltage exceeds the target output voltage. The internal synchronous rectifier ensures that the inductor current does not fall below zero. As a result, the achieved efficiency is higher in this situation than standard PWM-controlled converters achieve.
- Downconversion: when the input voltage is lower than the target output voltage, but higher than 2.2 V, the P-type power MOSFET will stay conducting resulting in an output voltage being equal to the input voltage minus some resistive voltage drop. The current limiting function remains active.

8.11 Low drop-out voltage regulators

The low drop-out voltage regulators are functionally equal apart from the shut-down mechanism: LDO2 can be controlled separately by pin SHDWN2, while LDO1 is controlled by pin SHDWN0 like the DC-to-DC converter.

The input voltage of each LDO must be 250 mV (at I_{LDO} = 50 mA) higher than its output voltage to achieve full specification on e.g. ripple rejection. However, the parts will function like an LDO down to a margin of 45 mV (at I_{LDO} = 50 mA) between input and output: the so-called drop-out voltage. At a lower margin between input and output, the LDOs will behave like a resistor.

Both LDOs are protected from high temperature (see Section 8.7).

Next to normal LDO functions, both regulators can be switched off or can be used as switches. Each regulator will act as a low-ohmic switch in the on-state when its feedback input is connected to ground. When the feedback input is higher than 2 V, the regulator will make its power FET high-ohmic. So the feedback inputs of the regulators can be used as digital inputs which make the LDOs behave as switches.

8.12 Low battery detector

The low battery detector is an autonomous circuit which can work at an input voltage down to 0.90 V. It is always on, even when all other blocks are in the shut-down mode.

The detector has two inputs: the input on pin LBI1 is tuned to accept a single-cell NiCd or NiMH battery voltage directly, while the input on pin LBI2 can detect a two-cell NiCd or NiMH battery voltage or higher voltage. The detection level of the input on pin LBI2 can be set by using a voltage divider between the battery voltage, pin LBI2 and ground. Hysteresis is included for proper operating. Furthermore, a capacitor of 10 nF (typical value) must be connected between pin LBI1 and ground when the input on pin LBI2 is used.

The output of the low battery detector on pin LBO is an open-collector output. The output is high (i.e. no current is sunk by the collector) when the input voltage of the detector is below the lower detection level.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_n	voltage on any pin	shut-down mode	–0.2	+6.5	V
		operating mode	–0.2	+5.5	V
T_j	junction temperature		–40	+150	°C
T_{amb}	ambient temperature		–20	+80	°C
T_{stg}	storage temperature		–40	+125	°C
V_{es}	electrostatic handling voltage	notes 1 and 2	Class II		V

Notes

1. ESD specification is in accordance with the JEDEC standard:
   a) Human Body Model (HBM) tests are carried out by discharging a 100 pF capacitor through a 1.5 kΩ series resistor.
   b) Machine Model (MM) tests are carried out by discharging a 200 pF capacitor via a 0.75 μH series inductor.
2. Exception is pin ILIM: 1000 V HBM.

10 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	140	K/W

11 QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611D"*.

12 CHARACTERISTICS

T_{amb} = –20 to +80 °C; all voltages are measured with respect to ground; positive currents flow into the IC; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC-to-DC converter						
UPCONVERSION; pin $\overline{U}$/D = LOW						
$V_{I(up)}$	input voltage		$V_{I(start)}$	–	5.50	V
$V_{O(up)}$	output voltage		$V_{O(uvlo)}$	–	5.50	V
$V_{I(start)}$	start-up input voltage	I_L < 10 mA	0.93	0.96	1.00	V
$V_{O(uvlo)}$	undervoltage lockout voltage	note 1	2.0	2.2	2.4	V
DOWNCONVERSION; pin $\overline{U}$/D = HIGH						
$V_{I(dwn)}$	input voltage	note 2	$V_{O(uvlo)}$	–	5.50	V
$V_{O(dwn)}$	output voltage		1.30	–	5.50	V
REGULATION						
$\Delta V_{O(wdw)}$	output voltage window size as a function of output voltage	PWM mode	1.5	2.0	2.5	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CURRENT LEVELS						
$I_{q(DCDC)}$	quiescent current at pin UPOUT/DNIN	note 3	–	110	–	μA
I_{shdwn}	current in shut-down mode	$V_{LBI1} = V_{l(up)} = 1.2$ V	–	65	–	μA
$I_{lim(max)}$	maximum current limit		–	5	–	A
ΔI_{lim}	current limit deviation	I_{lim} set to 1.0 A; note 4				
		upconversion	–12	–	+12	%
		downconversion	–12	–	+12	%
$I_{LX(max)}$	maximum continuous current at pins LX1 and LX2	T_{amb} = 80 °C	–	–	1.0	A
POWER MOSFETS						
$R_{DS(on)(N)}$	drain-to-source on-state resistance	NFET; I_{DS} = 100 mA; T_j = 27 °C	–	110	200	mΩ
$R_{DS(on)(P)}$	drain-to-source on-state resistance	PFET; I_{DS} = –100 mA; T_j = 27 °C	–	125	250	mΩ
EFFICIENCY						
η	efficiency upconversion	see Fig.10; V_O up to 3.3 V				
		V_I = 1.2 V; I_L = 100 mA	–	84	–	%
		V_I = 2.4 V; I_L = 200 mA	–	92	–	%
TIMING						
f_{sw}	switching frequency	PWM mode	480	600	720	kHz
$f_{i(sync)}$	synchronization clock input frequency		6	13	20	MHz
t_{start}	start-up time	note 6	–	10	–	ms
DIGITAL INPUT LEVELS						
$V_{IL(n)}$	LOW-level input voltage on all digital pins		0	–	0.4	V
$V_{IH(n)}$	HIGH-level input voltage	note 7				
	pin SYNC/PWM		$0.55V_4$	–	V_4 + 0.3	V
	pins SHDWN0 and SHDWN2		0.9	–	V_4 + 0.3	V
	all other digital input pins		V_4 – 0.4	–	V_4 + 0.3	V
Low drop-out voltage regulators; note 8						
$V_{I(LDO1)}$	output voltage range pin LDO1		$V_{O(uvlo)}$	–	5.50	V
$V_{I(LDO2)}$	output voltage range pin LDO2		1.8	–	V_4 + 0.3	V
V_{LDO}	output voltage range	$V_{LDO} < V_4$ + 0.3 V	1.30	–	5.50	V
$V_{dropout}$	drop-out voltage	note 9				
		I_{LDO} = 50 mA	–	30	45	mV
		I_{LDO} = 150 mA	–	90	135	mV
V_{drop}	minimum drop voltage for functionality within specification	I_{LDO} = 50 mA	250	–	–	mV
		I_{LDO} = 150 mA	500	–	–	mV

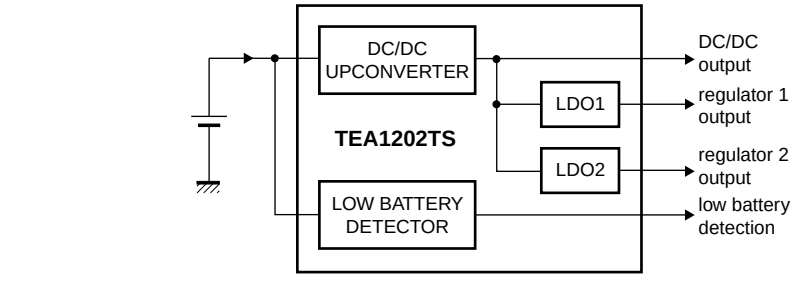
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{LDO}	output current	in regulation	–	–	250	mA
ΔV_{LDO}	output voltage accuracy	$V_I - V_{LDO}$ = 1 V; I_{LDO} = 1 mA; note 10	–3.5	–	+3.5	%
ΔV_{line}	line voltage regulation	1 mA < I_{LDO} < 150 mA; note 11				
		$(V_I - V_{LDO}) > V_{drop} < 4.5$ V	–	–	0.1	%/V
		4.5 V < $(V_I - V_{LDO})$ < 5.5 V	–	–	0.2	%/V
ΔV_{load}	load voltage regulation with changing load current	10 mA < I_{LDO} < 150 mA; note 12	–	–	–0.02	%/mA
PSRR	power supply ripple rejection	note 13	–	40	–	dB
$t_{res(up)}$	response time after a positive load step	I_O = 0.5 mA to 50 mA; C_L = 2.2 µF; $V_{O(error)}$ < ±0.1% of end value	–	–	20	µs
$t_{res(down)}$	response time after a negative load step	I_O = 50 mA to 0.5 mA; C_L = 2.2 µF; $V_{O(error)}$ < ±0.1% of end value	–	–	100	µs
$I_{q(LDO)}$	quiescent current		–	50	–	µA
$I_{shdwn(LDO)}$	shut-down current		–	–	1	µA
SWITCH CIRCUIT						
$R_{DS(on)(LD01)}$	LD01 drain-to-source resistance	LD01 in switched-on state; $V_{I(LDO1)}$ = 5 V; V_{FB1} < 0.4 V	–	500	750	mΩ
$R_{DS(on)(LD02)}$	LD02 drain-to-source resistance	LD02 in switched-on state; $V_{I(LDO2)}$ = 5 V; V_{FB2} < 0.4 V	–	300	450	mΩ
$I_{O(max)(LDO1)}$	LDO1 maximum output current	LDO1 in switched-on state; V_{FB1} > 0.4 V	–	–	0.40	A
$I_{O(max)(LDO2)}$	LDO2 maximum output current	LDO2 in switched-on state; V_{FB2} > 0.4 V	–	–	0.40	A
Low battery detector						
$t_{t(HL)}$	transition time	falling V_{bat}	–	2	–	µs
DETECTION INPUT PIN LBI1						
V_{det}	low battery detection level	falling V_{bat}	0.87	0.90	0.93	V
V_{hys}	low battery detection hysteresis		–	20	–	mV
TC_{Vdet}	temperature coefficient of detection level		–	0	–	mV/K
TC_{Vhys}	temperature coefficient of detection hysteresis		–	0.175	–	mV/K
DETECTION OUTPUT PIN LB0						
$I_{O(sink)}$	output sink current		15	–	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
General characteristics						
V_{ref}	reference voltage		1.165	1.190	1.215	V
I_q	quiescent current at pin UPOUT/DNIN	all blocks operating	–	270	–	μA
T_{amb}	ambient temperature		–20	+25	+80	°C
T_{max}	internal temperature for cut-off		150	160	170	°C

Notes

1. The undervoltage lockout level shows wide specification limits since it decreases at increasing temperature. When the temperature increases, the minimum supply voltage of the digital control part of the IC decreases and therefore the correct operation of this function is guaranteed over the whole temperature range. The undervoltage lockout level is measured at pin UPOUT/DNIN.
2. When $V_{I(dwn)}$ is lower than the target output voltage but higher than 2.2 V, the P-type power MOSFET will remain conducting (duty factor is 100%), resulting in $V_{O(dwn)}$ following $V_{I(dwn)}$.
3. The quiescent current is specified as the current in to pin UPOUT/DNIN (pin 4) in the upconversion configuration at V_I = 1.20 V and V_O = 3.30 V, using L1 = 6.8 μH, R1 = 150 kΩ and R2 = 91 kΩ.
4. The current limit is defined by resistor R10. This resistor must have 1% accuracy.
5. The specified efficiency is valid when using an output capacitor having an ESR of 0.1 Ω and an inductor of 6.8 μH with an ESR of 0.05 Ω and a sufficient saturation current level.
6. The specified start-up time is the time between the connection of a 1.20 V input voltage source and the moment the output reaches 3.30 V. The output capacitance equals 100 μF, the inductance equals 6.8 μH and no load is present.
7. V_4 is the voltage at pin UPOUT/DNIN. If the applied HIGH-level voltage is less than V_4 – 1 V, the quiescent current of the device will increase.
8. Take care regarding total dissipation if output current I_{LDO} > 50 mA and drop voltage V_{drop} > 2 V.
9. The drop-out voltage is defined as the voltage between the input and the output of the LDO when the output voltage has dropped 100 mV below its nominal value. The drop-out voltage is measured while the LDO input voltage is decreasing.
10. The output voltage of each LDO is defined by external feedback resistors. These resistors must have 1% accuracy.
11. $\Delta V_{line} = \frac{\Delta V_{LDO}}{V_{LDO} \times \Delta V_I} \times 100$ %/V.
12. $\Delta V_{load} = \frac{\Delta V_{LDO}}{V_{LDO} \times \Delta I_{LDO}} \times 100$ %/mA.
13. Measured with a sine wave at f_i = 100 Hz to 1 MHz, V_i = 100 mV (RMS), C_L = 2.2 μF and I_{LDO} = 10 mA.

13 APPLICATION INFORMATION



equivalent block diagram

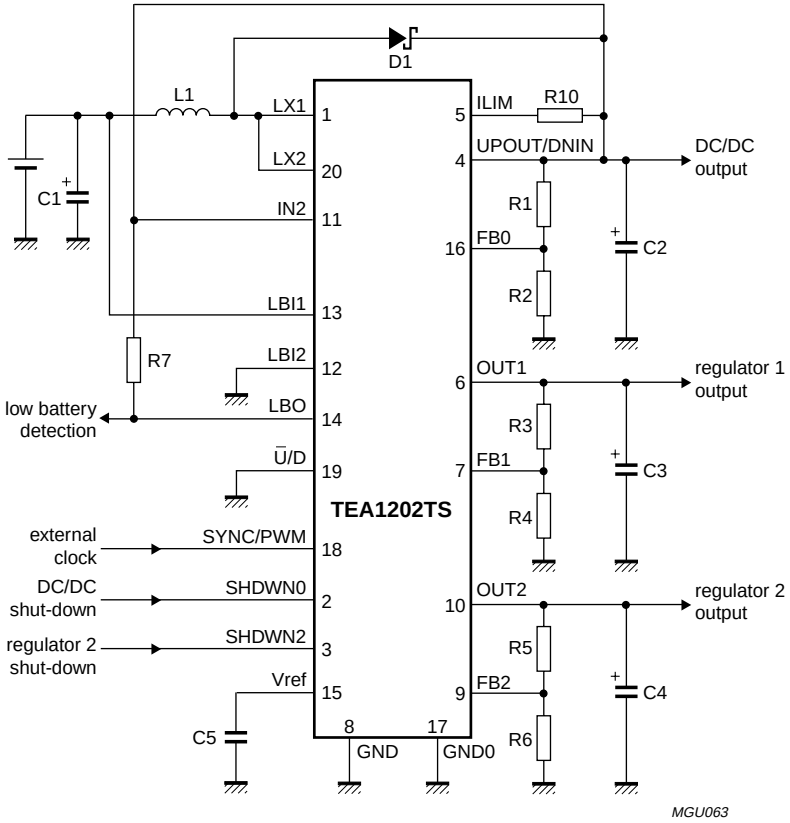
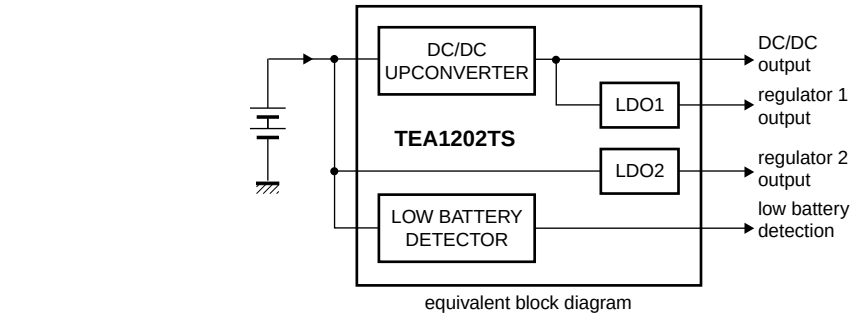


Fig.5 Application in single-cell NiCd or NiMH battery powered equipment.



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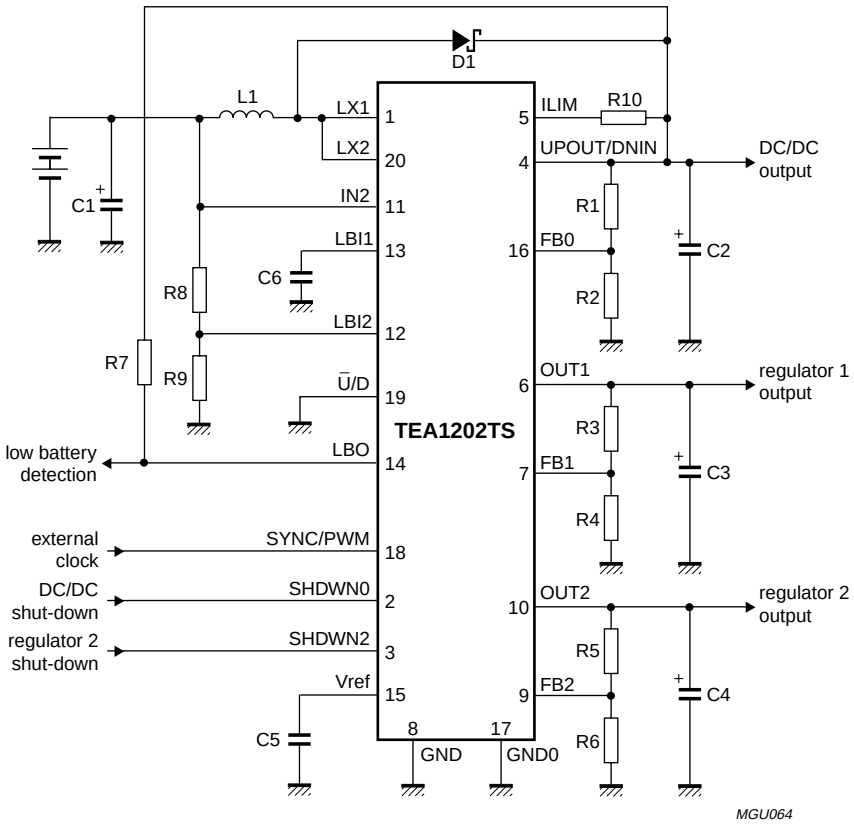


Fig.6 Application in two-cell NiCd or NiMH battery powered equipment.

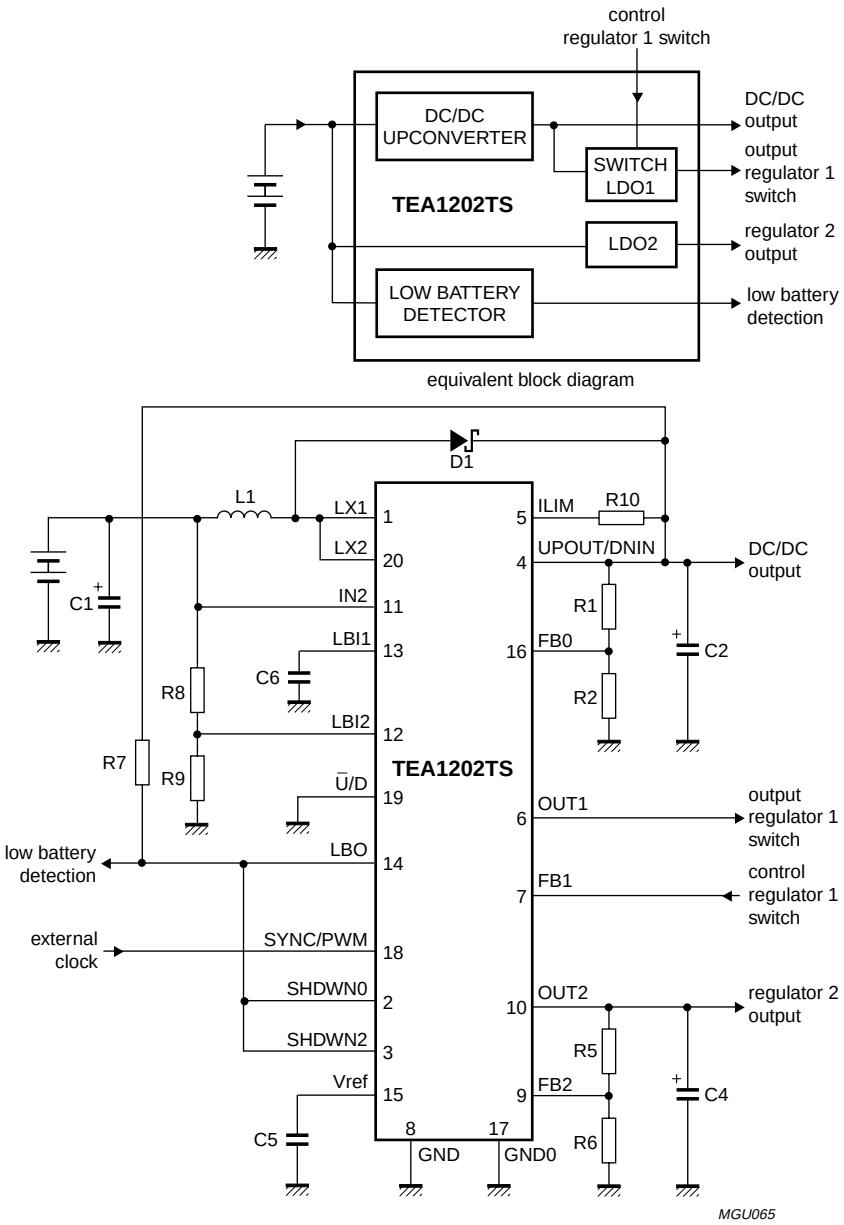
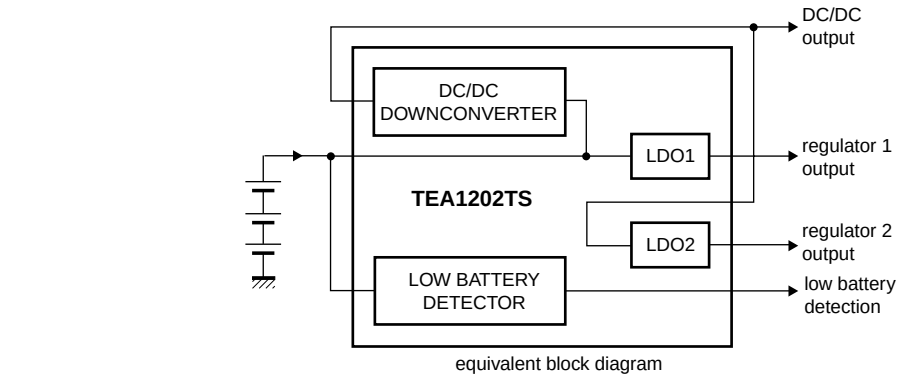


Fig.7 Application in two-cell NiCd or NiMH battery powered equipment with autonomous shut-down at low battery voltage and using LDO1 as a switch.



equivalent block diagram

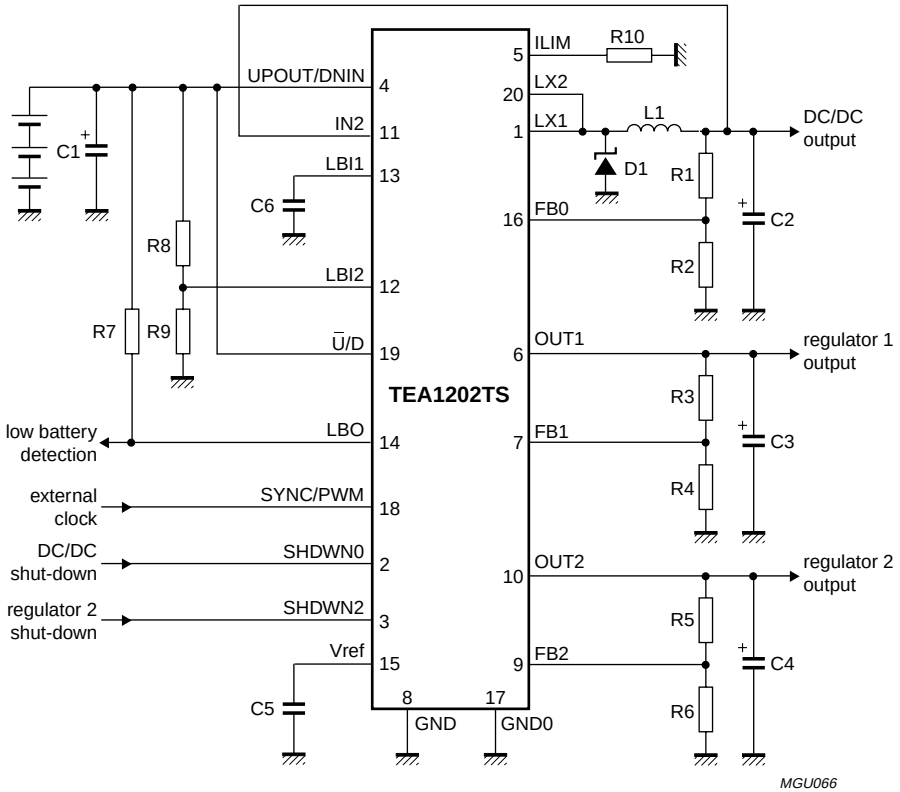


Fig.8 Application in three-cell NiCd or NiMH and single-cell Li-Ion battery powered equipment.

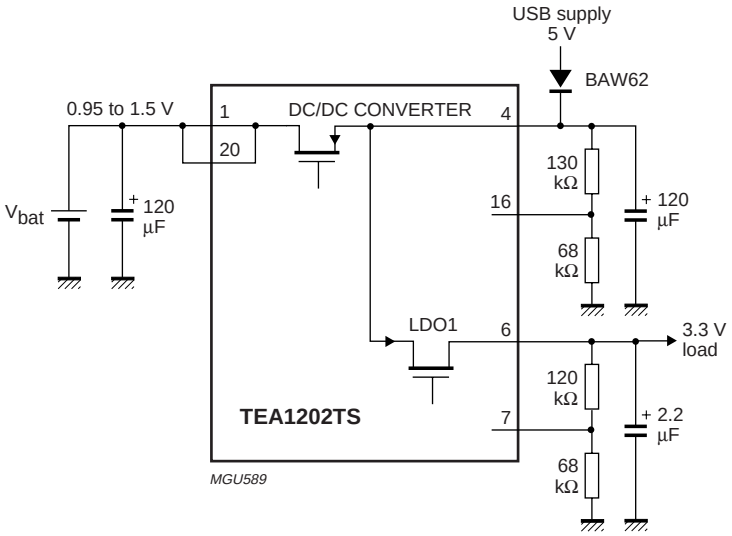


Fig.9 Application with USB and single-cell NiCd or NiMH battery supply.

13.1 External component selection

Component references apply to the circuits shown in Figs 5 to 8.

13.1.1 Inductor L1

The performance of the TEA1202TS is not very sensitive to inductance value. The best efficiency performance over a wide load current range is achieved by using an inductance of 6.8 µH, for example TDK SLF7032 or Coilcraft DO1608 range.

13.1.2 DC-to-DC input capacitor C1

The value of C1 depends strongly on the type of input source. In general, a 100 µF tantalum capacitor is sufficient.

13.1.3 DC-to-DC output capacitor C2

The value and type of C2 depends on the maximum output current and the ripple voltage which is allowed in the application. Low-ESR tantalum capacitors show good results. The most important specification of C2 is its ESR, which mainly determines output voltage ripple.

13.1.4 Diode D1

The Schottky diode is only used for a short time during takeover from N-type power MOSFET and P-type power MOSFET and vice versa. Therefore, a medium-power diode is sufficient in most applications, for example Philips PRLL5819.

13.1.5 Feedback resistors R1 and R2

The output voltage of the DC-to-DC converter is determined by the resistors R1 and R2. The following conditions apply:

- Only use 1% tolerance SMD-type resistors. If larger body-size resistors are used, the capacitance on pin FB0 will be too large and could cause inaccurate operation
- Resistors R1 and R2 should have a maximum value of 50 kΩ when connected in parallel. A higher value will result in inaccurate operation.

Under these conditions the output voltage can be calculated by the formula:

$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right)$$

13.1.6 Current limiting resistor R10

The maximum instantaneous current is set by the external resistor R10. The preferred type is SMD, 1% accuracy.

The connection of resistor R10 differs for each mode:

- At upconversion: resistor R10 must be connected between pins ILIM and UPOUT/DNIN; the current limiting level is defined by: $I_{lim} = \frac{320}{R10}$
- At downconversion: resistor R10 must be connected between pins ILIM and GND0; the current limiting level is defined by: $I_{lim} = \frac{300}{R10}$

The average inductor current during limited current operation also depends on the inductance value, input voltage, output voltage and resistive losses in all components in the power path. Ensure that $I_{lim} < I_{sat}$ (saturation current) of the inductor.

13.1.7 Reference voltage decoupling capacitor C5

Optionally, a decoupling capacitor can be connected between pin V_{ref} and ground in order to achieve a lower noise level of the output voltages of the LDO. The best choice for C5 is a ceramic multilayer capacitor of approximately 10 nF.

13.1.8 LDO output capacitors C3 and C4

A typical LDO output capacitor is a ceramic multilayer capacitor of 2.2 μF, for example GRM40X5R225K6.3 from Murata. The ESR of the output capacitor must be at least 10 mΩ to achieve stability and the specified transient response.

13.1.9 LDO feedback resistors R3, R4, R5 and R6

The output voltage of each LDO can be set by the external feedback resistors. Their values can be derived from the formulae:

$$V_O = V_{ref} \times \left(1 + \frac{R3}{R4}\right)$$

$$V_O = V_{ref} \times \left(1 + \frac{R5}{R6}\right)$$

The maximum value for each of the LDO feedback resistors is 500 kΩ.

13.1.10 Low battery detector components R7, R8, R9 and C6

Resistor R7 is connected between pin LBO and the input or output pin and must be 330 kΩ or higher.

A single-cell NiCd or NiMH battery can be connected directly to pin LBI1.

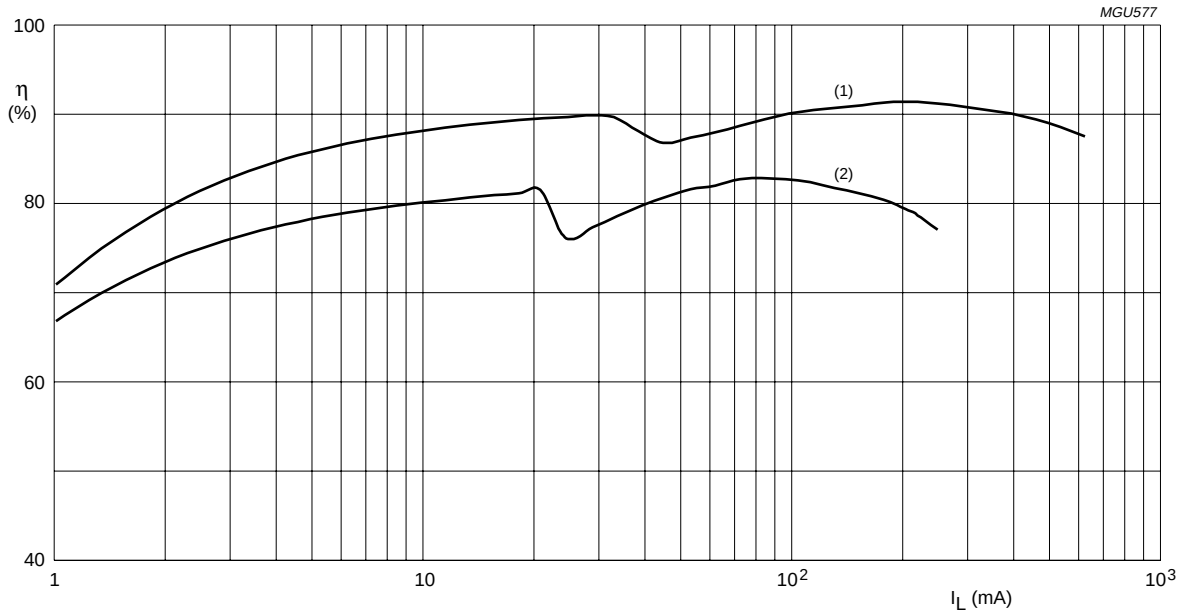
A higher battery voltage must be applied to pin LBI2 using a divider circuit with resistor R8 and R9. In that situation, capacitor C6 (10 nF) must be connected between pin LBI1 and ground. The low-battery detection level for a higher battery voltage can be set by the resistors at pin LBI2 using the formula:

$$V_{LBI2} = 0.90 \times \left(1 + \frac{R8}{R9}\right)$$

13.2 Application recommendations

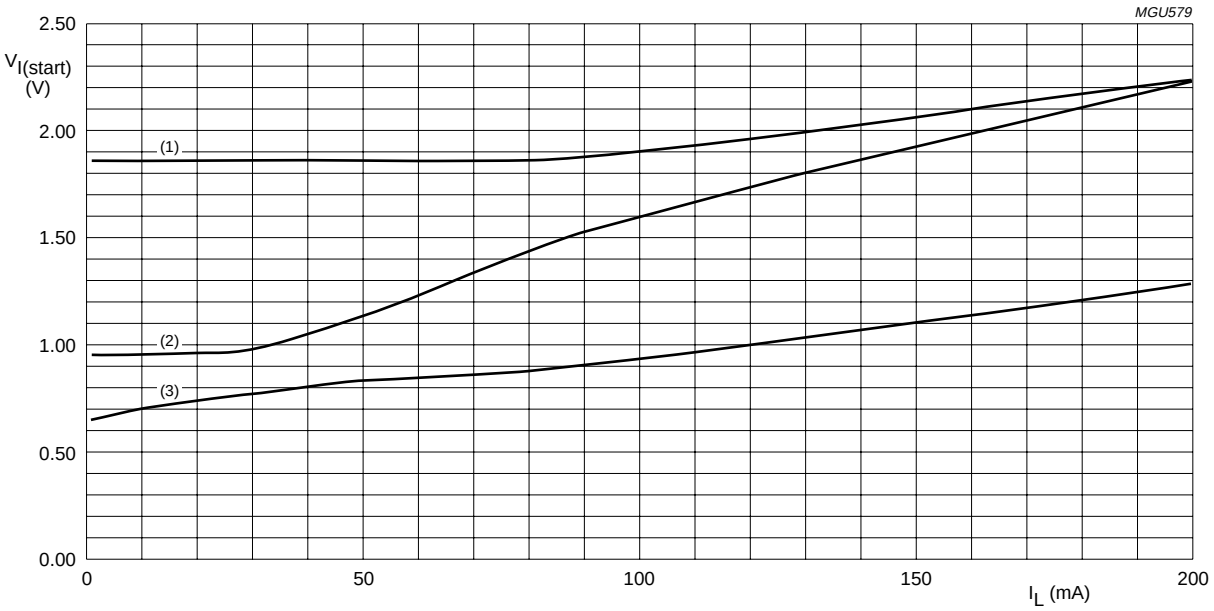
1. Connect loads above approximately 30 mA via LDO1 to avoid start-up problems.
2. Apply minimum input voltage to minimize the power dissipation of the LDOs.
3. For optimum LDO performance, the required drop voltage is 250 mV at I_{LDO} = 50 mA and 500 mV at I_{LDO} = 150 mA; the minimum required voltage drop is calculated by $I_{load} \times 900$ mΩ.
4. Minimum LDO input capacitance is 2.2 μF.
5. Minimum LDO output capacitance is 2.2 μF for load currents between 0 and 150 mA and 4.7 μF for load currents between 0 and 250 mA.
6. X7R or X5R-type ceramic capacitors with a minimum ESR of 10 mΩ must be used on the LDO outputs.
7. With the USB and battery powered concept shown in Fig.9, LDO1 is used as a regulator and not as a switch. For a good load regulation, the DC-to-DC converter is set at 3.5 V and the LDO at 3.3 V. This reduces the efficiency by approximately 5%. However, the efficiency can be improved by lowering the voltage drop, but this will reduce the output voltage performance.
8. In two or more cell applications, pin LBI1 is not used and should be decoupled with a 10 nF capacitor.
9. In a single-cell application pin LBI2 is not used and should be connected to ground.
10. The maximum continuous current at pins LX1 and LX2 is 1 A. During experiments, especially at low input voltages, the current can rise excessively. Avoid this situation by using a power supply with a 1 A current limit.

13.3 Typical performance characteristics



(1) V_I = 2.4 V. V_O = 3.5 V
(2) V_I = 1.2 V.

Fig.10 Efficiency as a function of load current.



(1) Two-cell start-up. V_I = 2.4 V; V_O = 3.5 V.
(2) Single-cell start-up.
(3) Minimum supply voltage after start-up.

Fig.11 Start-up voltage and minimum supply voltage as a function of load current.

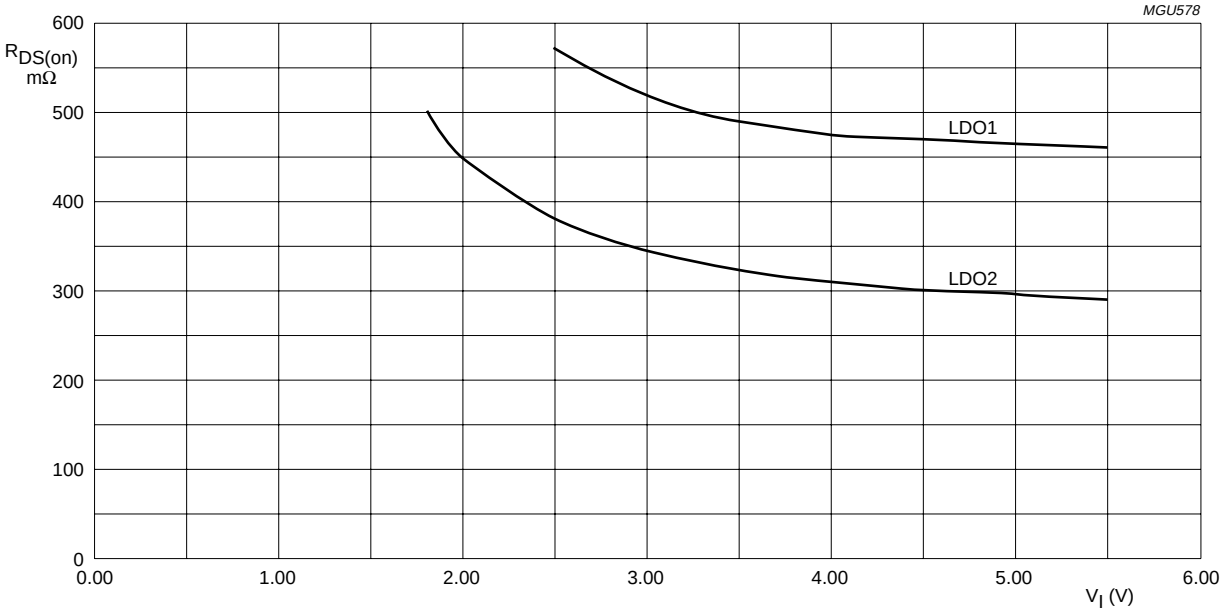
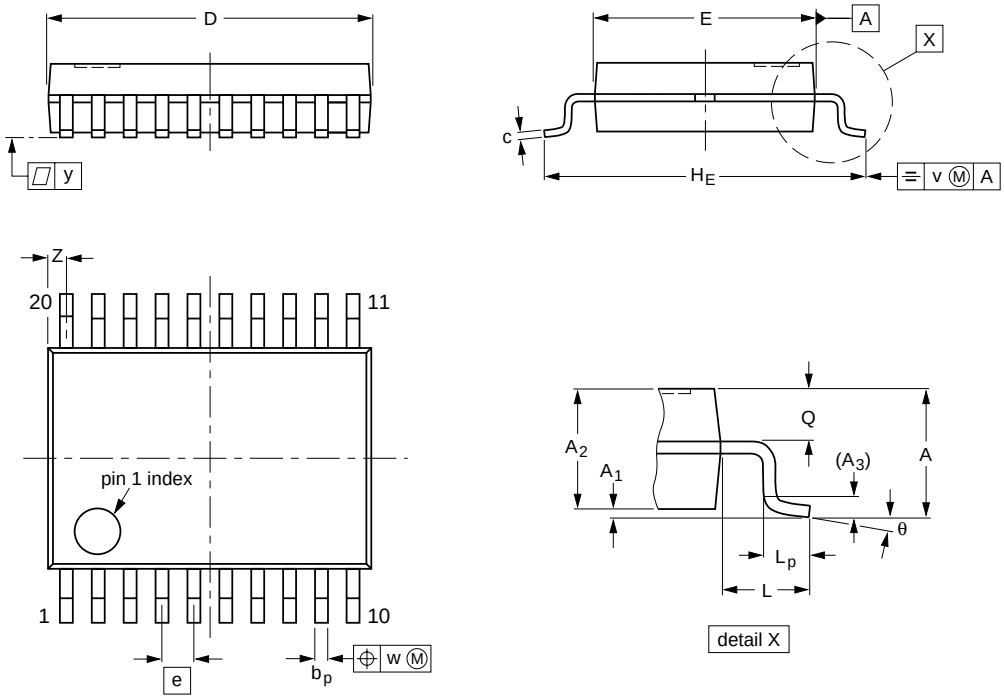
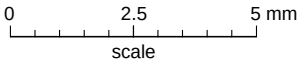


Fig.12 LDO1 and LDO2 drain-to-source on-state resistance as a function of input voltage.

14 PACKAGE OUTLINE

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm **SOT266-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0	1.4 1.2	0.25	0.32 0.20	0.20 0.13	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT266-1		MO-152					~~95-02-22~~ 99-12-27

15 SOLDERING

15.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

15.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

15.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

15.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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