LOW DROP-OUT 5V DUAL VOLTAGE REGULATOR

- OUTPUT CURRENT OF BOTH REGULATORS : 100 mA GUARANTEED
- INTERNAL SHORT-CIRCUIT AND THERMAL PROTECTION
- FIRST REGULATOR OUTPUT : LOW DISCHARGE CURRENT
- SECOND REGULATOR OUTPUT : SWITCHED-OFF WITH ACTIVE DISCHARGE
- RESET OUTPUT WITH ADJUSTABLE PULSE WIDTH

DESCRIPTION

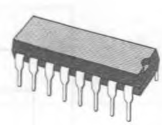
The TEA5110 is a dual positive 5V voltage regulator specially designed to supply a microprocessor and associated circuits.

The first regulator supplies the microprocessor in normal operating conditions. In standby mode, the regulator has a very high output impedance (current drain less than 1 µA) and the microprocessor may be powered by a battery.

The second regulator supplies the peripherals and provides a halt signal to the microprocessor to turn it in standby mode.

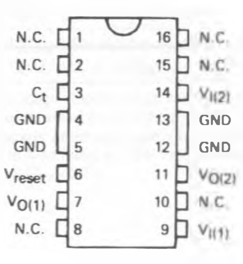
The circuit generates a reset pulse when :

- the supply voltage is applied to the circuit and the output of the second regulator is at its nominal value, and
- when the output of the second regulator is at its nominal value again after a shut-down on the output of the first regulator (see figure 2 page 4).



TEA5110
BATWING DIP16
(Plastic Package)

PIN CONNECTIONS



E88TEA5110-01

1 - N.C.		
2 - N.C.		
3 - C_t	: Time constant capacitor	
4 - GND	: Ground	
5 - GND	: Ground	
6 - V_{reset}	: Reset output	
7 - $V_{O(1)}$	: Output voltage 1	
8 - N.C.		
9 - $V_{I(1)}$	: Input voltage	
10 - N.C.		
11 - $V_{O(2)}$	: Output voltage 2	
12 - GND	: Ground	
13 - GND	: Ground	
14 - $V_{I(2)}$	: Input voltage 2	
15 - N.C.		
16 - N.C.		

ABSOLUTE MAXIMUM RATINGS

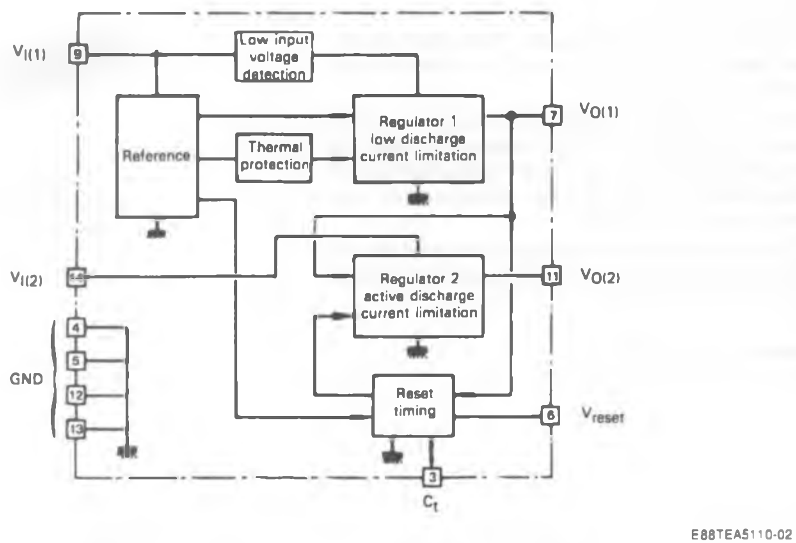
Symbol	Parameter	Value	Unit
V_I	Input Voltage	20	V
I_O	Output Current	Internally Limited	A
P_{tot}	Power Dissipation	Internally Limited	W
T_{oper}	Operating Ambient Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature Range	– 65 to 150	°C

THERMAL DATA

$R_{th\,(j-a)}$*	Junction–ambient Thermal Resistance	45	°C/W
$R_{th\,(j-c)}$	Junction–case Thermal Resistance	11	°C/W

* The $R_{th(j-a)}$ is measured on devices soldered on 35 µm thick copper surface of 40 cm2.

BLOCK DIAGRAM



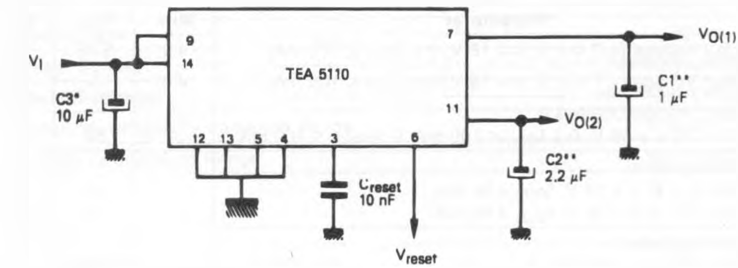
ELECTRICAL CHARACTERISTICS

T_j = + 25 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{O(1)}$	Output Voltage (+ 7 V ≤ V_I ≤ + 18 V, 0 ≤ $I_{O(1)}$ ≤ 100 mA)	4.9	5.05	5.2	V
$V_{O(2)}$	Output Voltage (+ 7 V ≤ V_I ≤ + 18 V, 0 ≤ $I_{O(2)}$ ≤ 100 mA)	4.8	5	5.2	V
$V_{O(1)}-V_{O(2)}$	Output Voltage Difference + 7 V ≤ V_I ≤ + 18 V, 0 ≤ $I_{O(1)}$ ≤ 100 mA, 0 ≤ $I_{O(2)}$ ≤ 100 mA	0	50	100	mV
 $K_{VI(1)}$ $K_{VI(2)}$	Line Regulation + 6.8 V ≤ V_I ≤ + 18 V, $I_{O(1)}$ = 50 mA + 6.8 V ≤ V_I ≤ + 18 V, $I_{O(2)}$ = 50 mA		 10 20	 50 50	 mV mV
 $K_{VO(1)}$ $K_{VO(2)}$	Load Regulation 5 mA ≤ $I_{O(2)}$ ≤ 100 mA, V_I = + 10 V 5 mA ≤ $I_{O(2)}$ ≤ 100 mA, V_I = + 10 V		 10 20	 50 50	 mV mV
I_Q	Quiescent Current (+ 6.8 V ≤ V_I ≤ + 18 V, $I_{Q(1)}$ = $I_{Q(2)}$ = 0)		6	8	mA
 $I_{SC(1)}$ $I_{SC(2)}$	Short–circuit Current V_I = + 10 V, 0 ≤ $V_{O(1)}$ ≤ + 5 V V_I = + 10 V, 0 ≤ $V_{O(2)}$ ≤ + 5 V		 200 200		 mA mA
 $V_I-V_{O(1)}$ $V_I-V_{O(2)}$	Minimum Dropout Voltage - (note 1) Output 1 — $I_{O(1)}$ = 0 Output 1 — $I_{O(1)}$ = 0.1 A Output 2 — $I_{O(2)}$ = 0 Output 2 — $I_{O(2)}$ = 0.1 A		 1.4 1.6 1.5 1.7		 V V V V
$I_{dis(1)}$	$V_{O(1)}$ Discharge Current (V_I = 0, $V_{O(1)}$ = + 5 V)			1	µA
	Minimum Input Voltage to Switch on $V_{O(2)}$ Output (fig. 1, note 2)	(V_{O1}+1.4)	(V_{O1}+1.6)	(V_{O1}+1.8)	V
ΔV_{IL}	Input Hysteresis to Switch off $V_{O(2)}$ Output (fig. 1)	200	300	400	mV
	Minimum $V_{O(1)}$ Output Voltage to Switch on $V_{O(2)}$	4.5	4.6	4.7	V
$\Delta V_{C(1)}$	$V_{O(1)}$ Hysteresis Voltage to switch off $V_{O(2)}$ (fig. 2)	30	50	70	mV
$V_{L(02)}$	$V_{O(2)}$ Low Output Voltage (active discharge) V_I = + 10 V, $I_{O(2)}$ = – 90 mA V_I = + 10 V, $I_{O(2)}$ = – 10 mA		 1.3 120	 1.6 180	 V mV
$V_{L(reset)}$	Reset Low Output Voltage (V_I = + 10 V, I_{reset} = – 16 mA)		120	400	mV
$V_{H(reset)}$	Reset High Output Voltage (V_I = + 10 V, I_{reset} = 1 mA)	$V_{O(2)}$–1V		$V_{O(2)}$	V
t_{reset}	Reset Pulse Duration (V_I = + 10 V, C_{reset} = 10 nF) – Note 3	4	8	16	ms
KVT	Average Temperature Coefficient of Output Voltage (T_j = 0 °C to – 70 °C)		0.5		mV/°C
θ	Thermal Shut Down Temperature	110			°C
SVR	Supply Voltage Rejection Ratio V_I = + 12 V, ΔV_I = 4 Vpp, I_O = 10 mA, f = 100 Hz		50		dB

Notes :
1. The dropout voltage (input-output voltage difference) is measured when the output voltage has dropped 100 mV from the nominal value obtained at 10 V input voltage.
   Dropout voltage is dependent upon load current and junction temperature.
2. $V_{O(1)}$ voltage is measured at 10 V input voltage.
3. t_{reset} (ms) = 0.8 C_{reset} (nF).

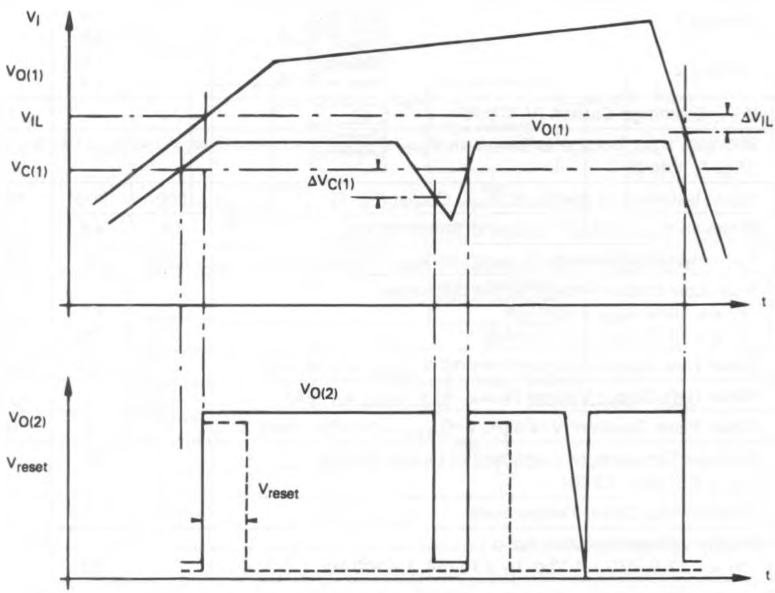
Figure 1 : Typical Application and Test Circuit.



C1, C2, C3 solid tantalum capacitors.
* Required when the circuit is far from power supply capacitors.
** Required for current limitation stability.

E88TEA5110-03

Figure 2 : Dynamic Characteristics of $V_{O(1)}$, $V_{O(2)}$, V_{reset} Outputs.



E88TEA5110-03

PACKAGE MECHANICAL DATA

16 PINS – PLASTIC DIP