

# DATA SHEET

## **TEA6810V; TEA6811V** Front-end and PLL synthesizers for car radios

Product specification  
Supersedes data of September 1994  
File under Integrated Circuits, IC01

1996 Jun 18

## Front-end and PLL synthesizers for car radios

## TEA6810V; TEA6811V

### FEATURES

- Synthesizer function which includes a Voltage Controlled Oscillator (VCO), dividers, phase detector, charge-pump and in-lock detector
- FM mixer with AGC
- AM RF amplifier with AGC
- AM mixer.



### APPLICATIONS

- Car radios.

### GENERAL DESCRIPTION

The TEA6810V and TEA6811V, together with TEA6821V forms an AM/FM receiving concept for electronically tuned car radios.

The TEA681xV is an FM/AM front-end with one local synthesized oscillator for both AM and FM which is used together with the TEA6821T in a double-conversion concept. It delivers a first FM-IF of 72.2 MHz and, for MW/LW, a first AM-IF of 10.7 MHz.

Minimum alignments are required due to wideband RF inputs and the common AM/FM VCO.

High dynamic behaviour and minimum distortion is obtained by a special RF input design combined with AGC. High sensitivity is possible in combination with RF input FETs.

Minimum interference is experienced due a to special synthesizer loop design and ensuring that the I<sup>2</sup>C-bus is inoperative in the locked-tuned condition.

The reference frequency for the synthesizer and the I<sup>2</sup>C-bus information is delivered by the TEA6821V.

The programmable local/dx switch enables switching the gain of the FM mixer from normal AGC control (FM dx) to the forced 4th level of AGC (FM local).

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V <sub>CCA1</sub>	analog supply voltage (pin 2)		4.75	5.0	5.25	V
V <sub>CCA2</sub>	analog supply voltage (pin 13)		8.1	8.5	8.9	V
V <sub>AMant</sub>	AM AGC range	see Fig.4	0.3	–	6.0	V
V <sub>FMant</sub>	FM AGC range	see Fig.5	10	–	600	mV
f <sub>AMant</sub>	AM input frequency		0.144	–	22	MHz
f <sub>FMant</sub>	FM input frequency		60	–	108	MHz
T <sub>amb</sub>	operating ambient temperature		–40	–	+85	°C

### ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA6810V	VSO40	plastic very small outline package; 40 leads	SOT158-1
TEA6811V	VSO40	plastic very small outline package; 40 leads; face down	SOT158-2

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BLOCK DIAGRAM

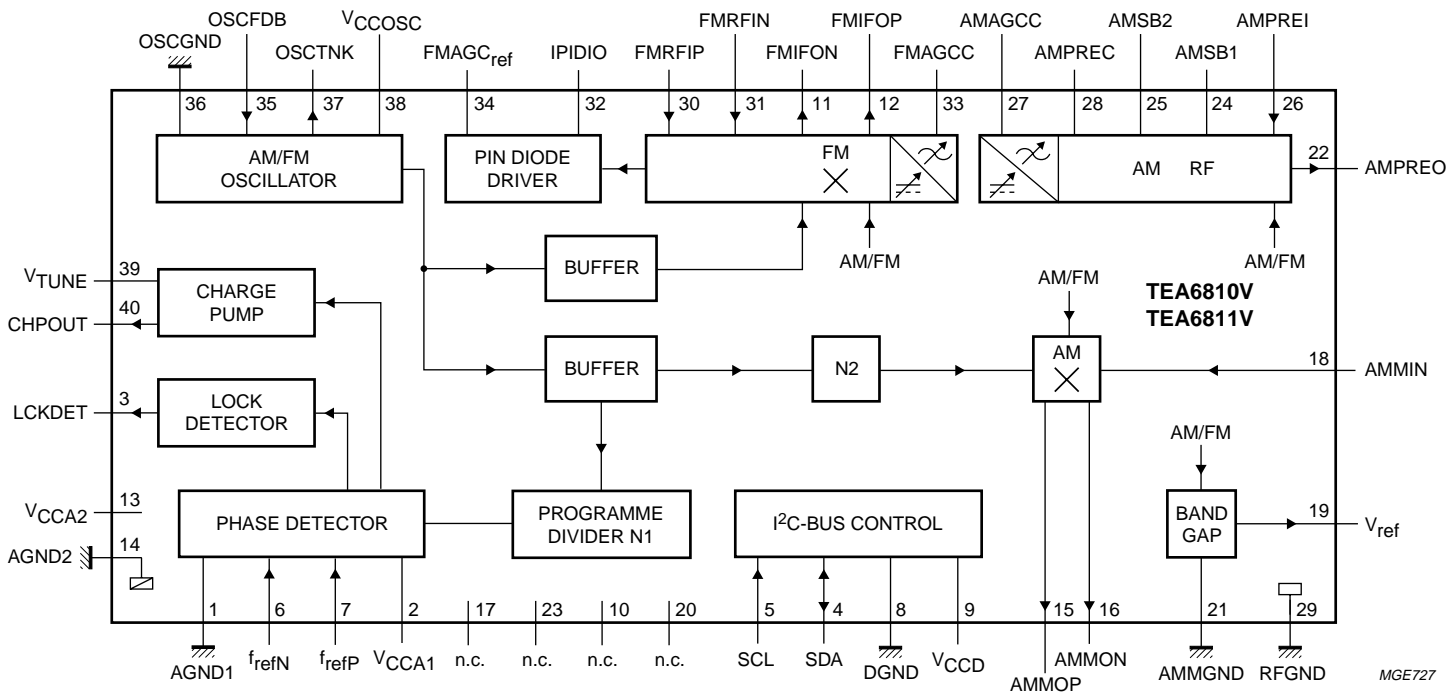


Fig.1 Block diagram.

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## PINNING

SYMBOL	PIN <sup>(1)</sup>		DESCRIPTION
	TEA6810	TEA6811	
AGND1	1	1	analog ground 1
V <sub>CCA1</sub>	2	2	analog supply voltage 1 (+5 V)
LCKDET	3	3	lock detector flag
SDA	4	4	serial data input/output; I <sup>2</sup> C-bus
SCL	5	5	serial clock input; I <sup>2</sup> C-bus
f <sub>refN</sub>	6	6	reference frequency input from TEA6821 N-terminal
f <sub>refP</sub>	7	7	reference frequency input from TEA6821 P-terminal
DGND	8	8	digital ground
V <sub>CCD</sub>	9	9	digital supply voltage (+5 V)
n.c.	10	10	not connected
FMIFON	11	11	FM mixer negative output (72.2 MHz)
FMIFOP	12	12	FM mixer positive output (72.2 MHz)
V <sub>CCA2</sub>	13	13	analog supply voltage 2 (+8.5 V)
AGND2	14	14	analog ground 2
AMMOP	15	15	AM mixer positive output (10.7 MHz)
AMMON	16	16	AM mixer negative output (10.7 MHz)
n.c.	17	17	not connected
AMMIN	18	18	AM mixer RF input
V <sub>ref</sub>	19	19	reference voltage output from AM band gap
n.c.	20	20	not connected
AMMGND	21	21	AM mixer ground
AMPREO	22	22	AM preamplifier output
n.c.	23	23	not connected
AMSB1	24	24	AM feedback switch SB1
AMSB2	25	25	AM feedback switch SB2
AMPREI	26	26	AM preamplifier input
AMAGCC	27	27	AM AGC capacitor
AMPREC	28	28	AM preamplifier decoupling capacitor
RFGND	29	29	RF ground
FMRFIP	30	30	RF positive input for FM mixer
FMRFIN	31	31	RF negative input for FM mixer
IPIDIO	32	32	pin diode drive
FMAGCC	33	33	FM AGC integrating capacitor
FMAGC <sub>ref</sub>	34	34	FM AGC reference voltage
OSCFDB	35	35	oscillator feedback input
OSCGND	36	36	oscillator ground
OSCTNK	37	37	oscillator tank output

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**TEA6810V; TEA6811V**

SYMBOL	PIN <sup>(1)</sup>		DESCRIPTION
	TEA6810	TEA6811	
V <sub>CCOSC</sub>	38	38	oscillator supply voltage (+8.5 V)
V <sub>TUNE</sub>	39	39	tuning voltage
CHPOUT	40	40	charge pump output

**Note**

1. Pins 10, 17, 20 and 23 should be connected to a common ground.

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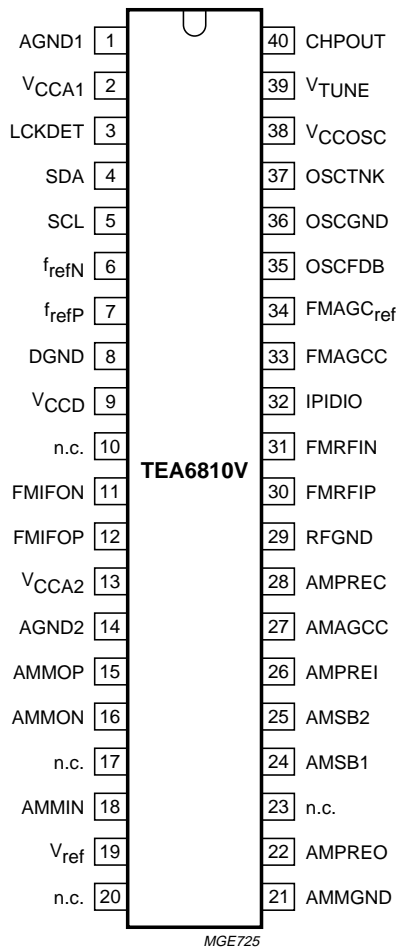


Fig.2 Pin configuration (TEA6810).

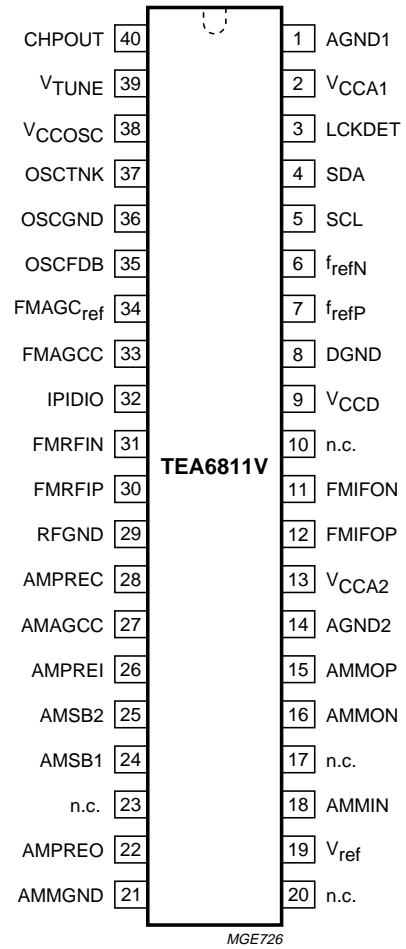


Fig.3 Pin configuration (TEA6811).

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## I<sup>2</sup>C-BUS ORGANIZATION

The TEA6810V; TEA6811V is controlled via the I<sup>2</sup>C-bus which is driven from the TEA6821V. For programming purposes a module address and four data bytes are required. When used partially, the transmission must be ended by a stop condition.

**Table 1** Bit organization

START	MODULE ADDRESS	PROGRAMMABLE DIVIDER DATA				SWITCH CONTROL	TEST			STOP	
S	byte 0	A	byte 1	A	byte 2	A	byte 3	A	byte 4	A	P

**Table 2** I<sup>2</sup>C-bus address and received bytes

BYTES TO BE RECEIVED (4 BYTES)	BUS ADDRESS							
	MSB				LSB			
	1	1	0	0	0	1	0	0
Byte 1 <sup>(1)</sup> program divider N1 (Low byte)	S7	S6	S5	S4	S3	S2	S1	S0
Byte 2 <sup>(1)</sup> program divider N1 (High byte)	S15	S14	S13	S12	S11	S10	S9	S8
Byte 3 switching	MSB in-lock counter	LSB in-lock counter	1 = HIGH 0 = LOW current tuning oscillator	1 = HIGH 0 = LOW current charge pump	1 = FM local 0 = FM dx	MSB divider N2	LSB divider N2	1 = FM 0 = AM
Byte 4 testing	1 = 3-state 0 = normal charge pump	1 = $f_{div}$ 0 = LCKDET	1 = test 0 = normal in-lock counter	X <sup>(2)</sup>	X	X	X	X

### Notes

1. N1 divider ratio is  $(N + 2)$ ; where N is the programmed binary number composed of bytes 1 and 2. For the minimum ratio; if  $N < 2048$  then N1 divider ratio is  $\{2048 + (N - 2)\}$ .
2. X = don't care.

**Table 3** N2 divider

N2 DIVIDER	MSB	LSB
3	0	0
5	0	1
10	1	0
15	1	1

**Table 4** In-lock

IN-LOCK	MSB	LSB	AM/FM
8	0	0	FM
16	1	0	AM or FM
32	1	1	AM or FM
48	0	0	AM
64	0	1	AM

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## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CCA1</sub>	analog supply voltage (pin 2)		-0.3	12	V
V <sub>CCA2</sub>	analog supply voltage (pin 13)		-0.3	12	V
V <sub>CCD</sub>	digital supply voltage (pin 9)		-0.3	12	V
V <sub>CCOSC</sub>	oscillator supply voltage (pin 38)		-0.3	12	V
P <sub>tot</sub>	maximum power dissipation		-	0.55	W
T <sub>stg</sub>	storage temperature		-65	+150	°C
V <sub>es</sub>	electrostatic handling	note 1	-300	+300	V

### Note

- Machine model: equivalent to discharging a 200 pF capacitor through 0 Ω.

## HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
R <sub>th j-a</sub>	thermal resistance from junction to ambient in free air	90	K/W

## DC CHARACTERISTICS

V<sub>13</sub> = V<sub>38</sub> = 8.5 V; V<sub>9</sub> = V<sub>2</sub> = 5.0 V; T<sub>amb</sub> = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
I <sub>CCA1</sub>	analog input current (pin 2)	AM mode	7	9	mA
		FM mode	6	8	mA
I <sub>CCA2</sub>	analog input current (pin 13)	AM mode	17	22	mA
		FM mode	15	18	mA
I <sub>CCOSC</sub>	oscillator input current (pin 38)	AM mode	4	6	mA
		FM mode	6	8	mA
I <sub>CCD</sub>	digital input current (pin 9)	AM mode	32	35	mA
		FM mode	27	30	mA
I <sub>AMMO</sub>	AM mixer output current (pins 15 and 16)	AM mode	8.5	-	mA
		FM mode	0	-	mA
I <sub>FMIFO</sub>	FM mixer output current (pins 11 and 12)	AM mode	0	-	mA
		FM mode	10	-	mA



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## AC CHARACTERISTICS

All voltage and current values are RMS values; noise values are unweighted within the bandwidth 0.03 to 20 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>AM signal channel;</b> (note 1; see Fig.4)						
RF PREAMPLIFIER STAGE						
Z <sub>21</sub>	transimpedance		40	65	–	kΩ
AGC STAGE; F <sub>12</sub> = 1 MHz						
V <sub>i2</sub>	HF input voltage	AGC start level 1	–	750	–	mV
		AGC start level 2	–	850	–	mV
		AGC stop level 1	–	145	–	mV
		AGC stop level 2	–	170	–	mV
I <sub>AGCsink</sub>	AGC sink current	V <sub>18</sub> = V <sub>19</sub> + 0.5 V; V <sub>27</sub> = V <sub>19</sub>	–	1	–	μA
I <sub>AGCsource</sub>	AGC source current	V <sub>18</sub> = V <sub>19</sub> - 0.5 V; V <sub>27</sub> = V <sub>19</sub>	–	2	–	mA
MIXER (f <sub>o</sub> = 10.7 MHz)						
R <sub>i</sub>	input resistance between pins 18 and 21		15 <sup>(2)</sup>	20	–	kΩ
C <sub>i</sub>	input capacitance between pins 18 and 21		–	5	–	pF
C <sub>o</sub>	output capacitance between pins 15 and 16		–	–	5 <sup>(2)</sup>	pF
G <sub>mC</sub>	conversion transconductance (I <sub>15</sub> to I <sub>16</sub> /V <sub>18</sub> to V <sub>19</sub> )		2.4	2.75	3.1	mS
ΔG <sub>mC</sub>	variation in conversion transconductance		–	–0.005	–	mS/K
IP <sub>3</sub>	third-order intermodulation		130 <sup>(2)</sup>	137	–	dBmV
CP	–1 dB compression point		114 <sup>(2)</sup>	120	–	dBmV
V <sub>n(eq)</sub>	equivalent input noise voltage		–	9	–	nV/√Hz
OSCILLATOR/N2 DIVIDER						
R <sub>N2</sub>	internal divider ratio (N2)	set by I <sup>2</sup> C-bus; see Table 3	–	15	–	
			–	10	–	
			–	5	–	
			–	3	–	
REFERENCE VOLTAGE (PIN 19)						
V <sub>o</sub>	output reference voltage		–	2.75	–	V
Z <sub>o</sub>	output impedance		–	40	–	Ω
I <sub>o(max)</sub>	maximum output current		–	–	0.1	mA

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>FM signal channel</b> (note 3; see Fig.5)						
MIXER						
$R_i$	input resistance between pins 30 and 31		1.65 <sup>(2)</sup>	2	–	k $\Omega$
$C_i$	input capacitance between pins 30 and 31		3.4 <sup>(2)</sup>	4	4.5 <sup>(2)</sup>	pF
$R_o$	output resistance between pins 11 and 12		10	–	–	k $\Omega$
$C_o$	output capacitance between pins 11 and 12		6.5 <sup>(2)</sup>	8	9 <sup>(2)</sup>	pF
$G_m$	transconductance	$I_{11}$ to $I_{12}/V_{30}$ to $V_{31} < V_{AGC1}$	5.5	6.3	6.9	mS
		$I_{11}$ to $I_{12}/V_{30}$ to $V_{31} < V_{AGC2}$	–	4.7	–	mS
		$I_{11}$ to $I_{12}/V_{30}$ to $V_{31} < V_{AGC3}$	–	2.3	–	mS
		$I_{11}$ to $I_{12}/V_{30}$ to $V_{31} > V_{AGC3}$	–	1.0	–	mS
$\Delta G_m T$	variation in transconductance with temperature	$< V_{AGC1}$	–	–0.015	–	mS/K
F	noise figure (both sidebands)	$f_i = 72.2$ MHz; PLL tuned	–	7 <sup>(2)</sup>	–	dB
$IP_3$	third-order intermodulation		135 <sup>(2)</sup>	139	–	dBmV
CP	–1 dB compression point		120 <sup>(2)</sup>	127	–	dBmV
$\alpha_{IF1}$	1st IF rejection		25 <sup>(2)</sup>	30	–	dB
$V_{AGC(S)}$	AGC start voltage between pins 30 and 31	start level 1	4.8	6.2	7.8	mV
		start level 2	–	15	–	mV
		start level 3	–	39	–	mV
$V_{AGC(H)}$	AGC hysteresis voltage	hysteresis level 1	–	1	–	mV
		hysteresis level 2	–	2	–	mV
		hysteresis level 3	–	3	–	mV
$R_{33}$	FM AGC output resistance		–	5	–	k $\Omega$
$I_{pin}$	pin diode current	$V_{32} = 1.4$ V	4	–	–	mA
$V_{pin}$	start level pin diode voltage between pins 30 and 31	$I_o = 1$ mA	–	57	–	mV
OSCILLATOR						
$f_{osc}$	oscillator frequency		116.8	–	207	MHz
$\Delta f_{osc}/\Delta T$	oscillator temperature dependence		–	–90	–	10 <sup>–6</sup> /K

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SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
SYNTHESIZER (see Fig.6)							
<i>Reference frequency input (pins 6 and 7)</i>							
$V_{\text{ref(p-p)}}$	reference frequency input voltage ( $V_6$ to $V_7$ ) (peak-to-peak value)			–	0.4	–	V
$t_{\text{trans}}$	reference frequency transition time			–	–	50	ns
$f_{\text{ref}}$	input reference frequency for:	tuning step (kHz)	N2				
	FM	50	–	–	50	–	kHz
	AM standard SW1	5	10	–	50	–	kHz
	AM full-band MW (USA)	10	5	–	50	–	kHz
	FM	25	–	–	25	–	kHz
	AM full-band SW1	5	5	–	25	–	kHz
	AM standard MW/LW	1	15	–	15	–	kHz
	AM full-band MW/LW	3	5	–	15	–	kHz
	AM full-band SW2	5	3	–	15	–	kHz
	FM	10	–	–	10	–	kHz
	AM standard SW1	1	10	–	10	–	kHz
	AM full-band MW/LW	1	5	–	5	–	kHz
	AM full-band SW1	1	5	–	5	–	kHz
	AM full-band SW2	1	3	–	5	–	kHz
<i>Phase detector/charge pump</i>							
$I_{\text{OL}}$	LOW level output charge pump current	$V_{40} = 4 \text{ V}$		120	175	215	$\mu\text{A}$
$I_{\text{OH}}$	HIGH level output charge pump current	$V_{40} = 4 \text{ V}$		0.85	1	1.2	mA
$V_{\text{OL}}$	LOW level tuning voltage at charge pump LOW	$I_{\text{O}} = 0.5I_{\text{charge}}; V_{13} = 8.5 \text{ V}$		0.2	–	8.25	V
$V_{\text{OH}}$	HIGH level tuning voltage at charge pump HIGH	$I_{\text{O}} = 0.5I_{\text{charge}}; V_{13} = 8.5 \text{ V}$		0.4	–	8.0	V
$I_{\text{oz}}$	3-state output current	$V_{40} = 4 \text{ V}$		–5	–	+5	nA
$\Delta f_{\text{r(p-p)}}$	residual FM frequency (peak-to-peak value)	$B = 300 \text{ Hz to } 20 \text{ kHz};$ $I_{\text{charge}} = I_{\text{OL}}; f_i = 100 \text{ MHz}$		–	9	16 <sup>(2)</sup>	Hz
$t_{\text{lock}}$	lock time	FM = 88 to 108 MHz		–	2	–	ms
		FM = 108 to 88 MHz		–	2	–	ms
		AM = 510 to 1710 kHz		–	2	–	ms
		AM = 1710 to 510 kHz		–	2	–	ms

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SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
<i>Programmable divider</i>							
N <sub>min</sub>	minimum programmable ratio			–	2 050	–	
N <sub>max</sub>	maximum programmable ratio			–	65537	–	
DR	divider ratio for:	tuning step (kHz)	N2				
	FM	50	–	2050	–	3 604	
	FM	25	–	6388	–	7208	
	FM	10	–	15970	–	18020	
	FM	5	–	31940	–	36040	
	AM standard MW/LW	1	15	10844	–	12420	
	AM standard SW1	5	10	3320	–	4140	
	AM standard SW1	1	10	16600	–	20700	
	AM full-band MW/LW	3	5	10448	–	10973	
	AM full-band MW/LW	1	5	31344	–	32920	
	AM full-band SW1	5	5	6700	–	8240	
	AM full-band SW1	1	5	33500	–	41200	
	AM full-band SW2	5	3	8240	–	10640	
	AM full-band SW2	1	3	41200	–	53200	
AM full-band MW (USA)	10	5	3172	–	3292		
<i>In-lock detector (reset by any start condition on I<sup>2</sup>C-bus)</i>							
V <sub>OH</sub>	in-lock HIGH level output voltage (pin 3)			4.0	–	5.0	V
V <sub>OL</sub>	in-lock LOW level output voltage (pin 3)			0	–	0.4	V
t <sub>d</sub>	in-lock delay	counter length = N		–	$N \times \frac{1}{f_{ref}}$	–	ms

**Notes**

1.  $f_{i1} = 1053$  kHz;  $f_{mod} = 400$  Hz;  $m = 0.3$ ;  $V_{i1} = V_{i2} = 1$  mV; N2 divider switched to divide-by-15.
2. Not measured 100% in production.
3.  $V_{i1} = 1$  mV;  $f_{i1} = 98$  MHz;  $f_{mod} = 1$  kHz;  $\Delta f = \pm 22.5$  kHz.

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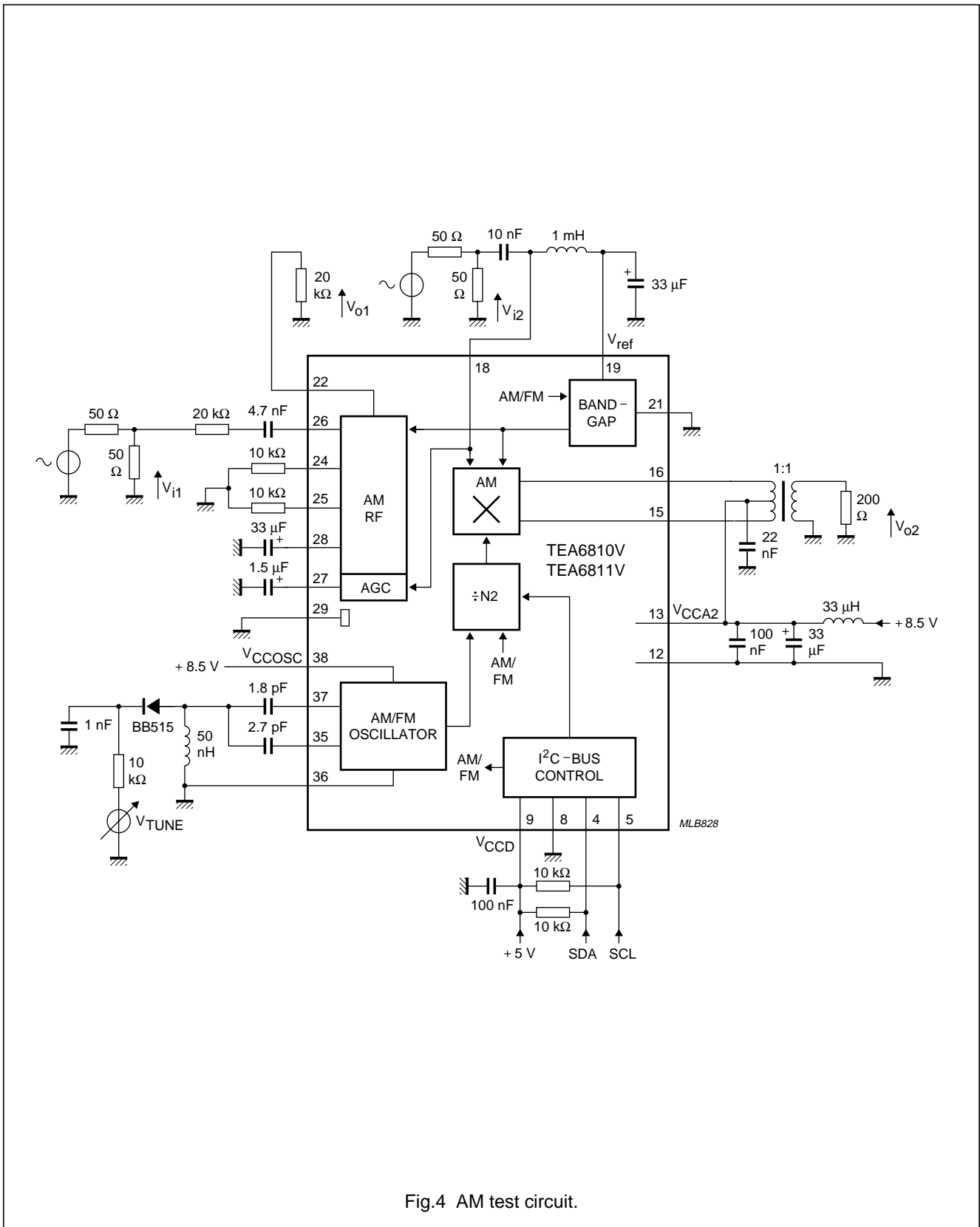


Fig.4 AM test circuit.

# Front-end and PLL synthesizers for car radios

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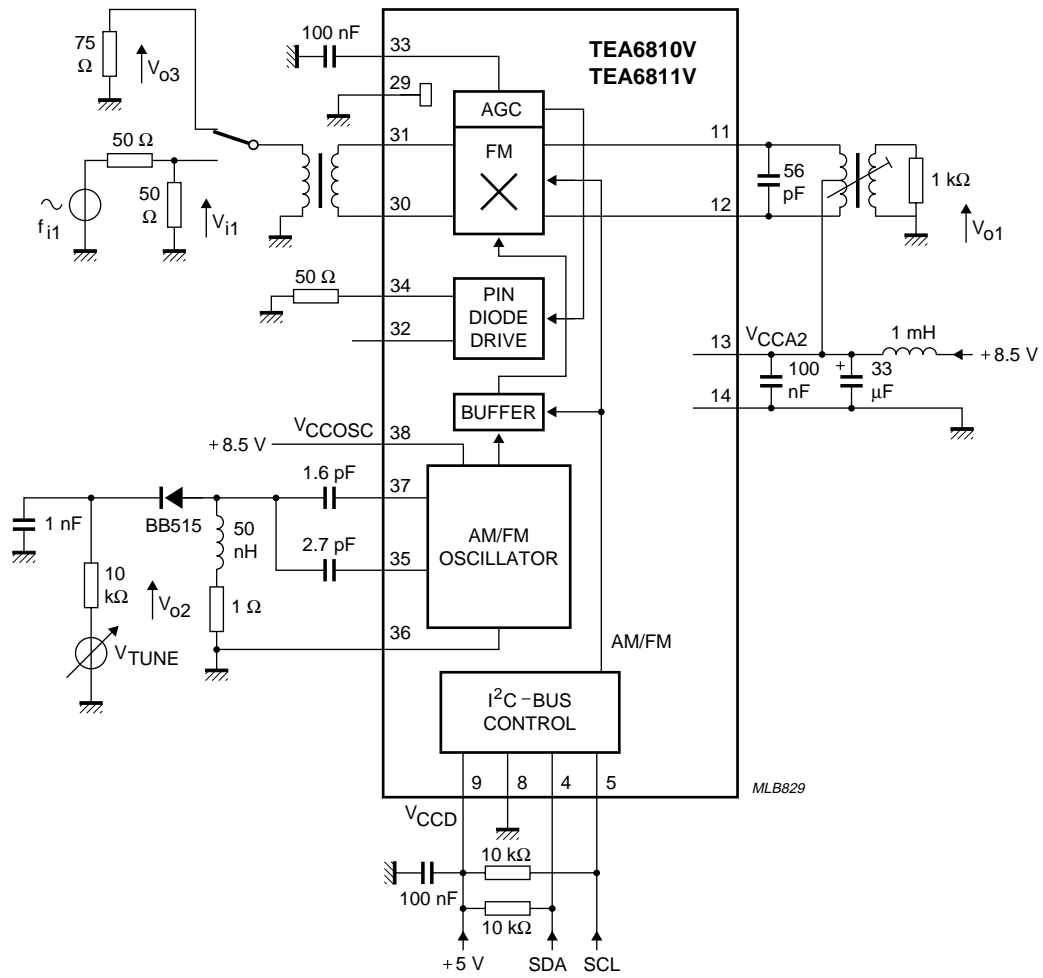


Fig.5 FM test circuit.

Front-end and PLL synthesizers for car radios

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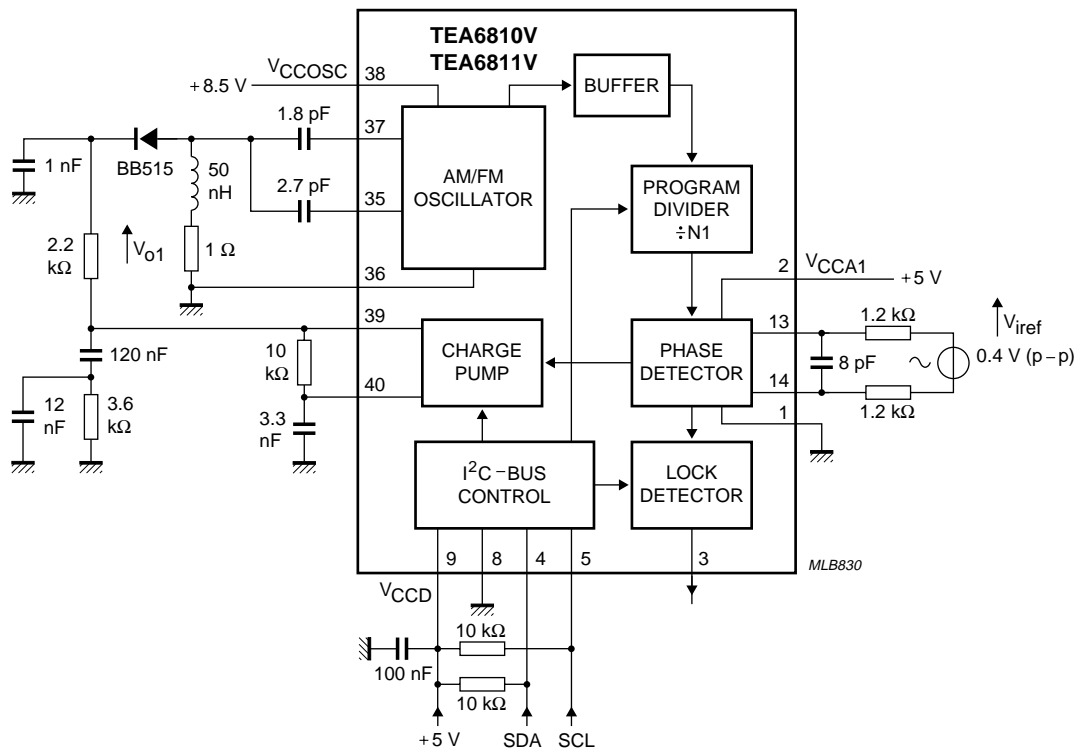


Fig.6 Synthesizer test circuit.

# Front-end and PLL synthesizers for car radios

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## INTERNAL PIN CONFIGURATION

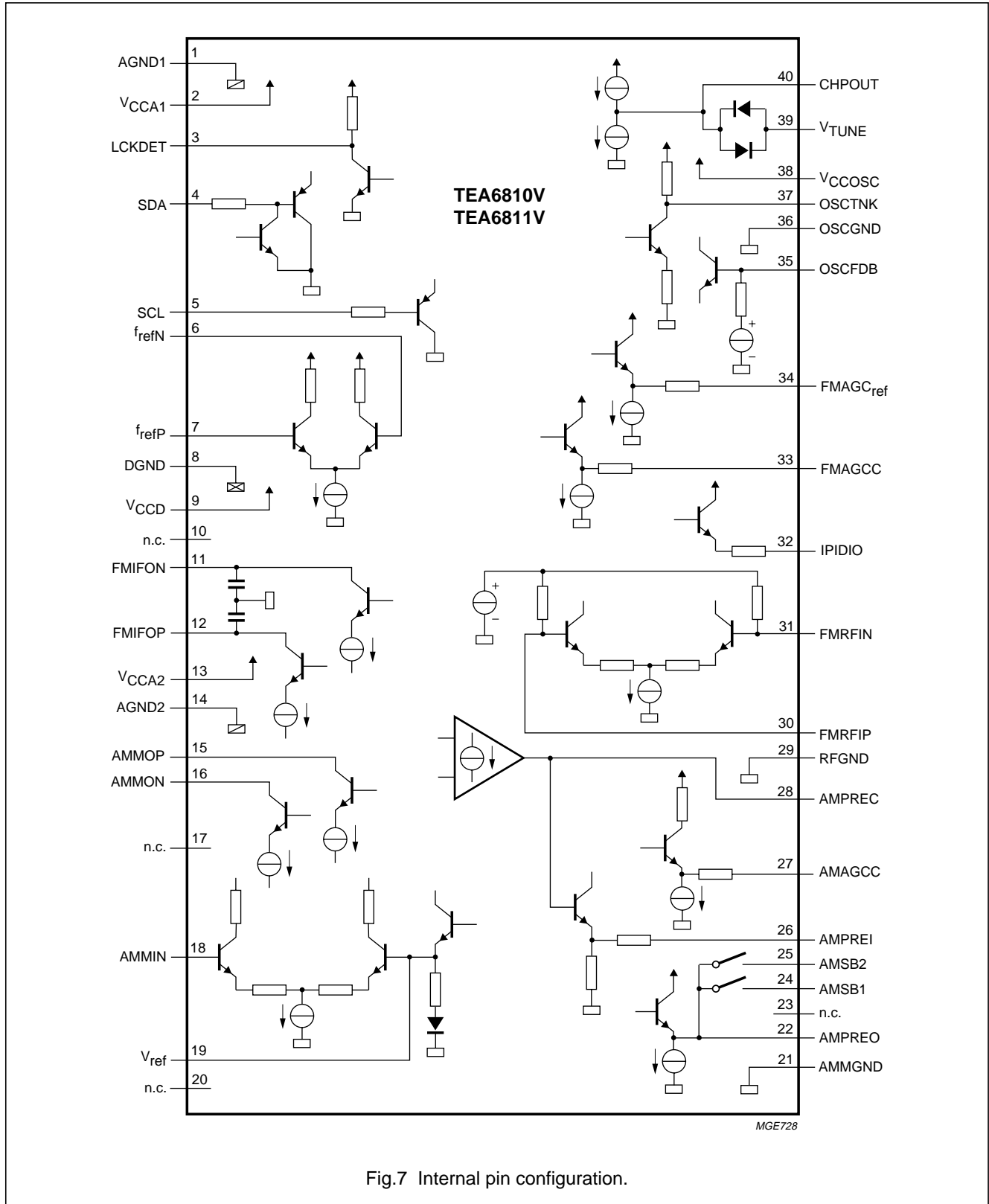


Fig.7 Internal pin configuration.



# Front-end and PLL synthesizers for car radios

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### APPLICATION INFORMATION

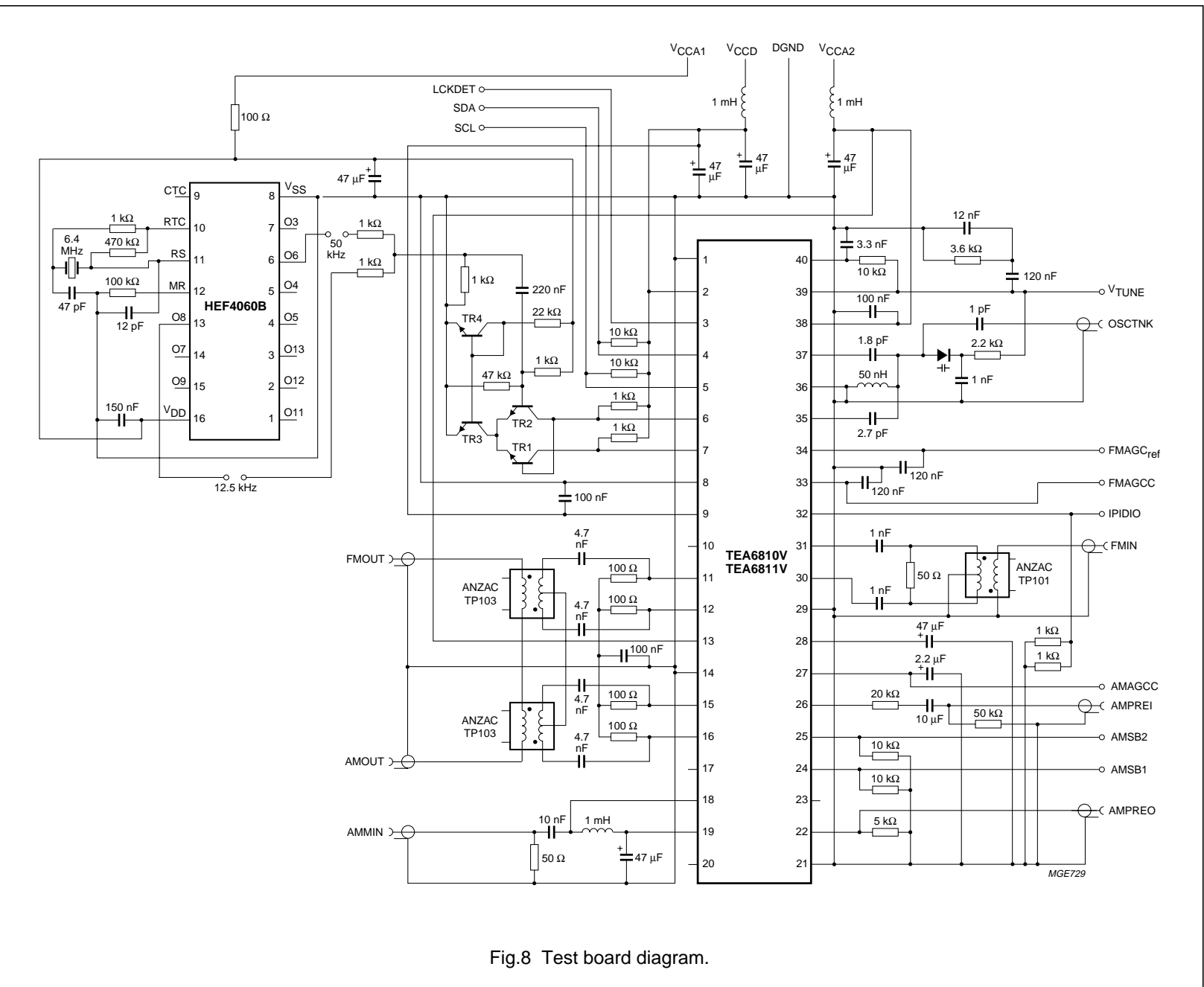


Fig.8 Test board diagram.

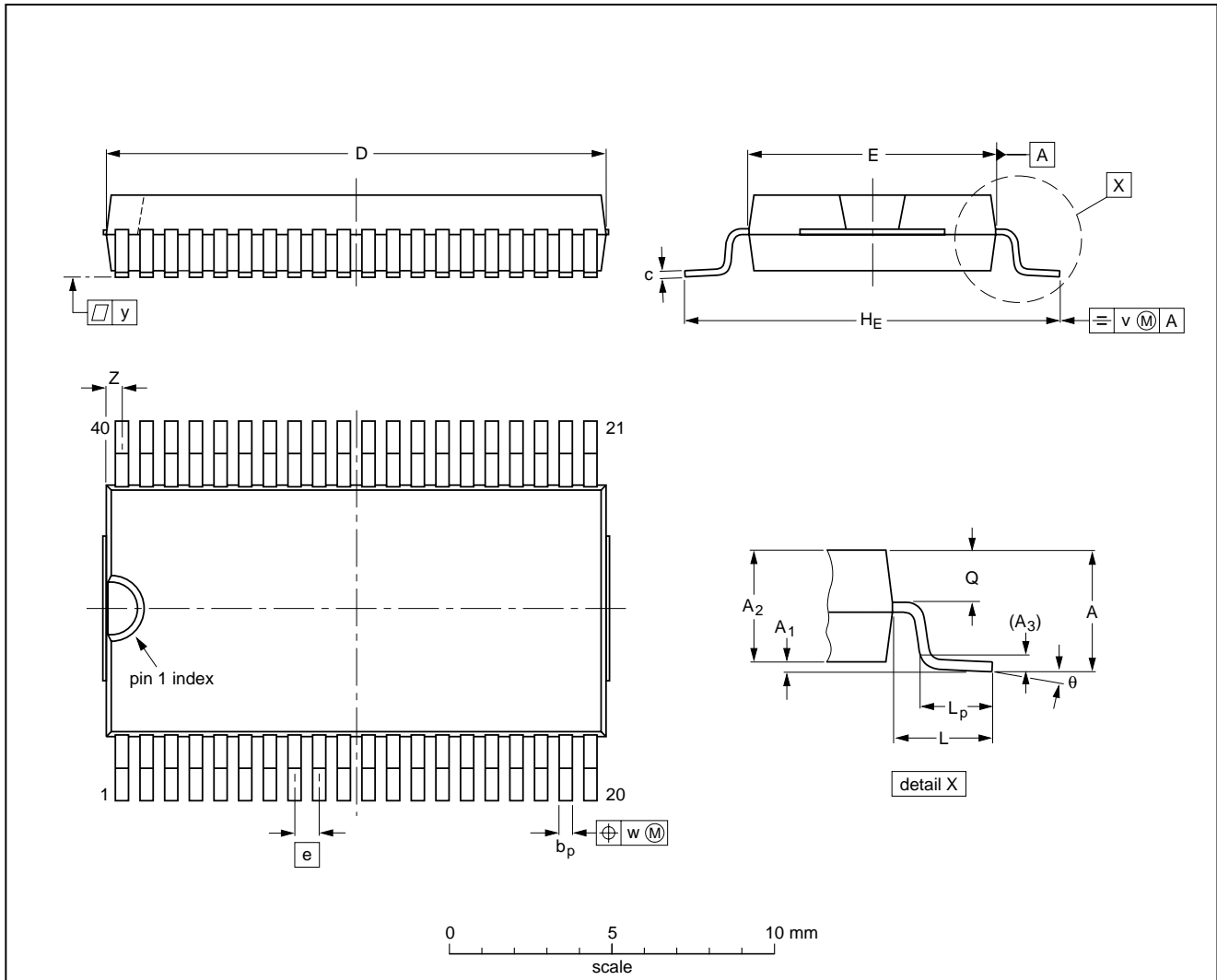
# Front-end and PLL synthesizers for car radios

## TEA6810V; TEA6811V

### PACKAGE OUTLINES

VSO40: plastic very small outline package; 40 leads

SOT158-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.70	0.3 0.1	2.45 2.25	0.25	0.42 0.30	0.22 0.14	15.6 15.2	7.6 7.5	0.762	12.3 11.8	2.25	1.7 1.5	1.15 1.05	0.2	0.1	0.1	0.6 0.3	7° 0°
inches	0.11	0.012 0.004	0.096 0.089	0.010	0.017 0.012	0.0087 0.0055	0.61 0.60	0.30 0.29	0.03	0.48 0.46	0.089	0.067 0.059	0.045 0.041	0.008	0.004	0.004	0.024 0.012	

**Notes**

1. Plastic or metal protrusions of 0.4 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

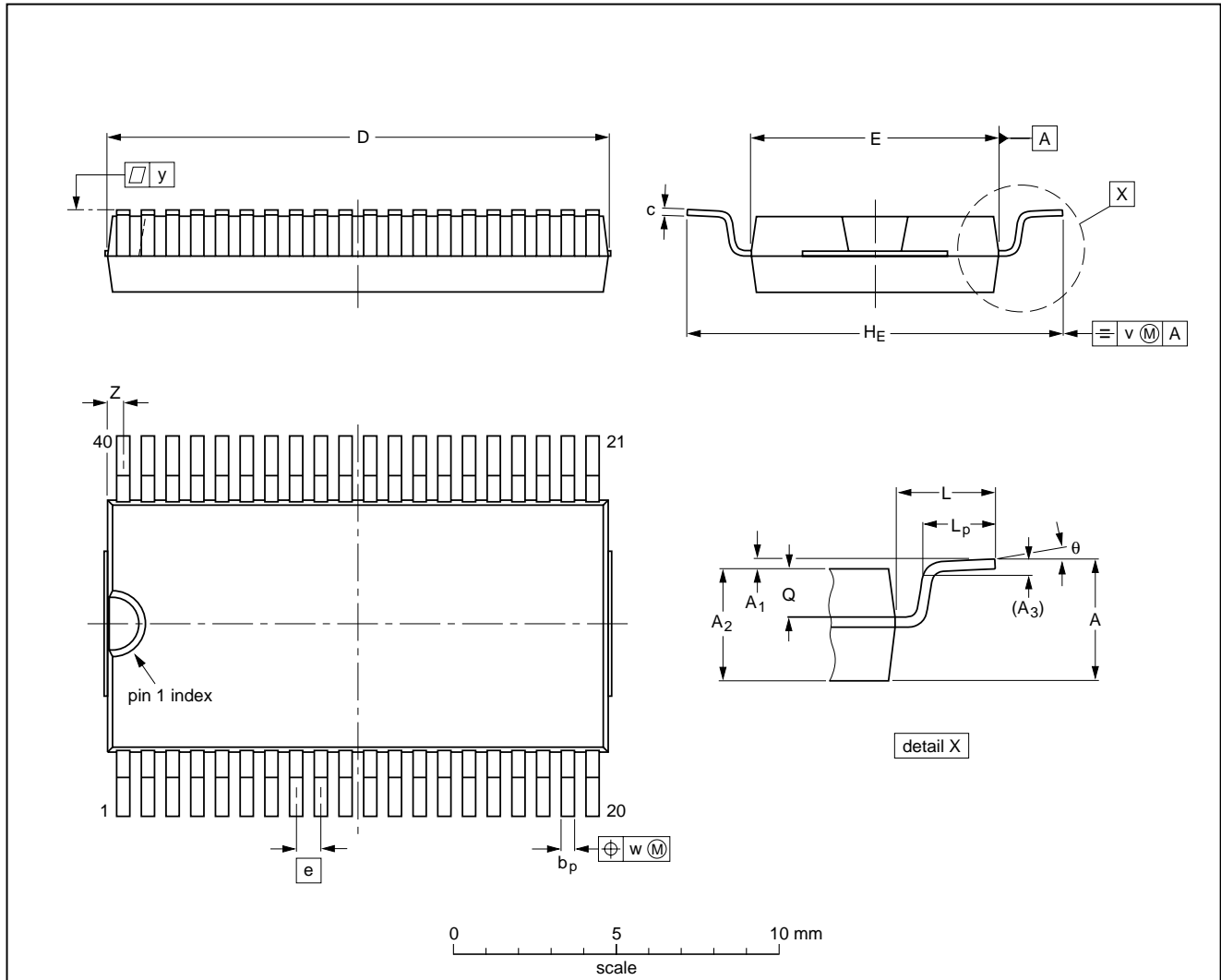
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT158-1						92-11-17 95-01-24

Front-end and PLL synthesizers for car radios

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VSO40: plastic very small outline package; 40 leads; face down

SOT158-2



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.70	0.3 0.1	2.45 2.25	0.25	0.42 0.30	0.22 0.14	15.6 15.2	7.6 7.5	0.762	12.3 11.8	2.25	1.7 1.5	1.15 1.05	0.2	0.1	0.1	0.6 0.3	7° 0°
inches	0.11	0.012 0.004	0.096 0.089	0.010	0.017 0.012	0.0087 0.0055	0.61 0.60	0.30 0.29	0.03	0.48 0.46	0.089	0.067 0.059	0.045 0.041	0.008	0.004	0.004	0.024 0.012	

Note

1. Plastic or metal protrusions of 0.4 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT158-2					92-11-17 95-01-24

## Front-end and PLL synthesizers for car radios

TEA6810V; TEA6811V

### SOLDERING

#### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "*IC Package Databook*" (order code 9398 652 90011).

#### Reflow soldering

Reflow soldering techniques are suitable for all VSO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

#### Wave soldering

Wave soldering techniques can be used for all VSO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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### DEFINITIONS

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

### LIFE SUPPORT APPLICATIONS

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**NOTES**

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**NOTES**

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