

# TIB82S105BC

## 16 × 48 × 8 FIELD-PROGRAMMABLE LOGIC SEQUENCER WITH 3-STATE OUTPUTS OR PRESET

SRPS025A – D2897, SEPTEMBER 1985 – REVISED NOVEMBER 1995

- 50-MHz Clock Rate
- Power-On Preset of All Flip-Flops
- 6-Bit Internal State Register With 8-Bit Output Register
- Power Dissipation . . . 600 mW Typical
- Programmable Asynchronous Preset or Output Control
- Functionally Equivalent to, but Faster Than 82S105A†

### description

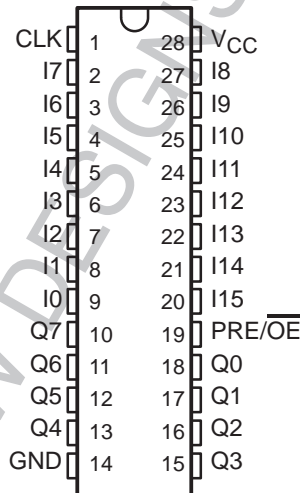
The TIB82S105BC is a TTL field-programmable state machine of the Mealy type. This state machine (logic sequencer) contains 48 product terms (AND terms) and 14 pairs of sum terms (OR terms). The product and sum terms are used to control the 6-bit internal state register and the 8-bit output register.

The outputs of the internal state register (P0–P5) are fed back and combined with the 16 inputs (I0–I15) to form the AND array. In addition a single sum term is complemented and fed back to the AND array, which allows any of the product terms to be summed, complemented, and used as an input to the AND array.

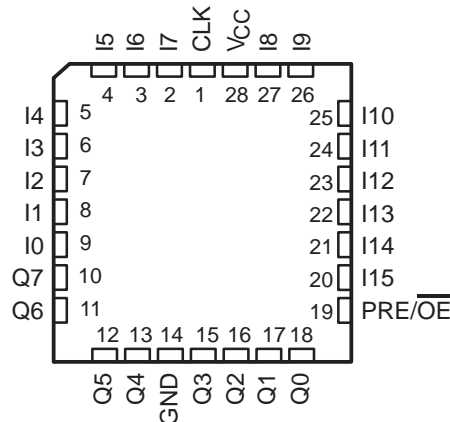
The state and output registers are positive-edge-triggered S/R flip-flops. These registers are unconditionally preset high during power up. Pin 19 can be used to preset both registers or, by blowing the proper fuse, be converted to an output control function.

The TIB82S105BC is characterized for operation from 0°C to 75°C.

**N PACKAGE  
(TOP VIEW)**



**FN PACKAGE  
(TOP VIEW)**



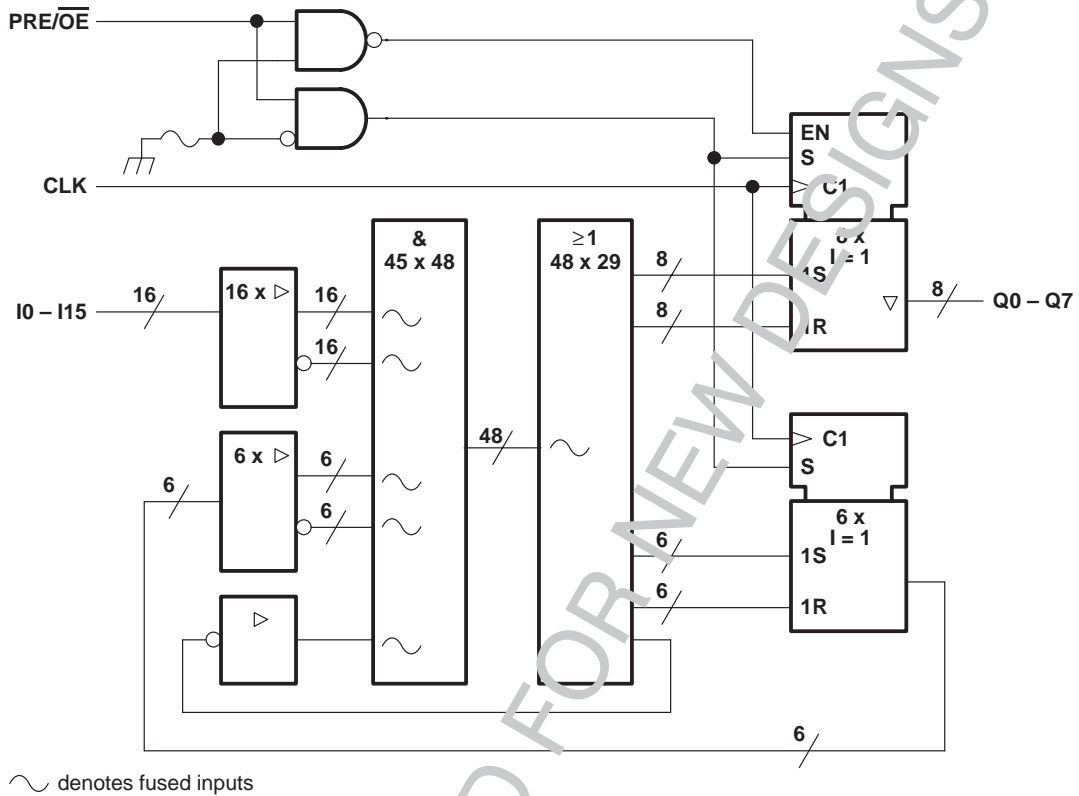
† Power-up preset and asynchronous preset functions are not identical to 82S105A. See Recommended Operating Conditions.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

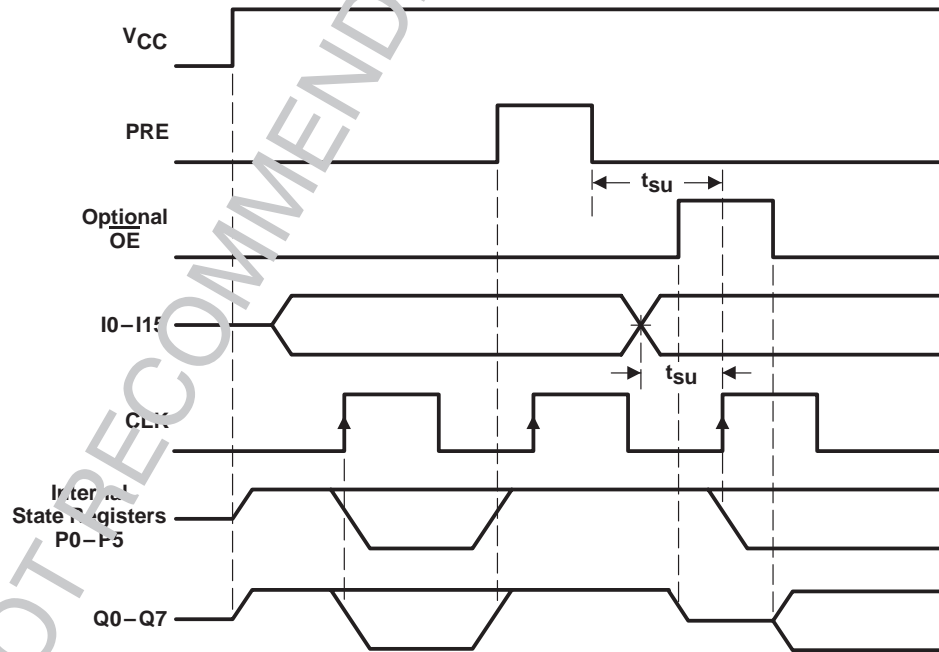


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**functional block diagram (positive logic)**



**timing diagram**

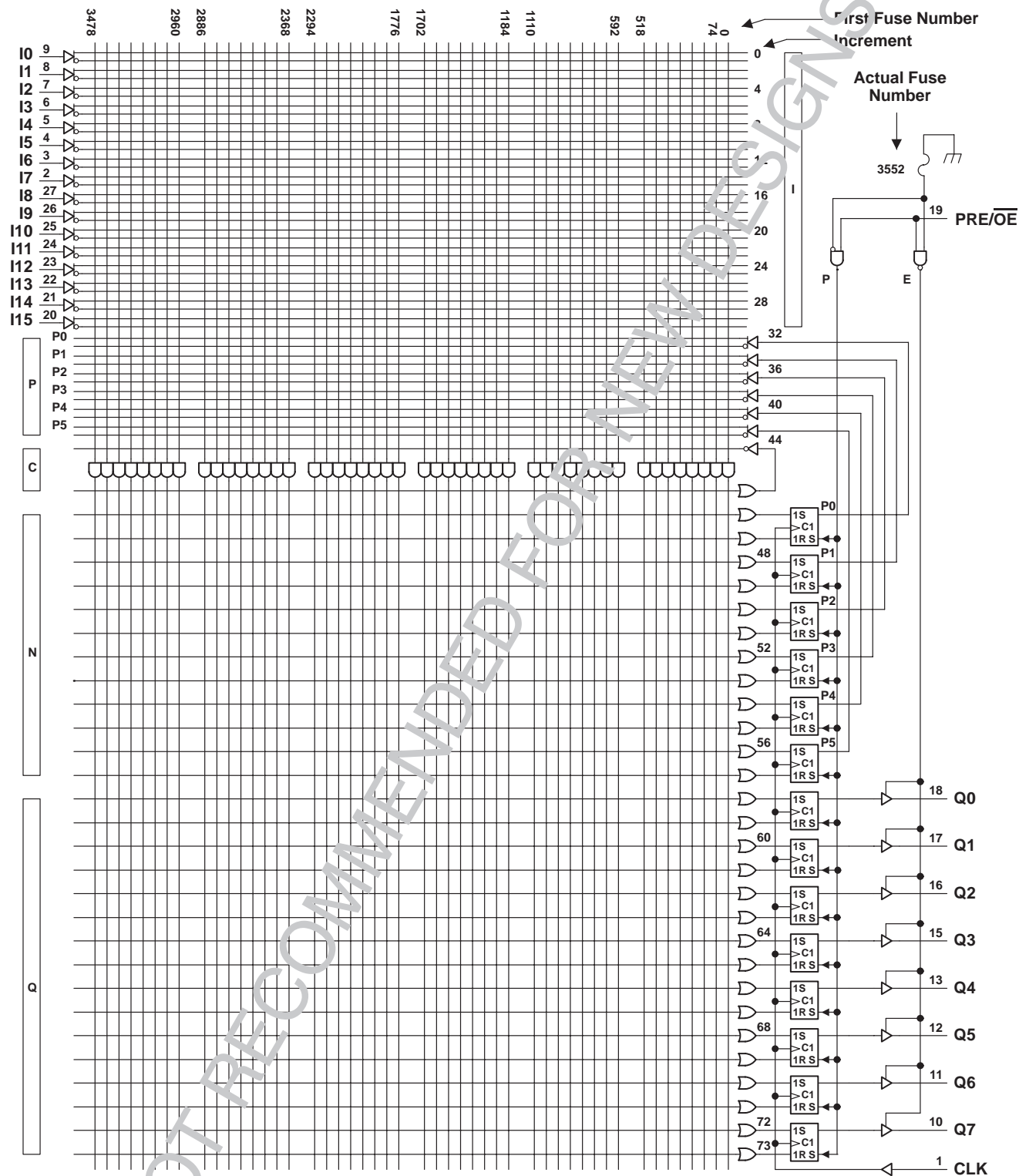


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### logic diagram (positive logic)



- NOTES: 1. All AND gate inputs with a blown link float to the high level.  
 2. All OR gate inputs with a blown link float to the low level.  
 3. Fuse numbers = First fuse number + Increment



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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 4)	7 V
Input voltage (see Note 4)	5.5 V
Voltage applied to disabled output (see Note 4)	5.5 V
Operating free-air temperature range	0°C to 75°C
Storage temperature range	–65°C to 150°C

NOTE 4: These ratings apply except for programming pins during a programming cycle.

### recommended operating conditions

		MIN	NOM	MAX	UNIT	
$V_{CC}$	Supply voltage	4.75	5	5.25	V	
$V_{IH}$	High-level input voltage	2		5.5	V	
$V_{IL}$	Low-level input voltage			0.8	V	
$I_{OH}$	High-level output current			–3.2	mA	
$I_{OL}$	Low-level output current			24	mA	
$f_{clock}$	Clock frequency†	1 thru 48 product terms without C-array ‡		0	50	MHz
		1 thru 48 product terms with C-array		0	30	
$t_w$	Pulse duration	Clock high or low		10		ns
		Preset		15		
$t_{su}$	Setup time before CLK↑, 1 thru 48 product terms	Without C-array		15		ns
		With C-array		30		
$t_{su}$	Setup time, Preset low (inactive) before CLK↑§	8			ns	
$t_h$	Hold time, input after CLK↑	0			ns	
$T_A$	Operating free-air temperature	0	25	75	°C	

† The maximum clock frequency is independent of the internal programmed configuration. If an output is fed back externally to an input, the maximum clock frequency must be calculated.

‡ The C-array is the single sum term that is complemented and fed back to the AND array.

§ After Preset goes inactive, normal clocking resumes on the first low-to-high clock transition.

NOT RECOMMENDED FOR NEW DESIGNS



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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$	$V_{CC} = 4.75\text{ V}$ ,	$I_I = -18\text{ mA}$			-1.2	V
$V_{OH}$	$V_{CC} = 4.75\text{ V}$ ,	$I_{OH} = -3.2\text{ mA}$	2.4	3		V
$V_{OL}$	$V_{CC} = 4.75\text{ V}$ ,	$I_{OL} = 24\text{ mA}$		0.37	0.5	V
$I_{OZH}$	$V_{CC} = 5.25\text{ V}$ ,	$V_O = 2.7\text{ V}$			20	$\mu\text{A}$
$I_{OZL}$	$V_{CC} = 5.25\text{ V}$ ,	$V_O = 0.4\text{ V}$			-20	$\mu\text{A}$
$I_I$	$V_{CC} = 5.25\text{ V}$ ,	$V_I = 5.5\text{ V}$			25	$\mu\text{A}$
$I_{IH}$	$V_{CC} = 5.25\text{ V}$ ,	$V_I = 2.7\text{ V}$			20	$\mu\text{A}$
$I_{IL}$	$V_{CC} = 5.25\text{ V}$ ,	$V_I = 0.4\text{ V}$			-0.25	$\text{mA}$
$I_{O\ddagger}$	$V_{CC} = 5.25\text{ V}$ ,	$V_O = 2.25\text{ V}$	-30		-112	$\text{mA}$
$I_{CC}$	$V_{CC} = 5.25\text{ V}$ , PRE/OE at GND,	$V_I = 4.7\text{ V}$ , Outputs open		120	180	$\text{mA}$

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
$f_{\text{max}}^{\S}$	Without C array		R1 = 500 $\Omega$ , R2 = 500 $\Omega$ , See Figure 5	50	70		MHz
	With C array			30	45		
$t_{pd}$	CLK $\uparrow$	Q			8	15	ns
$t_{pd}$	PRE $\uparrow$	Q			12	20	ns
$t_{pd}$	$V_{CC}\uparrow$	Q			0	10	ns
$t_{en}$	$\overline{\text{OE}}\downarrow$	Q			10	20	ns
$t_{dis}$	$\overline{\text{OE}}\uparrow$	Q			5	10	ns

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

§  $f_{\text{max}}$  is independent of the internal programmed configuration and the number of product terms used.

### programming information

Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

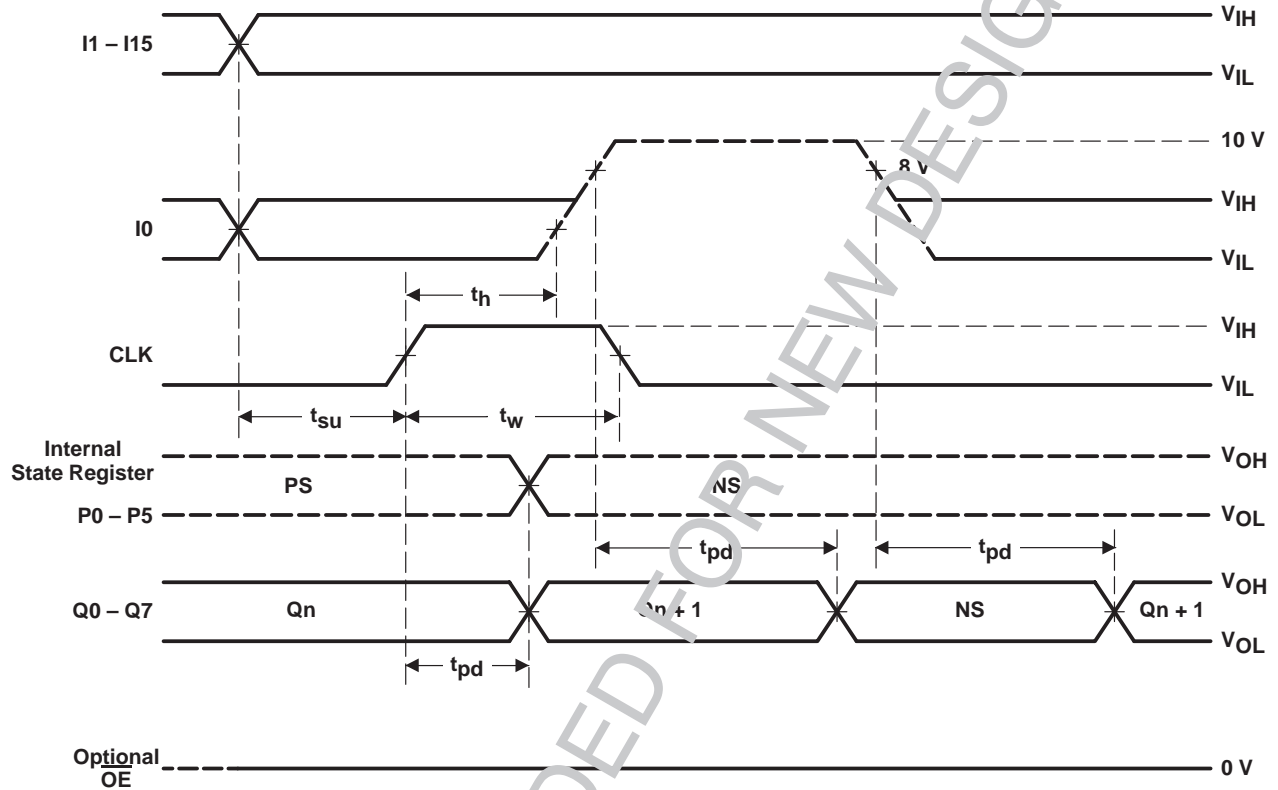


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**diagnostics**

A diagnostics mode is provided with these devices that allows the user to inspect the contents of the state register. When I0 (pin 9) is held at 10 V, the state register bits P0–P5 will appear at the Q0–Q5 outputs and Q6–Q7 will be high. The contents of the output register will remain unchanged.



PS = Present state, NS = Next state

Figure 1. Diagnostic Waveforms

NOT RECOMMENDED FOR NEW DESIGNS



## TIB82S105B, 82S105A COMPARISON

The Texas Instruments TIB82S105B is a 16 × 48 × 8 Field-Programmable Logic Sequencer that is functionally equivalent to the Signetics 82S105A. However, the TIB82S105B is designed for a maximum speed of 50 MHz with the preset function being made conventional. As a result the TIB82S105B differs from the 82S105A in speed and in the preset recovery function.

The TIB82S105B is a high-speed version of the original 82S105A. The TIB82S105B features increased switching speeds with no increase in power. The maximum operating frequency is increased from 20 MHz to 50 MHz and does not decrease as more product terms are connected to each sum (OR) line. For instance, if all 48 product terms were connected to a sum line on the original 82S105A, the  $f_{max}$  would be about 15 MHz. The  $f_{max}$  for the TIB82S105B remains at 50 MHz regardless of the programmed configuration. In addition, the preset recovery sequence was changed to a conventional recovery sequence, providing quicker clock recovery times. This is explained in the following paragraph.

The TIB82S105B and the 82S105A are equipped with power-up preset and asynchronous preset functions. The power-up preset causes the registers to go high during power up. The asynchronous preset inhibits clocking and causes the registers to go high whenever the preset pin is taken high. After a power-up preset occurs, the minimum setup time from power up to the first clock pulse must be met in order to assure that clocking is not inhibited. In a similar manner after an asynchronous preset, the preset input must return low (inactive) for a given time,  $t_{SU}$ , before clocking.

The Signetics 82S105A was designed in such a way that after both power-up preset and asynchronous preset it requires that a high-to-low clock transition occur before a clocking transition (low-to-high) will be recognized. This is shown in Figure 3. The Texas Instruments TIB82S105B does not require a high-to-low clock transition before clocking can be resumed, it only requires that the preset be inactive 8 ns (preset inactive-state setup time) before the clock rising edge. See Figure 4.

The TIB82S105B, with an  $f_{max}$  of 50 MHz, is ideal for systems in which the state machine must run several times faster than the system clock. It is recommended that the TIB82S105B be used in new designs. **However, if the TIB82S105B is used to replace the 82S105A, then the customer must understand that clocking will begin with the first clock rising edge after preset.**

Table 3. Speed Differences

PARAMETER	82S105A SIGNETICS	TIB82S105B TI ONLY
$f_{max}$	20 MHz	50 MHz
$t_{pd, CLK \rightarrow Q}$	20 ns	15 ns

NOT RECOMMENDED FOR NEW DESIGNS



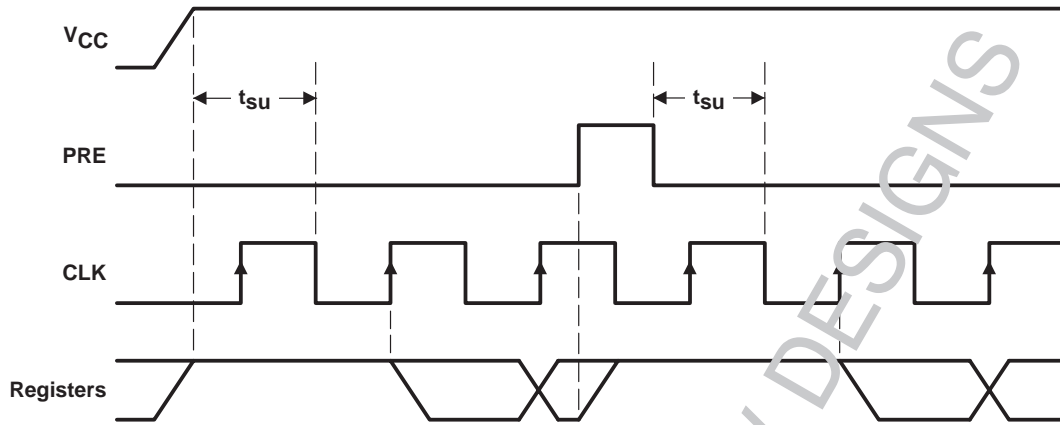


Figure 3. 82S105A Preset Recovery Operation

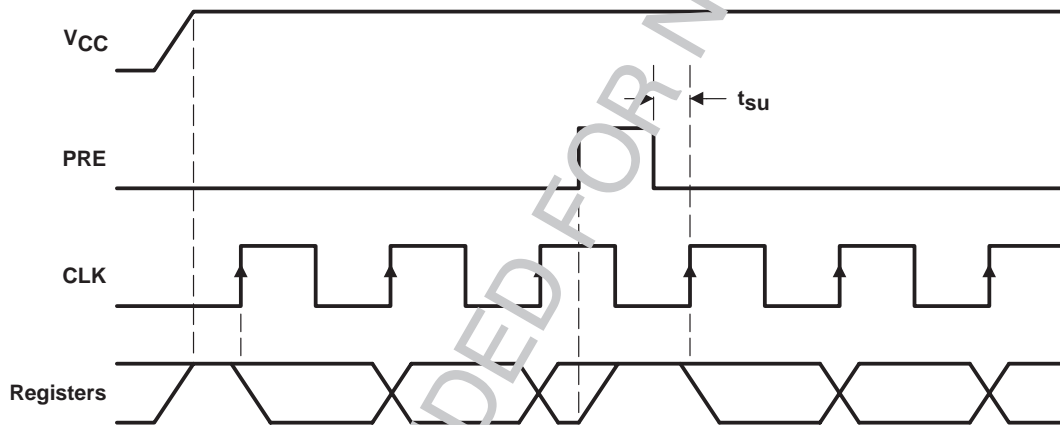


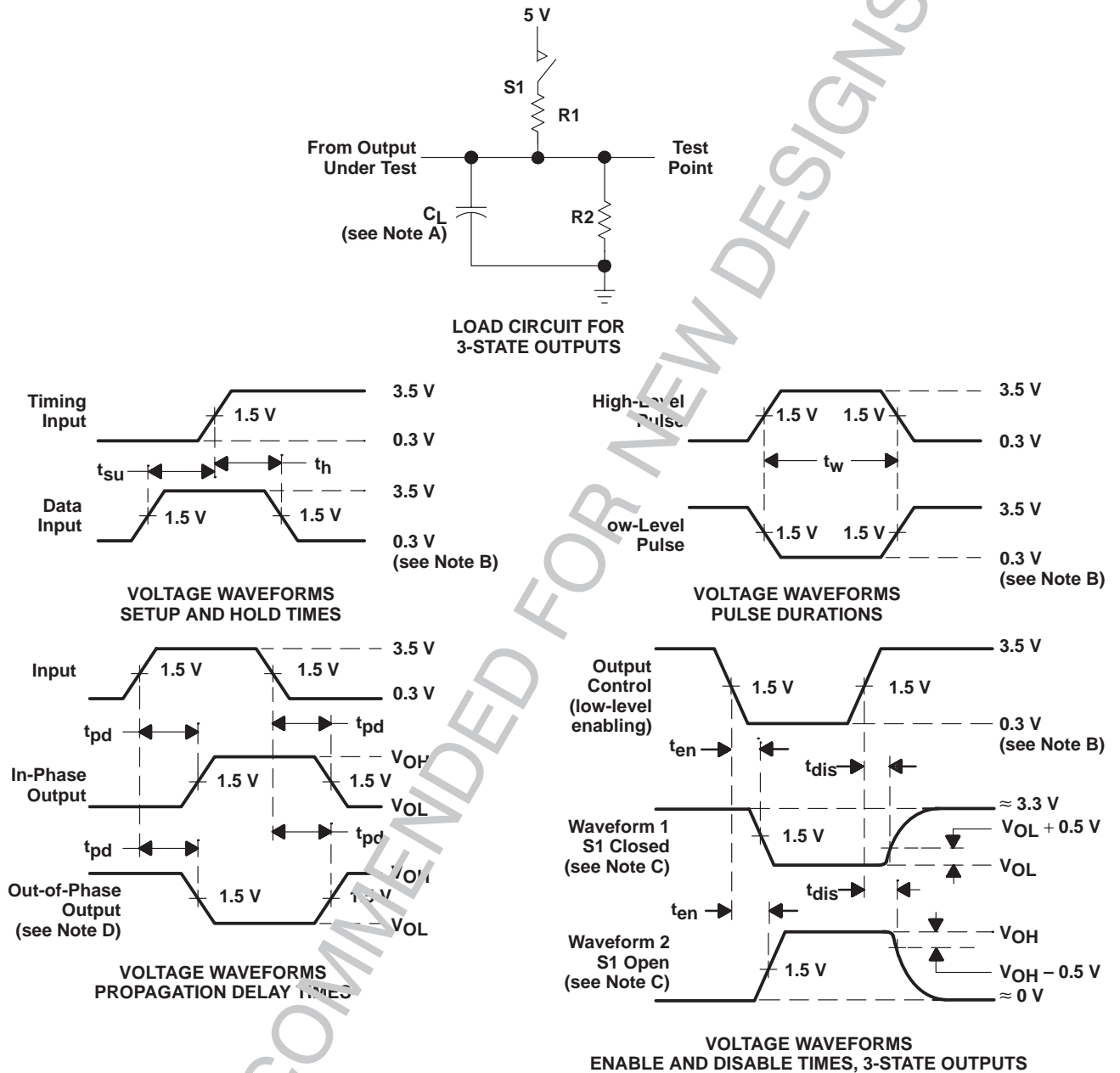
Figure 4. TIB82S105B Preset Recovery Operation

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**PARAMETER MEASUREMENT INFORMATION**



- NOTES: A.  $C_L$  includes probe and jig capacitance and is 50 pF for  $t_{pd}$  and  $t_{en}$ , 5 pF for  $t_{dis}$ .  
 B. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.  
 E. Equivalent loads may be used for testing.

**Figure 5. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TIB82S105BCFN	OBSOLETE	PLCC	FN	28		TBD	Call TI	Call TI
TIB82S105BCN	OBSOLETE	PDIP	N	28		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

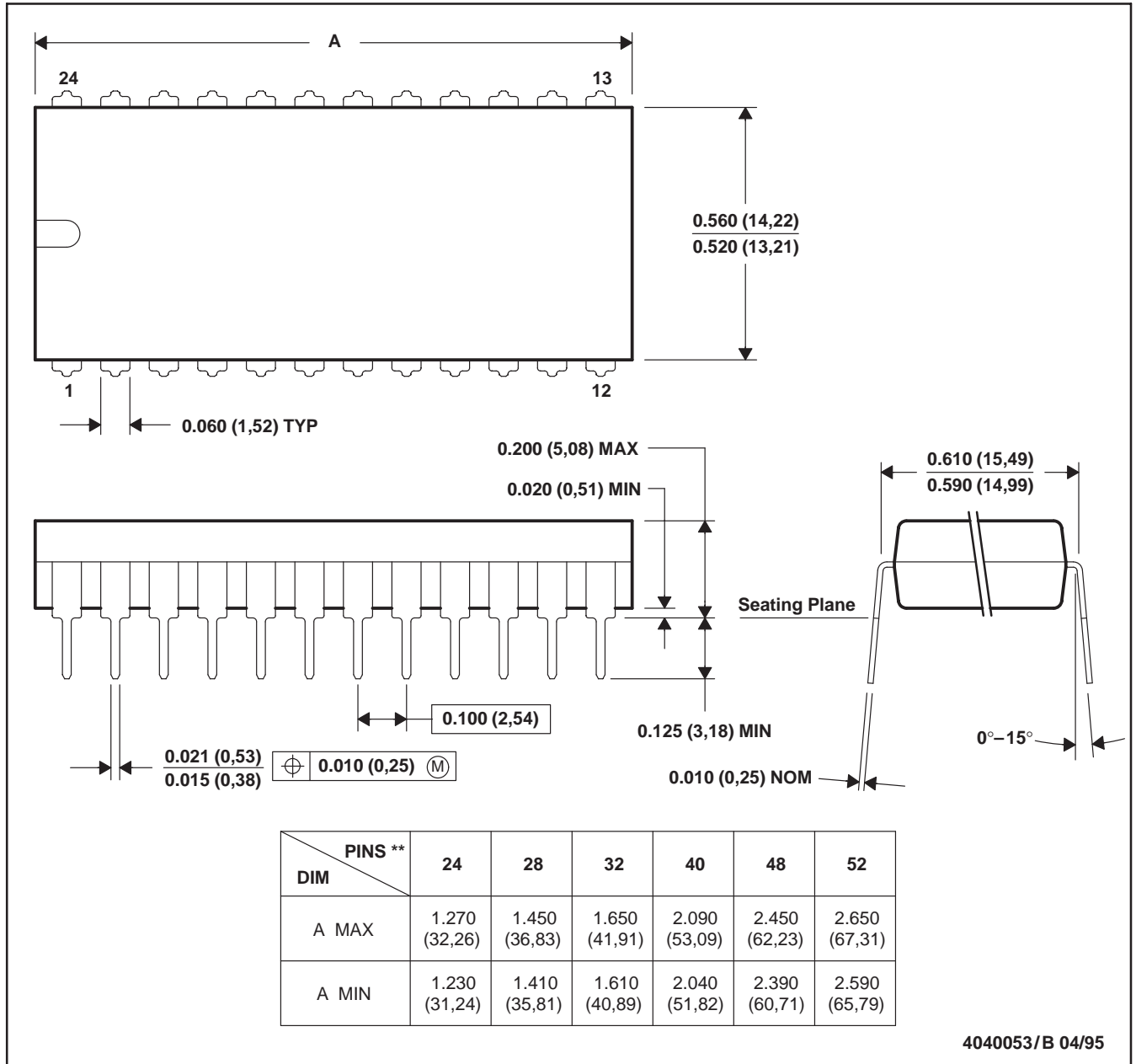
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**N (R-PDIP-T\*\*)**

**PLASTIC DUAL-IN-LINE PACKAGE**

24 PIN SHOWN

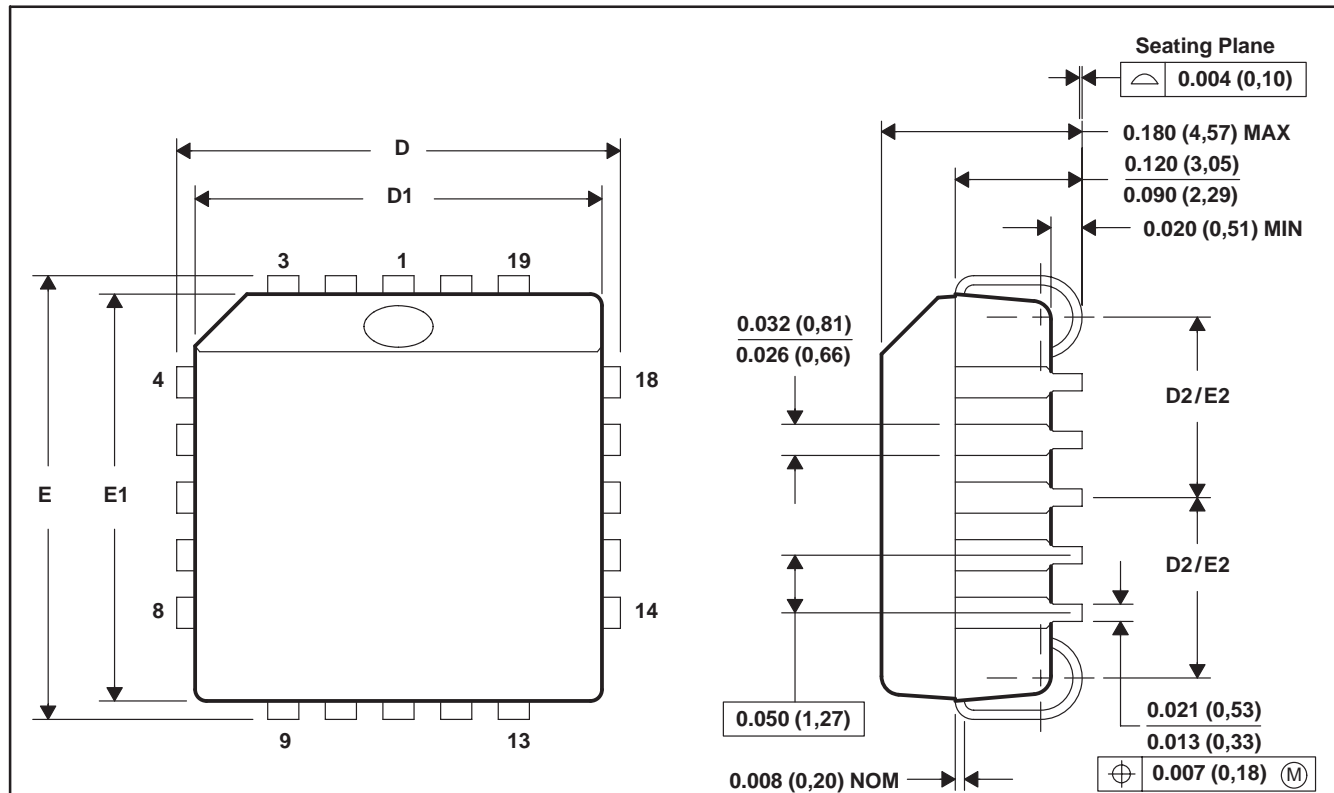


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-011  
 D. Falls within JEDEC MS-015 (32 pin only)

FN (S-PQCC-J\*\*)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

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- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-018

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