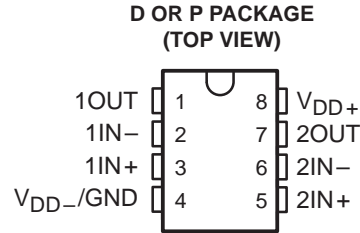


- Free-Air Operating Temperature  
–40°C to 150°C
- Output Swing Includes Both Supply Rails
- Low Noise . . . 9 nV/√Hz Typ at f = 1 kHz
- Low Input Bias Current . . . 1 pA Typ
- Common-Mode Input Voltage Range  
Includes Negative Rail
- High Unity-Gain Bandwidth . . . 2.2 MHz Typ
- High Slew Rate . . . 3.6 V/μs Typ
- Low Input Offset Voltage  
300 μV Typ at T<sub>A</sub> = 25°C
- Macromodel Included

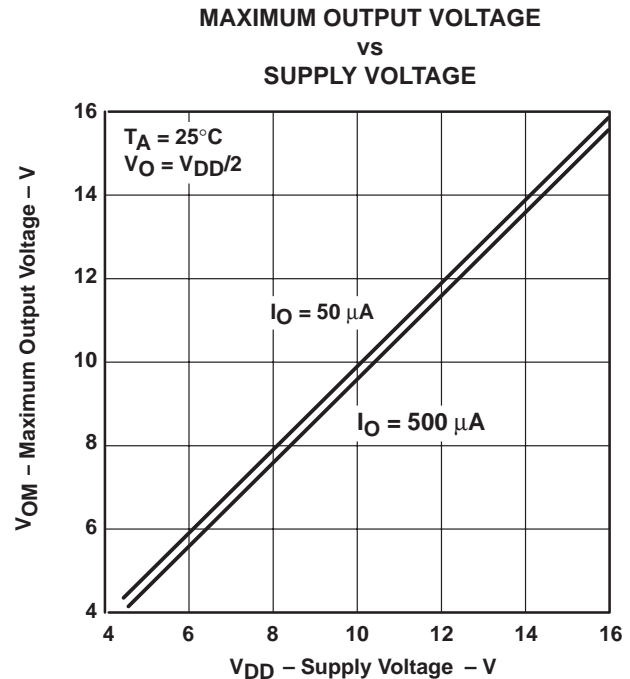


**description**

The TLC2872Z is a dual rail-to-rail output operational amplifier manufactured using Texas Instruments Advanced LinCMOS™ process. These devices offer comparable ac performance while having better noise, input offset voltage and power dissipation than existing CMOS operational amplifiers. In addition, the common-mode input voltage range is wider than typical standard CMOS type amplifiers. To take advantage of this improvement in performance, making this device available for a wider range of applications, V<sub>ICR</sub> is specified with a larger maximum input offset voltage test limit of ±5 mV. The Advanced LinCMOS™ process uses a silicon-gate technology to obtain input offset voltage stability with temperature and time that far exceeds that obtainable using metal-gate technology. Also, this technology makes possible input impedance levels that meet or exceed levels offered by top-gate JFET and expensive dielectric-isolated devices.

The TLC2872Z, manufactured using Texas Instruments high-temperature process flow, allows extended temperature operation up to 150°C in a plastic package. This adds extra reliability at the extended temperature and reduces the need for expensive hermetically sealed ceramic packages.

The TLC2872Z, which exhibits high input impedance and low noise, is excellent for small signal conditioning of high impedance sources, such as piezoelectric transducers. In addition, the rail-to-rail output feature with single or split supplies makes this device a great choice for inputs to ADCs in either the unipolar or bipolar mode of operation. This feature, combined with its temperature performance, makes the TLC2872Z ideal for sonobuoys, pressure sensors, temperature controls, active VR sensors, accelerometers, and many other applications.



**AVAILABLE OPTIONS**

T <sub>A</sub>	V <sub>IOmax</sub> AT 25°C	PACKAGED DEVICES		CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	
–40°C to 150°C	2.5 mV	TLC2872ZD	TLC2872ZP	TLC2872Y

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLC2872DR).

Advanced LinCMOS is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



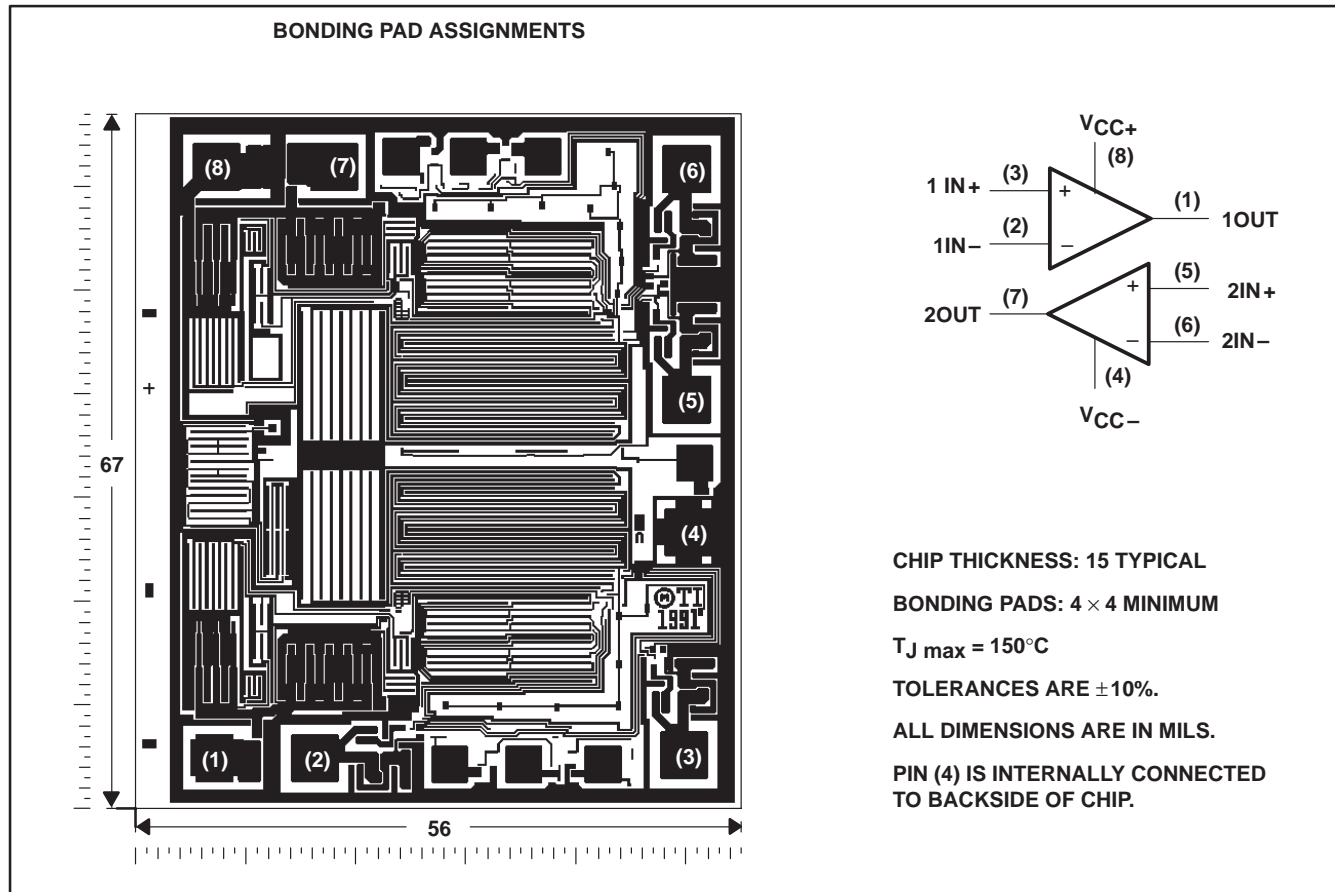
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**description (continued)**

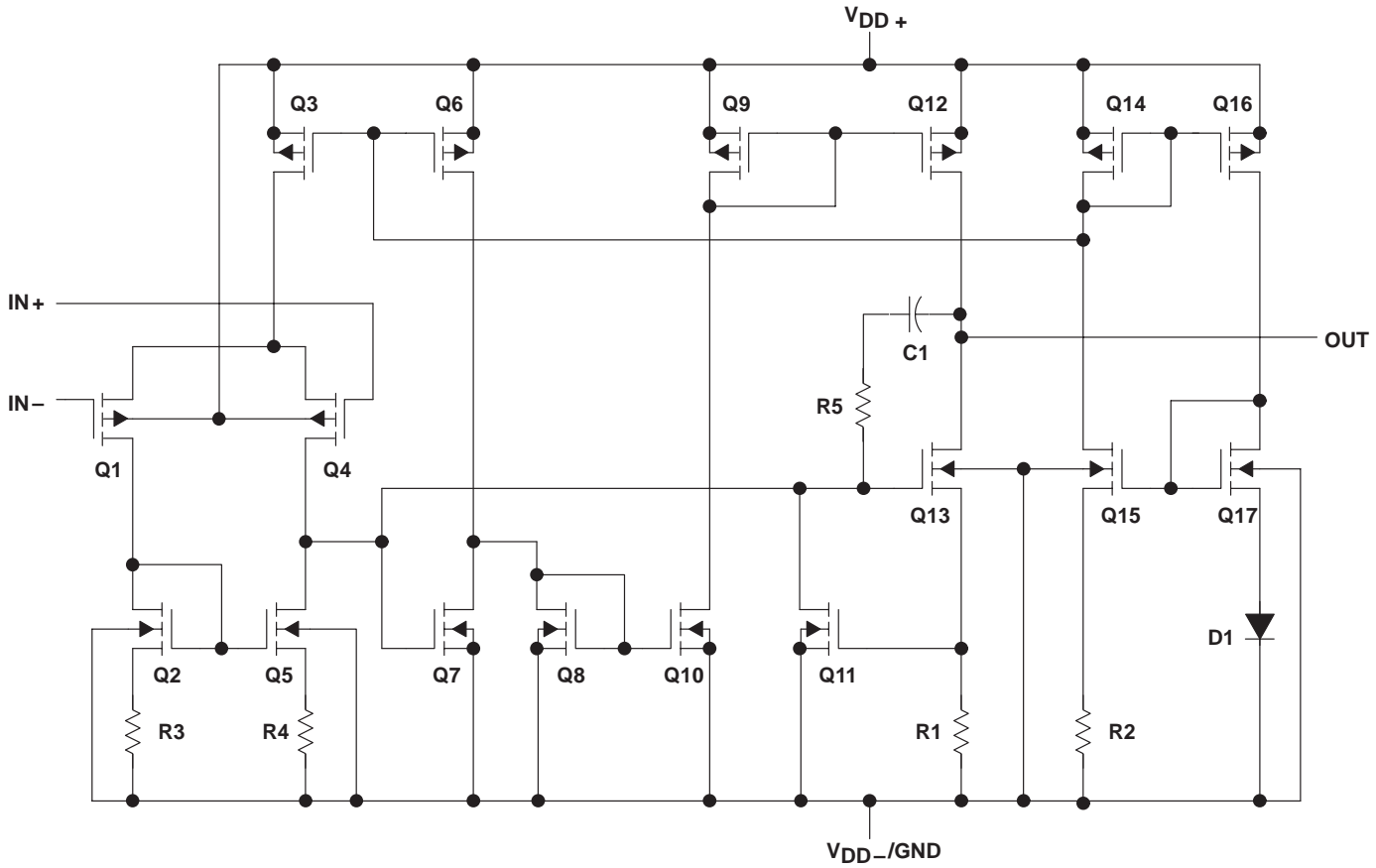
The inputs and outputs of this device are designed to withstand 100-mA surge current without sustaining latch-up. In addition, internal ESD-protection circuits prevent functional failures up to 2000 V. The device is characterized for operation over the extended (Z) temperature range of  $-40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ .

**TLC2872Y chip information**

This chip, when properly assembled, displays characteristics similar to TLC2872Z. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



equivalent schematic (each amplifier)



COMPONENT	COUNT†
Transistors	38
Diodes	9
Resistors	26
Capacitors	3

† Includes both amplifiers and all ESD, bias, and trim circuitry.

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage, $V_{DD+}$ .....	8 V
Supply voltage, $V_{DD-}$ .....	-8 V
Differential input voltage, $V_{ID}$ (see Note 1) .....	$\pm 16$ V
Input voltage range, $V_I$ (any input, see Note 2) .....	$\pm 8$ V
Input current, $I_I$ (each input) .....	$\pm 5$ mA
Output current, $I_O$ .....	$\pm 50$ mA
Total current into $V_{DD+}$ .....	$\pm 50$ mA
Total current out of $V_{DD-}$ .....	$\pm 50$ mA
Duration of short-circuit current at (or below) 25°C (see Note 3) .....	unlimited
Continuous total dissipation .....	See Dissipation Rating Table
Operating free-air temperature range, $T_A$ .....	-40°C to 150°C
Storage temperature range .....	-65°C to 165°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .....	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Differential voltages are at IN+ with respect to IN-. Excessive current will flow if input is brought below  $V_{DD-} - 0.3$  V.  
 2. All voltage values, except differential voltages, are with respect to the midpoint between  $V_{DD+}$  and  $V_{DD-}$ .  
 3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 105^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING	$T_A = 150^\circ\text{C}$ POWER RATING
D	812 mW	5.8 mW/°C	551 mW	348 mW	232 mW	87 mW
P	1120 mW	8 mW/°C	760 mW	480 mW	320 mW	120 mW

**recommended operating conditions**

	MIN	MAX	UNIT
Supply voltage, $V_{DD\pm}$	$\pm 2.2$	$\pm 8$	V
Input voltage range, $V_I$	$V_{DD-}$	$V_{DD+} - 1.5$	V
Common-mode input voltage, $V_{IC}$	$V_{DD-}$	$V_{DD+} - 1.5$	V
Operating free-air temperature, $T_A$	-40	150	°C



**electrical characteristics at specified free-air temperature,  $V_{DD} = 5\text{ V}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A$ †	TLC2872Z			UNIT
			MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_{DD} = \pm 2.5\text{ V}$ , $V_O = 0$ , $V_{IC} = 0$ , $R_S = 50\ \Omega$	25°C	300	2500	$\mu\text{V}$	
		Full range	3000			
$\alpha_{VIO}$ Temperature coefficient of input offset voltage		25°C to 150°C	2		$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)		25°C	0.002		$\mu\text{V}/\text{mo}$	
$I_{IO}$ Input offset current		25°C	0.0005		nA	
		Full range	3			
$I_{IB}$ Input bias current		25°C	0.001		nA	
		Full range	5			
$V_{ICR}$ Common-mode input voltage range	$R_S = 50\ \Omega$ , $ V_{IO}  \leq 5\text{ mV}$	25°C	0 to 4	-0.3 to 4.2	V	
		Full range	0 to 3.5			
$V_{OH}$ High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C	4.95	4.99	V	
		25°C	4.85	4.93		
		Full range	4.75			
		25°C	4.25	4.65		
$V_{OL}$ Low-level output voltage	$I_{OH} = -1\text{ mA}$	25°C	0.01	0.02	V	
		25°C	0.09	0.15		
		Full range	0.2			
		25°C	0.9	1.5		
$A_{VD}$ Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$ , $V_O = 1\text{ V to }4\text{ V}$	$R_L = 10\text{ k}\Omega$ ‡	25°C	15	35	V/mV
			Full range	10		
$r_{id}$ Differential input resistance			25°C	$10^{12}$		$\Omega$
$r_i$ Common-mode input resistance			25°C	$10^{12}$		$\Omega$
$c_i$ Common-mode input capacitance	$f = 10\text{ kHz}$ ,	P package	25°C	8		pF
$z_o$ Closed-loop output impedance	$f = 1\text{ MHz}$ ,	$A_V = 10$	25°C	140		$\Omega$
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.7\text{ V}$ , $R_S = 50\ \Omega$	$V_O = 2.5\text{ V}$	25°C	70	75	dB
			Full range	70		
$k_{SVR}$ Supply voltage rejection ratio ( $\Delta V_{DD}/\Delta V_{IO}$ )	$V_{DD} = 4.4\text{ V to }16\text{ V}$ , No load	$V_{IC} = V_{DD}/2$	25°C	80	95	dB
			Full range	80		
$I_{DD}$ Supply current	$V_O = 2.5\text{ V}$ , No load		25°C	2.2	3	mA
			Full range	3		

† Full range is  $-40^\circ\text{C}$  to  $150^\circ\text{C}$ .

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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**operating characteristics at specified free-air temperature,  $V_{DD} = 5\text{ V}$**

PARAMETER	TEST CONDITIONS	$T_A$ †	TLC2872Z			UNIT
			MIN	TYP	MAX	
SR Slew rate at unity gain	$V_O = 0.5\text{ V to }2.5\text{ V}, R_L = 10\text{ k}\Omega\ddagger, C_L = 100\text{ pF}\ddagger$	25°C	2.3	3.6		V/ $\mu\text{s}$
		Full range	1.1			
$V_n$ Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C	50			nV/ $\sqrt{\text{Hz}}$
	$f = 1\text{ kHz}$	25°C	9			
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ to }1\text{ Hz}$	25°C	1			$\mu\text{V}$
	$f = 0.1\text{ to }10\text{ Hz}$	25°C	1.4			
$I_n$ Equivalent input noise current		25°C	0.6			fA/ $\sqrt{\text{Hz}}$
THD + N Total harmonic distortion plus noise	$V_O = 0.5\text{ V to }2.5\text{ V}, f = 20\text{ kHz}, R_L = 10\text{ k}\Omega\ddagger$	25°C	$A_V = 1$	0.0013%		
			$A_V = 10$	0.004%		
			$A_V = 100$	0.03%		
Gain-bandwidth product	$f = 10\text{ kHz}, C_L = 100\text{ pF}\ddagger$	$R_L = 10\text{ k}\Omega\ddagger, 25^\circ\text{C}$	2.18			MHz
BOM Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V}, R_L = 10\text{ k}\Omega\ddagger,$	$A_V = 1, C_L = 100\text{ pF}\ddagger$	25°C	1		MHz
Settling time	$A_V = -1, \text{ Step} = 0.5\text{ V to }2.5\text{ V}, R_L = 10\text{ k}\Omega\ddagger, C_L = 100\text{ pF}\ddagger$	To 0.1%	25°C	1.5		$\mu\text{s}$
		To 0.01%		2.6		
$\phi_m$ Phase margin at unity gain	$R_L = 10\text{ k}\Omega\ddagger, C_L = 100\text{ pF}\ddagger$	25°C	50°			
Gain margin		25°C	10			dB

† Full range is  $-40^\circ\text{C}$  to  $150^\circ\text{C}$ .

‡ Referenced to 2.5 V



**electrical characteristics,  $V_{DD} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		TLC2872Y			UNIT
				MIN	TYP	MAX	
$V_{IO}$	Input offset voltage	$V_{IC} = 0,$ $R_S = 50\ \Omega$	$V_O = 0,$		300	2500	$\mu\text{V}$
	Input offset voltage long-term drift (see Note 4)				0.002		$\mu\text{V}/\text{mo}$
$I_{IO}$	Input offset current				0.0005		nA
$I_{IB}$	Input bias current			0.001		nA	
$V_{ICR}$	Common-mode input voltage range	$R_S = 50\ \Omega,$	$ V_{IO}  \leq 5\ \text{mV}$	0	-0.3		V
				to 4	to 4.2		
				0			
				to 3.5			
$V_{OH}$	High-level output voltage	$I_{OH} = -20\ \mu\text{A}$		4.95	4.99		V
		$I_{OH} = -200\ \mu\text{A}$		4.85	4.93		
		$I_{OH} = -1\ \text{mA}$		4.25	4.65		
$V_{OL}$	Low-level output voltage	$V_{IC} = 2.5\ \text{V}, I_{OL} = 50\ \mu\text{A}$		0.01	0.02		V
		$V_{IC} = 2.5\ \text{V}, I_{OL} = 500\ \mu\text{A}$		0.09	0.15		
		$V_{IC} = 2.5\ \text{V}, I_{OL} = 5\ \text{mA}$		0.9	1.5		
$A_{VD}$	Large-signal differential voltage amplification	$V_{IC} = 2.5\ \text{V},$ $V_O = 1\ \text{V to } 4\ \text{V}$	$R_L = 10\ \text{k}\Omega^\dagger$	15	35		V/mV
			$R_L = 1\ \text{M}\Omega^\dagger$		175		
$r_{id}$	Differential input resistance			$10^{12}$			$\Omega$
$r_i$	Common-mode input resistance			$10^{12}$			$\Omega$
$c_i$	Common-mode input capacitance	$f = 10\ \text{kHz},$	P package		8		pF
$z_o$	Closed-loop output impedance	$f = 1\ \text{MHz},$	$A_V = 10$		140		$\Omega$
CMRR	Common-mode rejection ratio	$V_{IC} = 0\ \text{to } 2.7\ \text{V},$ $R_S = 50\ \Omega$	$V_O = 2.5\ \text{V},$	70	75		dB
$k_{SVR}$	Supply voltage rejection ratio ( $\Delta V_{DD\pm} / \Delta V_{IO}$ )	$V_{DD} = 4.4\ \text{V to } 16\ \text{V},$ No load	$V_{IC} = V_{DD}/2,$	80	95		dB
$I_{DD}$	Supply current	$V_O = 2.5\ \text{V},$	No load		2.2	3	mA

$^\dagger$  Referenced to 2.5 V

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**operating characteristics,  $V_{DD} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$**

PARAMETER		TEST CONDITIONS		TLC2872Y			UNIT	
				MIN	TYP	MAX		
SR	Slew rate at unity gain	$V_O = 0.5\text{ V to }2.5\text{ V}$ , $R_L = 10\text{ k}\Omega^\dagger$ , $C_L = 100\text{ pF}^\dagger$		2.3	3.6		V/ $\mu\text{s}$	
$V_n$	Equivalent input noise voltage	$f = 10\text{ Hz}$		50			nV/ $\sqrt{\text{Hz}}$	
		$f = 1\text{ kHz}$		9				
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ to }1\text{ Hz}$		1			$\mu\text{V}$	
		$f = 0.1\text{ to }10\text{ Hz}$		1.4				
$I_n$	Equivalent input noise current			0.6			fA/ $\sqrt{\text{Hz}}$	
THD + N	Total harmonic distortion plus noise	$V_O = 0.5\text{ V to }2.5\text{ V}$ , $f = 20\text{ kHz}$ , $R_L = 10\text{ k}\Omega^\dagger$		$A_V = 1$				
				$A_V = 10$				0.0013%
				$A_V = 100$				0.004%
Gain-bandwidth product		$f = 10\text{ kHz}$ , $C_L = 100\text{ pF}^\dagger$		$R_L = 10\text{ k}\Omega^\dagger$		2.18	MHz	
BOM	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6\text{ V}$ , $R_L = 10\text{ k}\Omega^\dagger$		$A_V = 1$ , $C_L = 100\text{ pF}^\dagger$		1	MHz	
	Settling time	$A_V = -1$ , Step = $0.5\text{ V to }2.5\text{ V}$ , $R_L = 10\text{ k}\Omega^\dagger$ , $C_L = 100\text{ pF}^\dagger$		To 0.1%		1.5	$\mu\text{s}$	
				To 0.01%		2.6		
$\phi_m$	Phase margin at unity gain	$R_L = 10\text{ k}\Omega^\dagger$ , $C_L = 100\text{ pF}^\dagger$				50°		
	Gain margin					10	dB	

$^\dagger$  Referenced to 2.5 V





TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
$V_{IO}$	Input offset voltage	Distribution	1
$\alpha V_{IO}$	Input offset voltage temperature coefficient	Distribution	2
$I_{IB}/I_{IO}$	Input bias and offset currents	vs Free-air temperature	3
$V_I$	Input voltage range	vs Free-air temperature	4
$V_{OH}$	High-level output voltage	vs Output current	5
$V_{OL}$	Low-level output voltage	vs Output current	6, 7
$V_{OM}$	Maximum output voltage	vs Frequency	8
$I_{OS}$	Short-circuit output current	vs Supply voltage	9
		vs Free-air temperature	10
$A_{VD}$	Large-signal differential voltage amplification	vs Load resistance	11
		vs Frequency	12
		vs Free-air temperature	13
$I_{DD}$	Supply current	vs Supply voltage	14
		vs Free-air temperature	15
SR	Slew rate	vs Load capacitance	16
		vs Free-air temperature	17
$\phi_m$	Phase margin	vs Frequency	12
		vs Load capacitance	18
	Gain margin	vs Load capacitance	19

NOTE: All loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

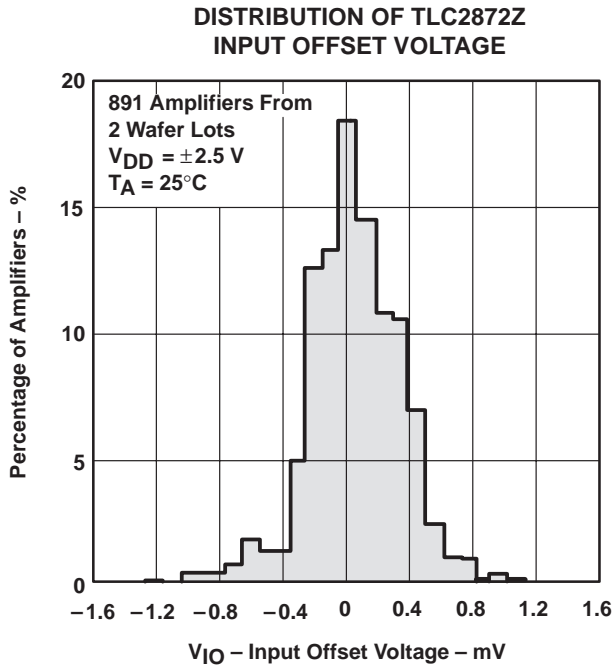


Figure 1

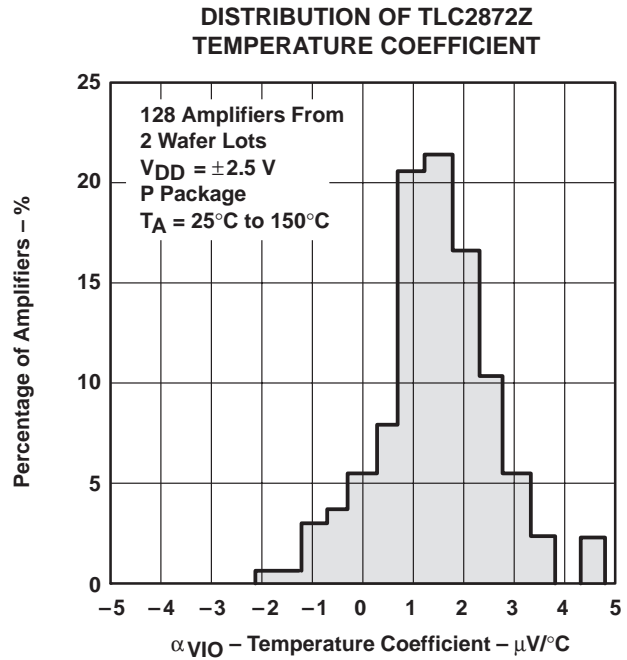


Figure 2

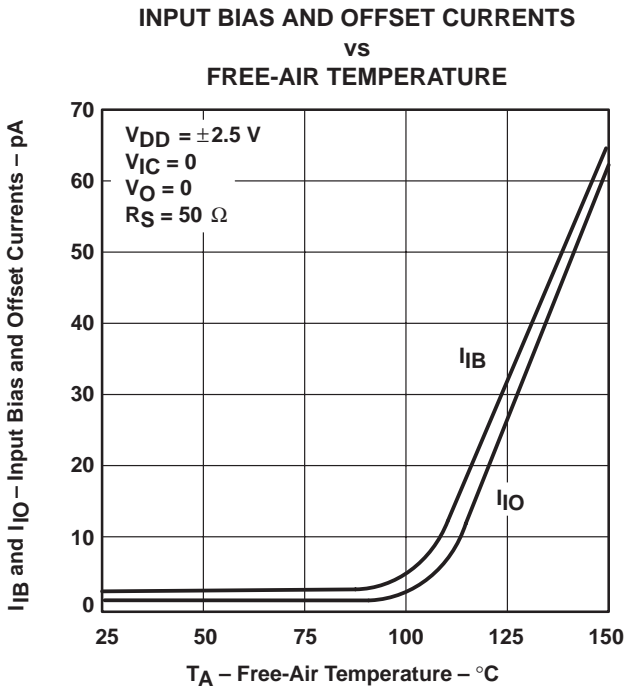


Figure 3

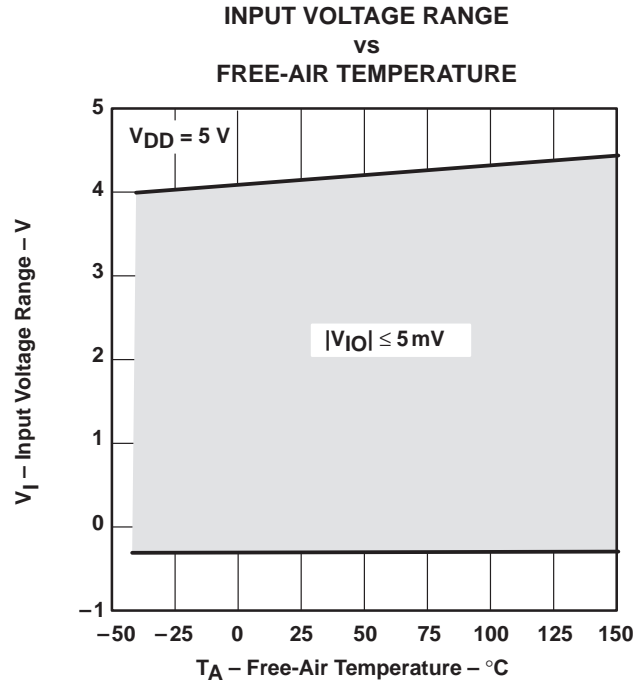


Figure 4

TYPICAL CHARACTERISTICS

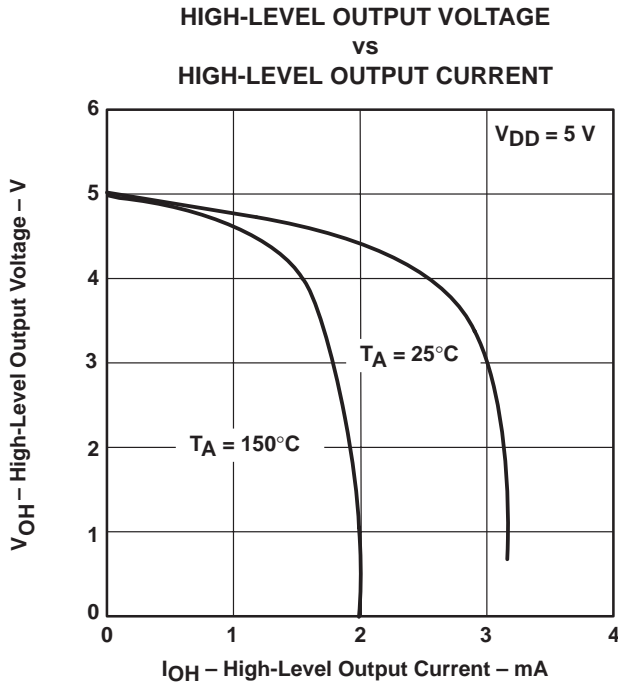


Figure 5

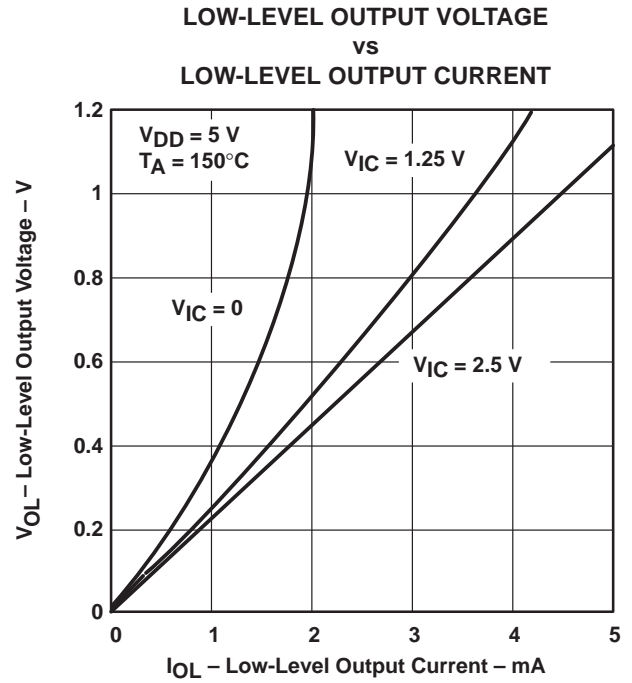


Figure 6

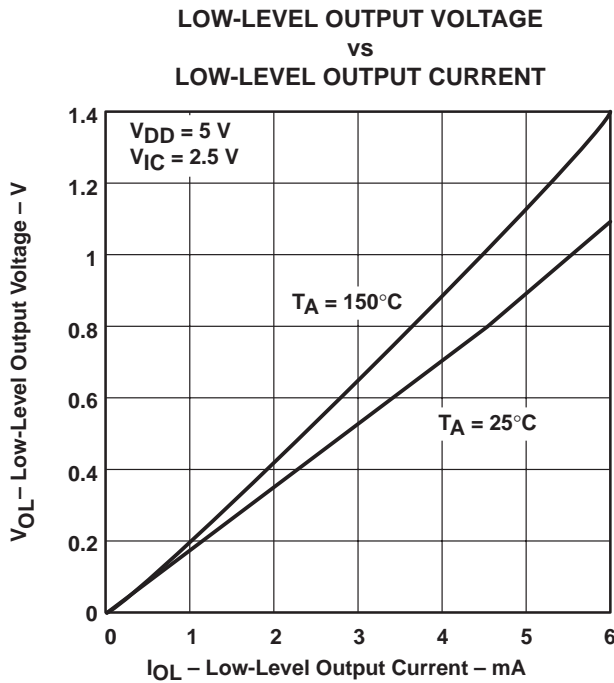


Figure 7

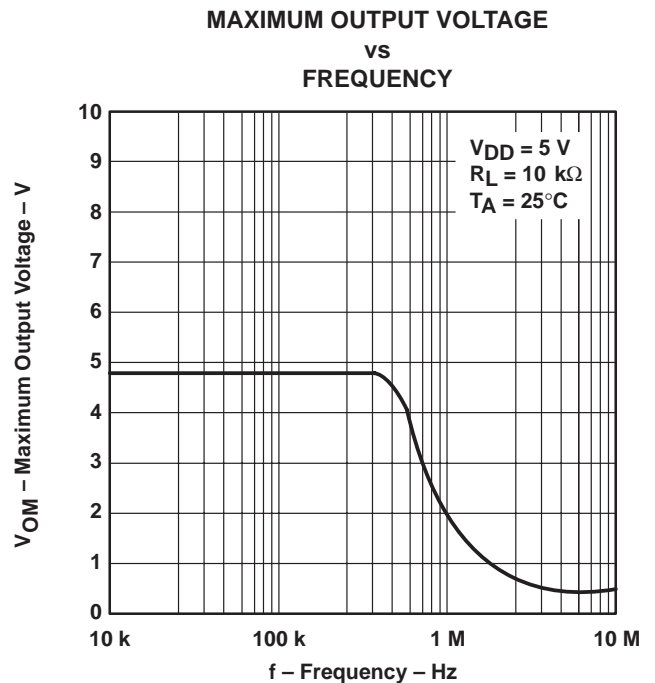


Figure 8

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT  
 vs  
 SUPPLY VOLTAGE

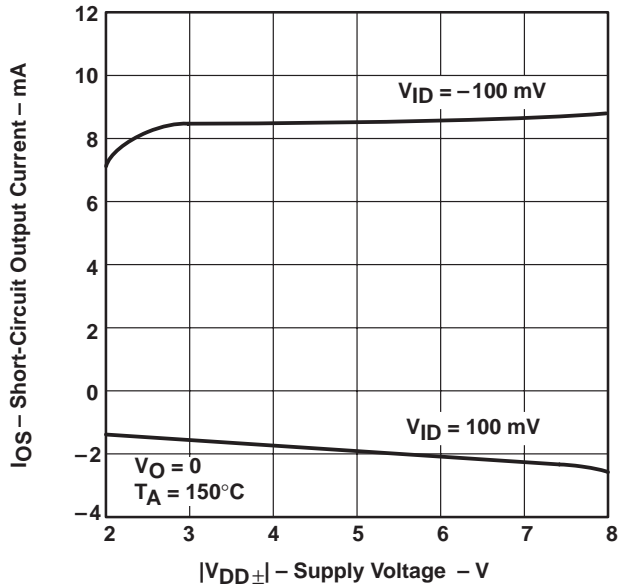


Figure 9

SHORT-CIRCUIT OUTPUT CURRENT  
 vs  
 FREE-AIR TEMPERATURE

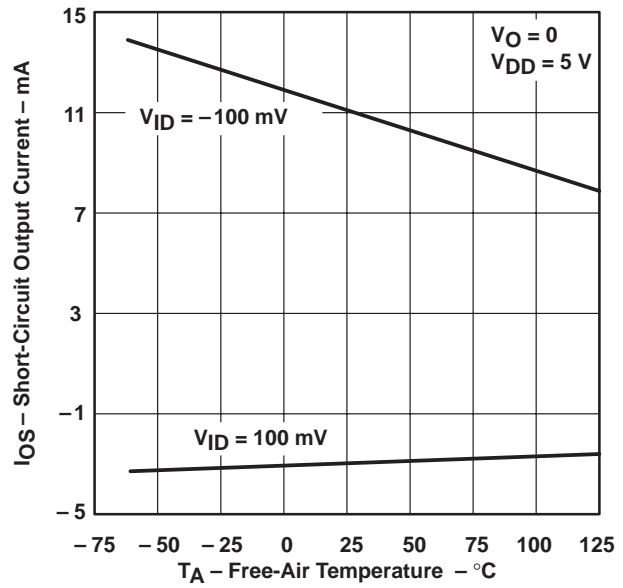


Figure 10

LARGE-SIGNAL DIFFERENTIAL  
 VOLTAGE AMPLIFICATION  
 vs  
 LOAD RESISTANCE

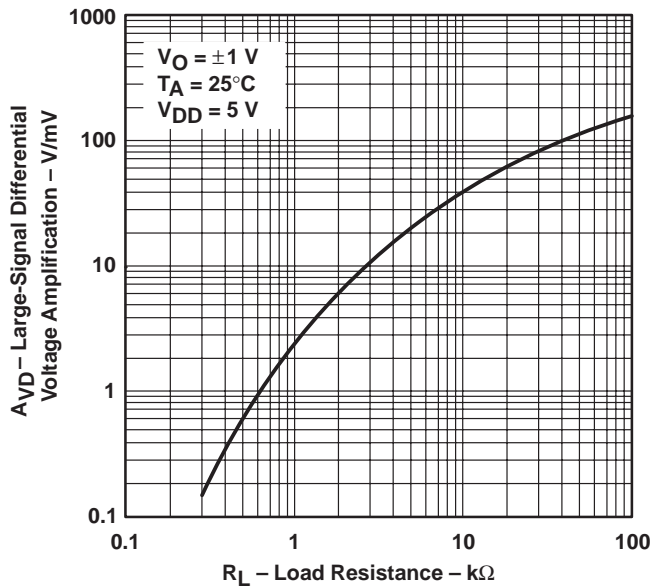


Figure 11

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE  
 AMPLIFICATION and PHASE MARGIN  
 vs  
 FREQUENCY

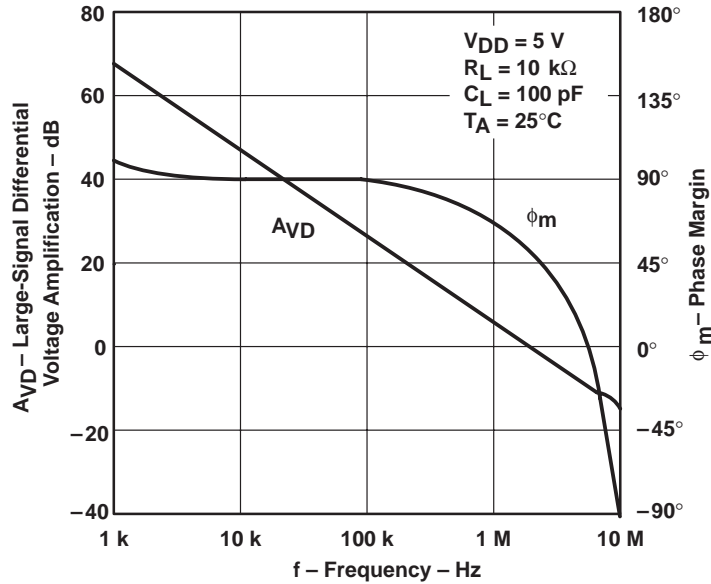


Figure 12

LARGE-SIGNAL DIFFERENTIAL  
 VOLTAGE AMPLIFICATION  
 vs  
 FREE-AIR TEMPERATURE

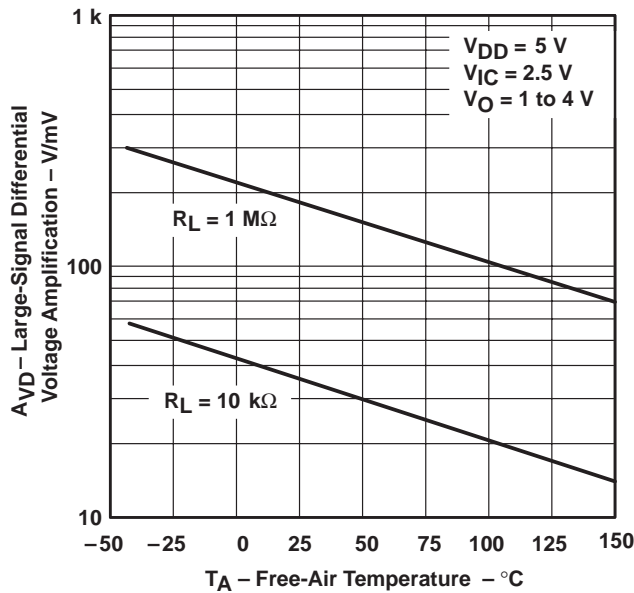


Figure 13

SUPPLY CURRENT  
 vs  
 SUPPLY VOLTAGE

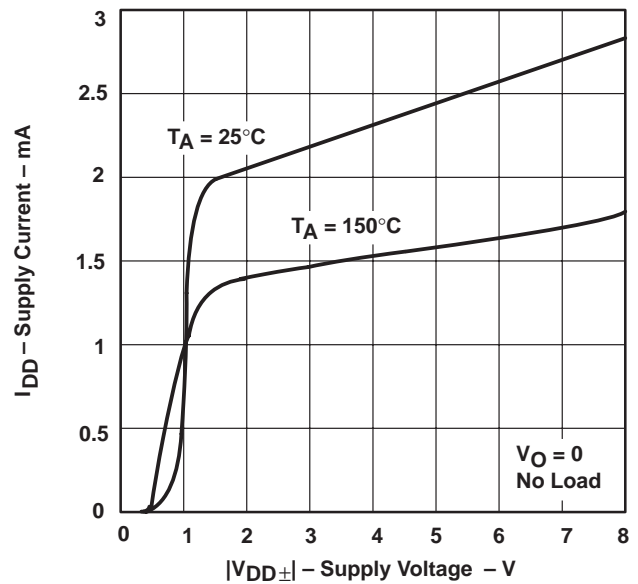
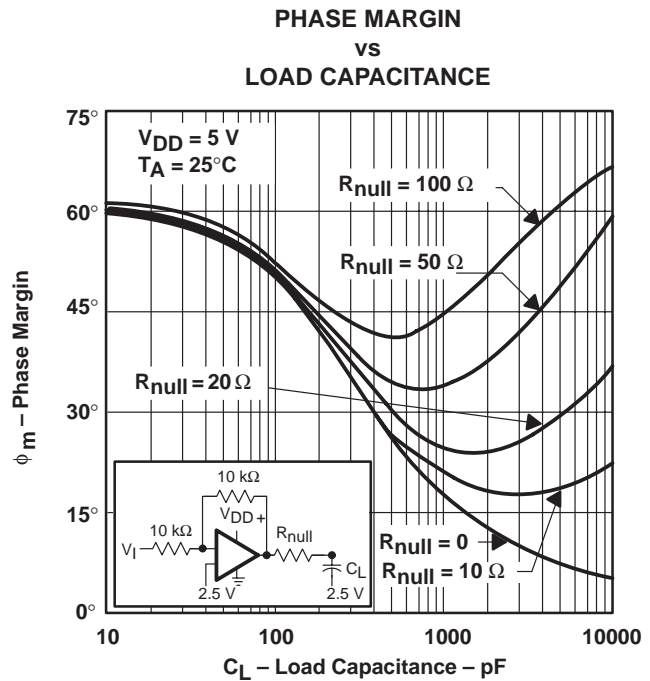
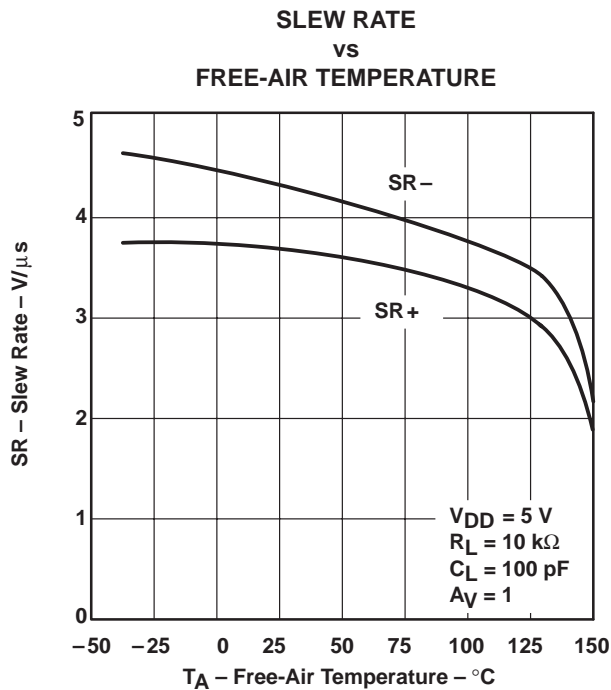
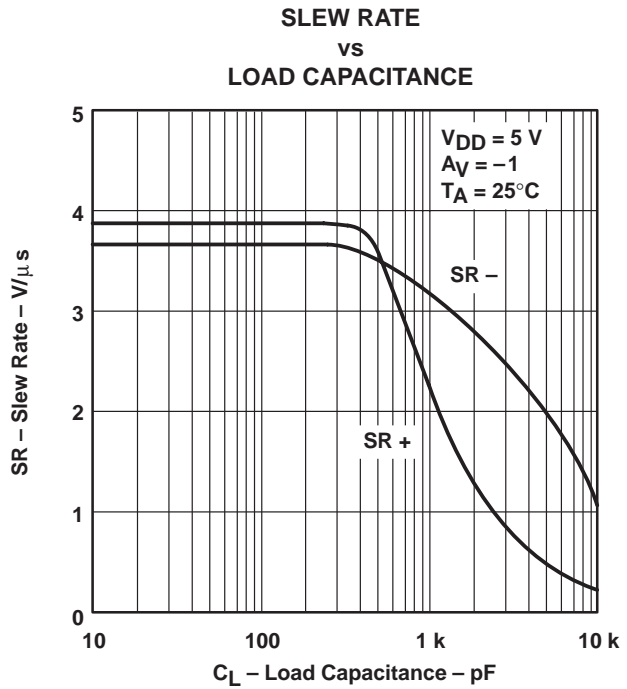
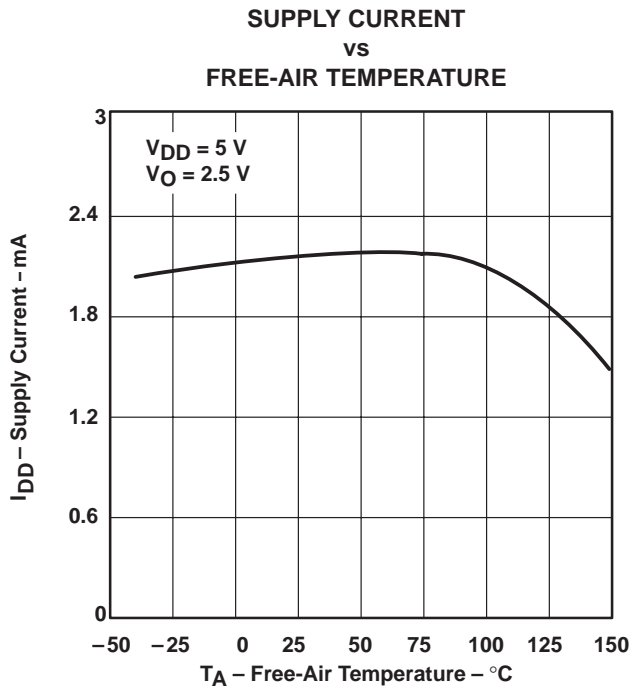


Figure 14

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS†

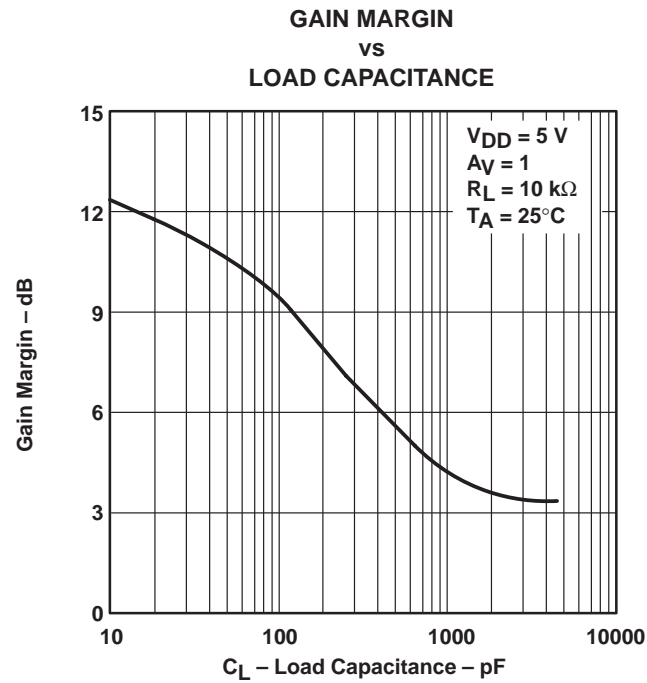


Figure 19

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

# TLC2872Z, TLC2872Y

## Advanced LinCMOS™ RAIL-TO-RAIL

### DUAL OPERATIONAL AMPLIFIERS

SLOS117 – OCTOBER 1992

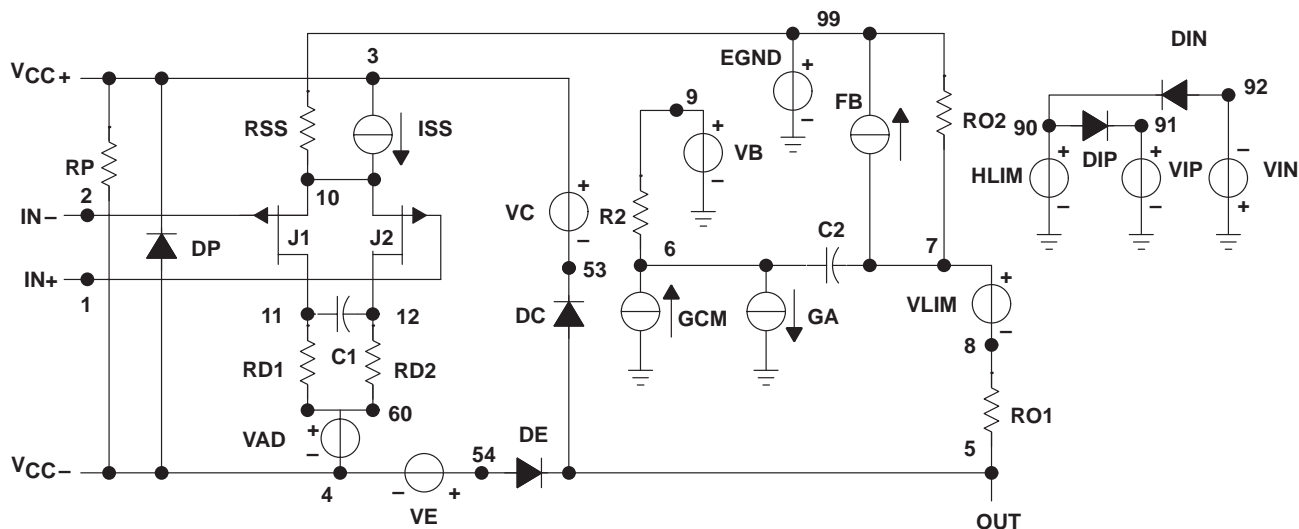
## APPLICATION INFORMATION

### macromodel information

Macromodel information provided was derived using *PSpice™ Parts™* model generation software. The Boyle macromodel (see Note 5) and subcircuit in Figure 20 were generated using the TLC2872Z typical electrical and operating characteristics at  $T_A = 25^\circ\text{C}$ . Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).



```
.SUBCKT TLC2872 1 2 3 4 5
C1 11 12 14E-12
C2 6 7 60.00E-12
DC 5 53 DX
DE 54 5 DX
DLP 90 91 DX
DLN 92 90 DX
DP 4 3 DX
EGND99 0 POLY (2) (3,0) (4,0) 0 .5 .5
FB 7 99 POLY (5) VB VC VE VLP VLN 0
+ 984.9E3 -1E6 1E6 1E6 -1E6
GA 6 0 11 12 377.0E-6
GCM 0 6 10 99 134E-9
ISS 3 10 DC 216.0E-6
HLIM 90 0 VLIM 1K
J1 11 12 10 JX
J2 12 1 10 JX
R2 6 9 100.OE3
RD1 60 11 2.653E3
RD2 60 12 2.653E3
R01 8 5 50
R02 7 99 50
RP 3 4 4.310E3
RSS 10 99 925.9E3
VAD 60 4 -.5
VB 9 0 DC 0
VC 3 53 DC .78
VE 54 4 DC .78
VLIM 7 8 DC 0
VLP 91 0 DC 1.9
VLN 0 92 DC 9.4
.MODEL DX D (IS=800.0E-18)
.MODEL JXPJF (IS=1.500E-12 BETA=1.316E3
+ VTO=-.270)
.ENDS
```

Figure 20. Boyle Macromodel and Subcircuit

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