TLC320AD56C
Data Manual

Sigma-Delta Analog Interface Circuit

SLAS101A
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1 Introduction

The TLC320AD56C provides high resolution low-speed signal conversion from digital-to-analog (D/A) and from analog-to-digital (A/D) using oversampling sigma-delta technology. This device consists of two serial synchronous conversion paths (one for each data direction) and includes an interpolation filter before the digital-to-analog converter (DAC) and a decimation filter after the analog-digital-converter (ADC) (see Figure 1–1). Other overhead functions provide on-chip timing and control. The sigma-delta architecture produces high resolution A/D and D/A conversion at low system speeds and low cost.

The options and the circuit configurations of this device can be programmed through the serial interface. The options include reset, power-down, communications protocol, serial clock rate, and test mode as outlined in Appendix A. The TLC320AD56C is characterized for operation from 0°C to 70°C.

1.1 Features

The TLC320AD56C includes the following features:

- Single 5-V power supply voltage or 5 V analog and 3 V digital supply voltages
- Power dissipation (P_D) of 150 mW maximum in the operating mode
- Power-down mode to 2.5 mW typical
- General-purpose 16-bit signal processing
- 2's-complement data format
- Typical dynamic range of 85 dB for the DAC and 87 dB for the ADC
- Minimum 79-dB total signal-to-(noise + distortion) for the ADC
- Minimum 80-dB total signal-to-(noise + distortion) for the DAC
- Differential architecture throughout the device
- Internal reference voltage (V_{ref})
- Internal 64X oversampling
- Serial port interface
- Phone-mode output control
- System test mode, digital loopback test mode
- Capable of supporting all V.34 sample rates by varying MCLK frequency
- Supports business audio applications
- Variable conversion rate selected as MCLK/512

1.2 Functional Block Diagram

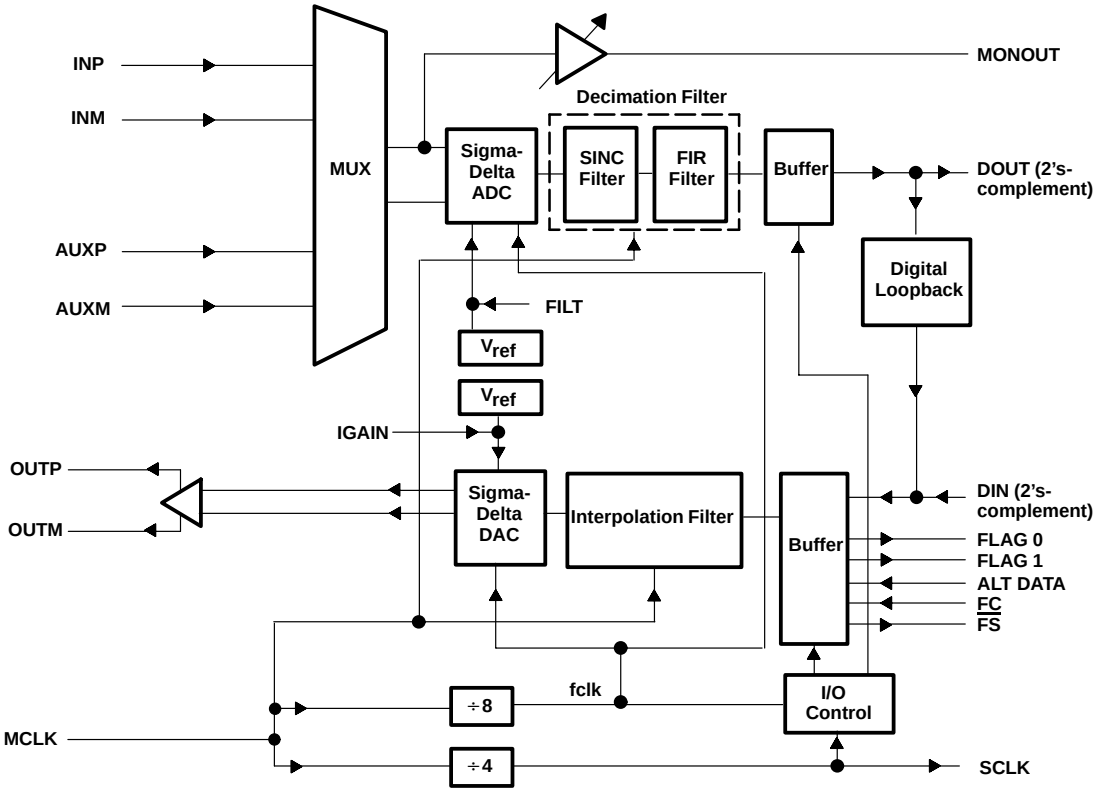
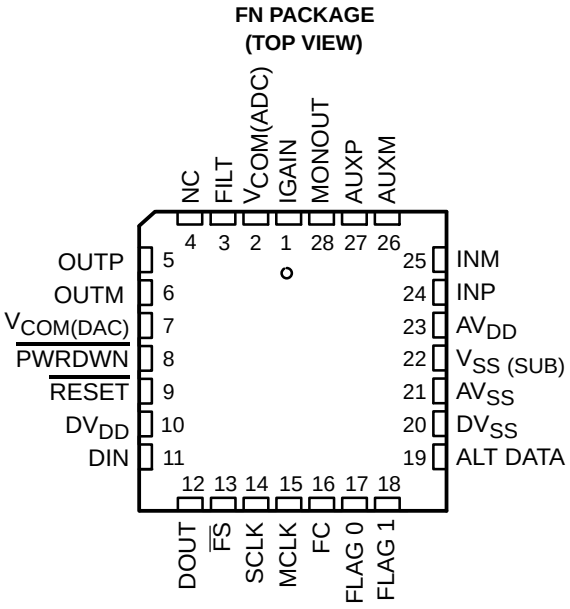


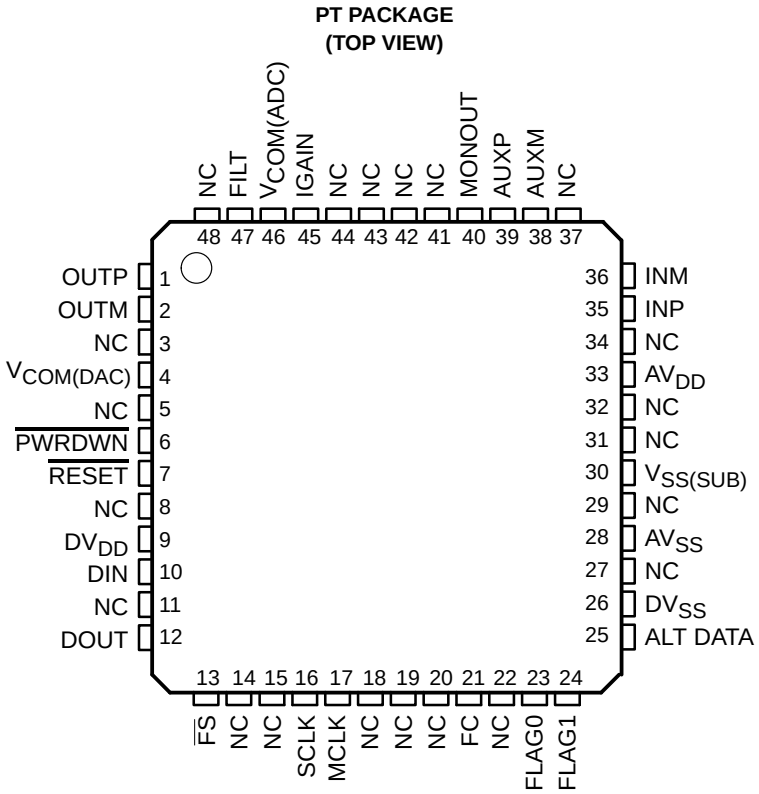
Figure 1–1. Functional Block Diagram

1.3 Terminal Assignments



NC – No internal connection

Figure 1–2. Terminal Assignments



NC – No internal connection

Figure 1–3. Terminal Assignments

1.4 Ordering Information

T_A	PACKAGE	
	CHIP CARRIER (FN)	QUAD FLAT PACK (PT)
0°C to 70°C	TLC320AD56CFN	TLC320AD56CPT

1.5 Terminal Functions

TERMINALS			I/O	DESCRIPTION
NAME	NUMBER			
	PT	FN		
ALT DATA	25	19	I	Signals on this terminal are routed to DOUT during secondary communication if phone mode is enabled.
AUXM	38	26	I	Inverting input to auxiliary analog input. AUXM requires an external RC antialias filter.
AUXP	39	27	I	Noninverting input to auxiliary analog input. Requires an external RC antialias filter.
AV_{DD}	33	23	I	Analog ADC path supply (5 V only)
DIN	10	11	I	Data input. DIN receives the DAC input data and command information from the DSP and is synchronized to SCLK.
DOUT	12	12	O	Data output. DOUT transmits the ADC output bits and is synchronized to SCLK. This terminal is at high-Z when $\overline{FS}$ is not activated.
DV_{DD}	9	10	I	Digital power supply (5 V or 3 V)
DV_{SS}	26	20	I	Digital ground
FC	21	16	I	Function code. FC is sampled and latched on the rising edge of $\overline{FS}$ for the primary serial communication. Refer to the Serial Communications section for more details.
FLAG 0	23	17	O	Output flag 0. During phone mode, FLAG 0 contains the value set in Control 2 register.
FLAG 1	24	18	O	Output flag 1. During phone mode, FLAG 1 contains the value set in Control 2 register.
FILT	47	3	O	Bandgap filter. FILT is provided for decoupling of the bandgap reference, and provides 2.5 V to which the analog inputs or outputs can be referenced. The optimal capacitor value is 0.1 μF (ceramic). This voltage node should be loaded only with a high-impedance dc load.
$\overline{FS}$	13	13	O	Frame sync. When $\overline{FS}$ goes low, the serial communication port is activated. In all serial transmission modes, $\overline{FS}$ is held low during bit transmission. Refer to section 3 *Serial Communications* for detailed description.
INM	36	25	I	Inverting input to analog modulator. INM requires an external RC antialias filter.
INP	35	24	I	Noninverting input to analog modulator. INP requires an external RC antialias filter.
IGAIN	45	1	O	Current gain reference scaling. IGAIN is provided for decoupling of the current gain reference and provides a 1.35-V reference. The optimal load is a 27-K resistor.
MCLK	17	15	I	Master clock. The master clock derives the internal clocks of the sigma-delta analog interface circuit.
MONOUT	40	28	O	Monitor output. MONOUT allows for monitoring of the analog input and is a high-impedance output. The gain or mute is selected using Control 2 register.
OUTM	2	6	O	Inverting current output of the DAC. OUTM is functionally identical with and complementary to OUTP. OUTM and OUTP current outputs can be loaded with 5 kΩ differentially or single-ended. This signal can also be used alone for single-ended operation.

NOTE 1: All digital inputs and outputs are TTL-compatible, unless otherwise noted for DV_{DD} = 5 V.

1.5 Terminal Functions (Continued)

TERMINALS			I/O	DESCRIPTION
NAME	NUMBER			
	PT	FN		
OUTP	1	5	O	Noninverting current output of the DAC. OUTM and OUTP current outputs can be loaded with 5 kΩ differentially or single ended. This signal can also be used alone for single-ended operation.
$\overline{\text{PWRDWN}}$	6	8	I	Power down. When this terminal is pulled low, the device goes into a power-down mode; the serial interface is disabled and most of the high-speed clocks are disabled. However, all the register values are sustained and the device resumes full power operation without reinitialization when this terminal is pulled high again. $\overline{\text{PWRDWN}}$ resets the counters only and preserves the programmed register contents. See subsection 2.21. *Reset and Power-Down Functions.*
$\overline{\text{RESET}}$	7	9	I	Reset. The reset function is provided to initialize all the internal registers to their default values. The serial port can be configured to the default state accordingly. Refer to section 1.7 *Register Functional Summary* and subsection 2.2.1 *Reset and Power-Down Functions* for more detailed descriptions.
SCLK	16	14	O	Shift clock. The shift clock signal is derived from MCLK and is used to clock serial data into DIN and out of DOUT.
$V_{SS(SUB)}$	30	22	I	Analog substrate. This terminal must be grounded.
$V_{COM(ADC)}$	46	2	O	Common mode filter. This terminal is provided for decoupling of the common mode reference and provides a 2.5 V reference. The optimal capacitor value is 0.10 μF. This node should be loaded only with a high-impedance dc load.
$V_{COM(DAC)}$	4	7	O	Common mode filter. This terminal is provided for decoupling of the common mode reference and provides a 2.5 V reference. The optimal capacitor value is 0.10 μF. This node should be loaded only with a high-impedance dc load.
AV_{SS}	28	21	I	Analog ground

NOTE 1: All digital inputs and outputs are TTL-compatible, unless otherwise noted for DV_{DD} = 5 V.

1.6 Definitions and Terminology

Data Transfer Interval This is time during which data is transferred from DOUT and to DIN. This interval is 16 shift clocks and this data transfer is initiated by the falling edge of the frame-sync signal.

Signal Data This refers to the input signal and all of the converted representations through the ADC channel and return through the DAC channel to the analog output. This is contrasted with the purely digital software control data.

Primary Communications This refers to the digital data transfer interval. Since the device is synchronous, the signal data words from the ADC channel and to the DAC channel occur simultaneously.

Secondary Communications This refers to the digital control and configuration data transfer interval into DIN and the register read data cycle from DOUT. The data transfer interval occurs when requested by hardware or software.

Frame Sync Frame sync refers only to the falling edge of the signal that initiates the data transfer interval. The primary frame sync starts the primary communications, and the secondary frame sync starts the secondary communications.

Frame Sync and Sampling Period	The time between the falling edges of successive primary frame-sync signals.
f_S	The sampling frequency that is the reciprocal of the sampling period.
Frame-Sync Interval	The time period occupied by 16 shift clocks. It goes high on the sixteenth rising edge of SCLK after the falling edge of the frame sync.
ADC Channel	This term refers to all signal processing circuits between the analog input and the digital conversion results at DOUT.
DAC Channel	This term refers to all signal processing circuits between the digital data word applied to DIN and the differential output analog signal available at OUTP and OUTM.
Host	Any processing system that interfaces to DIN, DOUT, SCLK, or $\overline{FS}$.
Dxx	Bit position in the primary data word (xx is the bit number).
DSxx	Bit position in the secondary data word (xx is the bit number).
d	The alpha character d represents valid programmed or default data in the control register format (see section 3.2 *Secondary Serial Communications*) when discussing other data bit portions of the register.
X	The alpha character X represents a do-not-care bit position within the control register format.
FIR	Finite duration impulse response.

1.7 Register Functional Summary

There are three data and control registers that are used as follows:

Register 0 The No-Op register. The 0 address allows secondary requests without altering any other register.

Register 1 The Control 1 register. The data in this register controls:

- The software reset
- The software power down
- Selection of the normal or auxiliary analog inputs
- Selection of the digital loopback
- 16-bit or 15-bit mode of operation
- Selection of monitor amp output

Register 2 The Control 2 register. The data in this register:

- Contains the output flag indicating a decimator FIR filter overflow
- Contains Flag 0 and Flag 1 output values for use in the phone mode
- Selects the phone mode

2 Functional Description

2.1 Device Functions

The functions of the TLC320AD56C are described in the following sections.

2.1.1 Operating Frequencies

The sampling (conversion) frequency is derived from the master clock (MCLK) input by equation 1.

$$f_S = \text{Sampling (conversion) frequency} = \frac{MCLK}{512} \quad (1)$$

The inverse is the time between the falling edges of two successive primary frame synchronization signals and is the conversion period.

2.1.2 ADC Signal Channel

To produce excellent common-mode rejection of unwanted signals, the analog signal is processed differentially until it is converted to digital data.

The input signal is filtered and applied to the ADC input. The ADC converts the signal into discrete output digital words in 2s-complement format, corresponding to the analog signal value at the sampling time. These 16-bit digital words, representing sampled values of the analog input signal, are clocked out of the serial port during the frame-sync interval, (DOUT), one word for each primary communication interval. During secondary communications, the data previously programmed into the registers can be read out with the appropriate register address, and the read bit set to 1. When no register read is requested, all 16 bits are 0 in the secondary word.

2.1.3 DAC Signal Channel

DIN receives the 16-bit serial data word (2's complement) from the host during the primary communications interval and latches the data on the seventeenth rising edge of SCLK. The data are converted to an analog current by the sigma-delta DAC comprised of a digital interpolation filter, and a digital 1-bit modulator. The DACs differential outputs OUTP and OUTM are a current output-type, (which requires resistive loading 5kΩ maximum). These outputs are then connected to the external low pass filter, as shown in the application schematics in Figure 3–7 and Figure 3–8 to complete the signal reconstruction. This filter can be incorporated in the data access arrangement (DAA) for modem applications.

2.1.4 Serial Interface

The digital serial interface consists of the shift clock, the frame synchronization signal, the ADC-channel data output, and the DAC-channel data input. During the primary 16-bit frame synchronization interval, the SCLK transfers the ADC channel results from DOUT and transfers 16-bit DAC data into DIN.

During the secondary frame synchronization interval, the SCLK transfers the register read data from DOUT when the read bit is set to a 1. In addition, the SCLK transfers control and device parameter information into DIN. The functional sequence is shown in Figure 3–1.

2.1.5 Register Programming

All register programming occurs during secondary communications, and data is latched and valid on the rising edge of the frame-sync signal. When the default value for a particular register is desired, that register does not need to be addressed during the secondary communications. The no-op command addresses the pseudo-register (register 0), and no register programming takes place during this communications.

DOUT is released from the high-impedance state on the falling edge of the primary or secondary frame-sync interval. In addition, each register can be read back during DOUT secondary communications by setting the read bit D13 to 1 in the appropriate register. When the register is in the read mode, no data can be written to the register during this cycle. To return this register to the write mode requires a subsequent secondary communication.

2.1.6 Sigma-Delta ADC

The sigma-delta ADC is a fourth-order sigma-delta modulator with 64 times oversampling. The ADC provides high resolution and low noise performance using oversampling techniques.

2.1.7 Decimation Filter

The decimation filter reduces the digital data rate to the sampling rate. This is accomplished by decimating with a ratio of 1:64. The output of this filter is a sixteen-bit 2's-complement data word clocking at the sample rate selected.

NOTE

The sample rate is determined through a relationship of MCLK/512.

2.1.8 Sigma-Delta DAC

The sigma-delta DAC is a fourth-order sigma-delta modulator with 64 times oversampling. The DAC provides high-resolution, low-noise performance from a 1-bit converter using oversampling techniques. The TLC320AD56C is a current-output DAC and requires a load resistor for current-to-voltage conversion (see Figures 3–7 and 3–8).

2.1.9 Interpolation Filter

The interpolation filter resamples the digital data at a rate of 64 times the incoming sample rate. The high-speed data output from this filter is then used in the sigma-delta DAC.

2.1.10 Digital Loopback

The digital loopback provides a means of testing the ADC/DAC channels and can be used for in-circuit system-level tests. The loopback feeds the ADC output to the DAC input on the IC.

Digital loopback is enabled by setting the appropriate bit in Control 1 register (see Appendix A).

2.1.11 FIR Overflow Flag

The decimator FIR filter provides an overflow flag to the Control 2 register to indicate that the input to the filter has exceeded the range of the internal filter calculations. When this bit is set in the register, it will remain set until the register is read by the user. Reading this value will always reset the overflow flag.

2.2 Terminal Functions

The terminal functions are described in the following sections.

2.2.1 Reset and Power-Down Functions

2.2.1.1 Reset

The TLC320AD56C resets the internal counters and registers, including the programmed registers, in one of two ways:

1. By applying a low-going reset pulse to the reset terminal
2. By writing to the programmable software reset bit (D07 in Control 1 register)

$\overline{\text{PWRDWN}}$ resets the counters only and preserves the programmed register contents. The $\overline{\text{PWRDWN}}$ terminal must be kept low 20 ms after the power supplies have settled.

2.2.1.2 Conditions of Reset

The two internal reset signals used for the reset and synchronization functions are:

1. Counter Reset – This signal resets all flip-flops and latches that are not externally programmed, with the exception of those generating the reset pulse itself. Additionally, this signal resets the software power-down bit. A counter reset is initiated with the $\overline{\text{RESET}}$ terminal or RESET bit or $\overline{\text{PWRDWN}}$ terminal.

2. Register Reset – This signal resets all flip-flops and latches that are not reset by the counter reset, except those generating the reset pulse itself. A register reset is initiated with the $\overline{\text{RESET}}$ terminal or RESET bit.

Both reset signals should be at least six master clock periods long, T_{RESET}, and should release on the trailing edge of the master clock.

2.2.1.3 Software and Hardware Power Down

Given the definitions above, the software programmed power-down condition is cleared by clearing the software bit (Control 1 register, bit 6) to a 0 or by cycling the power to the device or bringing $\overline{\text{RESET}}$ low.

The output of the monitor amplifier maintains its midpoint voltage during hardware and software power downs to minimize pops and clicks.

$\overline{\text{PWRDWN}}$ powers down the entire chip. Cycling the power-down terminal from high to low and back high resets all flip-flops and latches that are not externally programmed, thereby preserving the register contents.

When $\overline{\text{PWRDWN}}$ is not used, it should be tied high.

2.2.2 Master Clock Circuit

The clock circuit generates and distributes necessary clocks throughout the device. MCLK is the external master clock input. SCLK is derived from MCLK in order to provide clocking of the serial communications between the device and a digital signal processor (DSP). The sample rates of the data paths are set to MCLK/512.

2.2.3 Data Out (DOUT)

DOUT is taken from the high-impedance state by the falling edge of frame sync. The most significant data bit then appears on DOUT.

DOUT is placed in a high-impedance state on the sixteenth rising edge of SCLK after the falling edge of frame sync. In the primary communication, the data word is the ADC conversion result. In the secondary communication, the data is the register read results when requested by the read/write (R/$\overline{\text{W}}$) bit with the eight MSBs set to 0 (see Section 3 *Serial Communications*). If no register read is requested, the secondary word is all zeroes.

2.2.4 Data In (DIN)

In the primary communication, the data word is the input digital signal to the DAC channel. In the secondary communication, the data is the control and configuration data to set up the device for a particular function. (see section 3 *Serial Communications*).

2.2.5 Hardware Program Terminal (FC)

FC provides for hardware programming requests for secondary communication. It works in conjunction with the control bit D00 of the secondary data word. The signal on FC is latched 1/2 shift clock after the rising edge of the next internally generated primary frame-sync interval. The FC terminal should be tied low when not used (see Section 3.2 *Secondary Serial Communication* and Table 3–2).

2.2.6 Frame-Sync Function

The frame-sync signal indicates that the device is ready to send and receive data. The data transfer from DOUT and into DIN begins on the falling edge of the frame-sync signal.

The frame sync is generated internally and goes low on the rising edge of SCLK and remains low during the 16-bit data transfer.

2.2.7 Multiplexed Analog Input

The two differential analog inputs (INP and INM or AUXP and AUXM) are multiplexed into the sigma-delta modulator. The performance of the AUX channel is similar to the normal input channel. A simple RC antialiasing filter must be connected to AUXP and AUXM (also INP and INM when used).

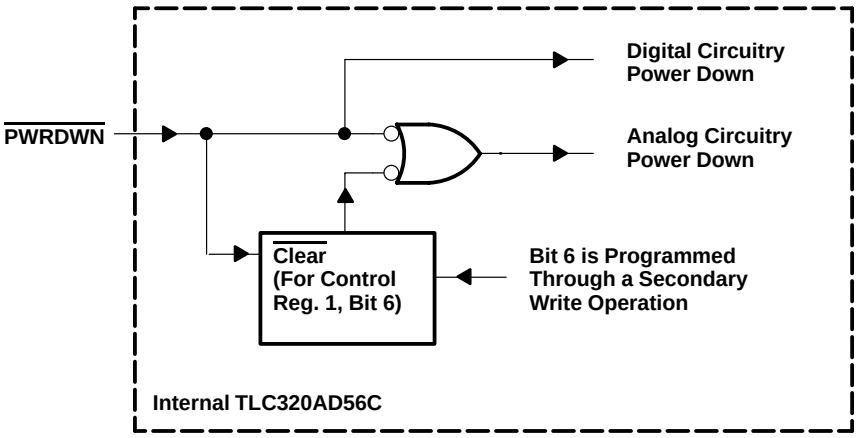


Figure 2–1. Internal Power-Down Logic

2.2.8 Analog Input

The signal applied to the terminals INM and INP (shown in Figure 2–2) should be differential to preserve the device specifications. A single-ended input signal should always be converted to a differential input signal prior to being used by the TLC320AD56C (see section 5 *Application Information*). The signal source driving the analog inputs (INM, INP, AUXM, AUXP) should have a low source impedance for lowest noise performance and accuracy. To obtain maximum dynamic range, the input signal should be centered at midsupply. A simple RC antialiasing filter must be connected to INP and INM (also AUXP and AUXM if used). A suitable tradeoff for the cutoff frequency (f_{CO}) of the antialiasing filter is $f_{CO} = 3 \times f_S$. With this cutoff frequency, the attenuation within the band of interest ($0 – f_S/2$) is less than 0.1 dB.

2.2.9 Analog Output

The analog output swing across the OUTP and OUTM terminals depends on the value of the resistor used from the IGAIN terminal to analog ground and the resistor load across the OUTP and OUTM terminals. Both resistors can be used to set the output voltage swing and then gained to the desired value in the external DAC output filter as shown in Figure 5–1 and Figure 5–2. With this external filter, the gain of the DAC channel is –2.5 dB.

The resistor on the IGAIN terminal sets up the output current pumped and the resistor across OUTP and OUTM is the load which converts the current output of the DAC to a voltage. Hence, the voltage swing across OUTP and OUTM depends on the ratio of the load resistor to the value of the resistor from the IGAIN terminal to analog ground. With 0 dB digital code applied to the DAC channel, the IGAIN resistor set at 27 kΩ, and a load resistor of 5 kΩ, the output swing across OUTP and OUTM is –10.5 dB. The ratio of IGAIN resistance to load resistance can be adjusted to get the desired voltage swing. For the best distortion performance, it is recommended that the output swing be limited to –6 dB relative to 6 V_{PP}.

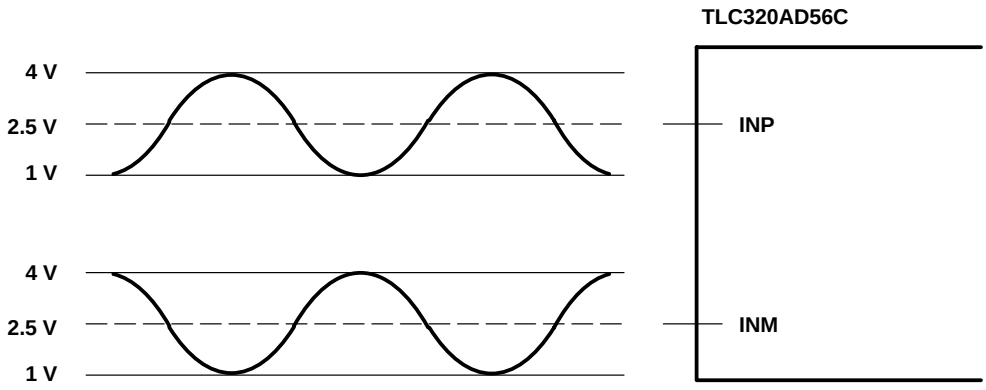


Figure 2–2. Differential Analog-Input Configuration

3 Serial Communications

DOUT, DIN, SCLK, $\overline{FS}$, and FC are the serial communication signals. The digital output data from the ADC is taken from DOUT. The digital input data for the DAC is applied to DIN. The synchronizing clock for the serial communication data and the frame sync is taken from SCLK. The frame synchronization pulse that encloses the ADC/DAC data transfer interval is taken from $\overline{FS}$. For an audio signal data transmitted from the ADC or to the DAC, primary serial communication is used. To read or write words that control both the options and the circuit configurations of the device, secondary communication is used.

The purpose of the primary and secondary communications is to allow conversion data and control data to be transferred across the same serial port. A primary transfer is always dedicated to conversion data. A secondary transfer is used to set up and read the register values described in Appendix A. A primary transfer occurs for every conversion period. A secondary transfer occurs only when requested. Two methods exist for requesting a secondary command. The FC terminal can be used to request a secondary communication by asserting it, or the least significant bit (LSB) of the DAC data within a primary transfer can request a secondary communication. The selection of which method is enabled is provided in Control 1 register (bit D0) as shown in Appendix A.

For all serial communications, the most significant bit (MSB) is transferred first. For a 16-bit ADC word and a 16-bit DAC word, D15 is the MSB and D0 is the LSB. For a 15-bit DAC data word in the 16-bit primary communication, D15 is the MSB, D1 is the LSB, and D0 is used for the embedded function control. All digital data values are in 2s-complement format.

These logic signals are compatible with TTL-voltage levels and CMOS current levels (when V_{DD} = 5 V dc). These logic signals are also compatible with a 3-V supply.

3.1 Primary Serial Communication

A primary serial communication transmits and receives conversion signal data. The ADC word length is always 16 bits. The DAC word length depends on the status of D0 in the Control 1 register. After power up or reset, the device defaults to a 15-bit mode (not 16-bit mode). The DAC word length is 15 bits and the last bit of the primary 16-bit serial communication word is a function control bit used to request secondary serial communications. In 16-bit mode, all 16 bits of the primary communications word are used as data for the DAC and the hardware terminal FC must be used to request secondary communications.

Figure 3–1 shows the timing relationship for SCLK, $\overline{FS}$, DOUT and DIN in a primary communication. The timing sequence for this operation is as follows:

1. $\overline{FS}$ is brought low by the TLC320AD56C.
2. One 16-bit word is transmitted from the ADC (DOUT) and one 16-bit word is received for the DAC (DIN).
3. $\overline{FS}$ is brought high by the TLC320AD56C signaling the end of the conversion.

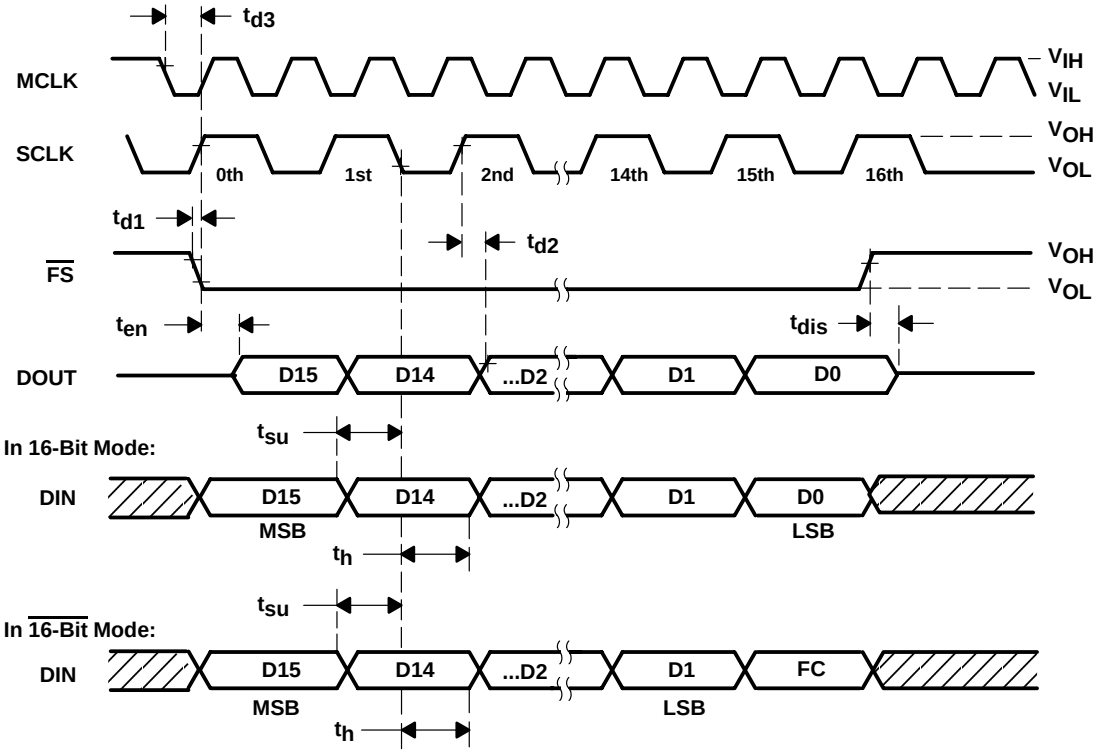


Figure 3–1. Primary Serial Communication Timing

When a secondary request is made through the LSB of the DAC data word ($\overline{16\text{-bit}}$ mode), the format in Table 3–1 is used.

Table 3–1. Secondary Request Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
← 15-bit DAC 2's-complement format →														↔ control	
← 16-bit ADC 2's-complement format →															

3.2 Secondary Serial Communication

Secondary serial communication is used to read or write 16-bit words that program both the options and the circuit configurations of the device. All register programming occurs during secondary communications. Two primary and secondary communication cycles are required to program the two registers. When the default value for a particular register is desired, then the user could omit addressing it during secondary communication. The NOOP command addresses a pseudo-register, register 0, and no register programming takes place during this secondary communication.

There are two methods for initiating secondary communications. They are 1) by asserting a high signal level on FC, or 2) by asserting the LSB of the DIN 16-bit serial communication high while not in 16-bit mode (see Control 1 register, bit 0).

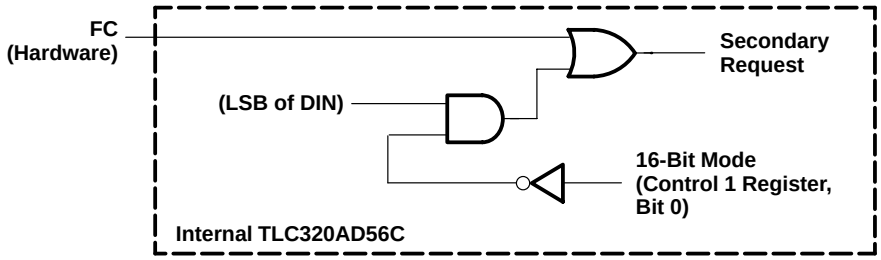


Figure 3–2. Hardware and Software Ways to Make a Secondary Request

1. Figures 3–3 and 3–4 show the two different ways FC requests secondary communication words as well as the timing for $\overline{FS}$, DOUT, DIN, and SCLK. The examples span two primary communication frames. Figure 3–3 shows the use of hardware function control.

   During a secondary communication, a register may be written to or read from. When writing a value to a register, the DIN line contains the value to be written. The data returned on DOUT is 00H. When performing a read function, the DIN line may still provide data to be written to an addressed register; however, the DOUT line contains the most recent value in the register addressed by DIN.

   In Figure 3–3, FC is clocked in and latched on the rising edge of frame sync ($\overline{FS}$). This causes the start of the secondary information 32 FCLKs after the start of the primary communication frame. Read and write examples are shown for DIN and DOUT.

2. Figure 3–4 shows the use of software function control.

   The software request is typically used when the required resolution of the DAC channel is less than 16 bits. Then the least significant bit (D0) can be used for the secondary requests as shown in Table 3–2.

Table 3–2. Least Significant Bit Control Function

Control Bit D0	Control Bit Function
0	No operation (NOOP)
1	Secondary communication request

On the falling edge of the next $\overline{FS}$, D15–D1 is input to DIN or D15–D0 is output to DOUT.

When a secondary communication request is made, $\overline{FS}$ goes low 32 FCLKs after the beginning of the primary frame.

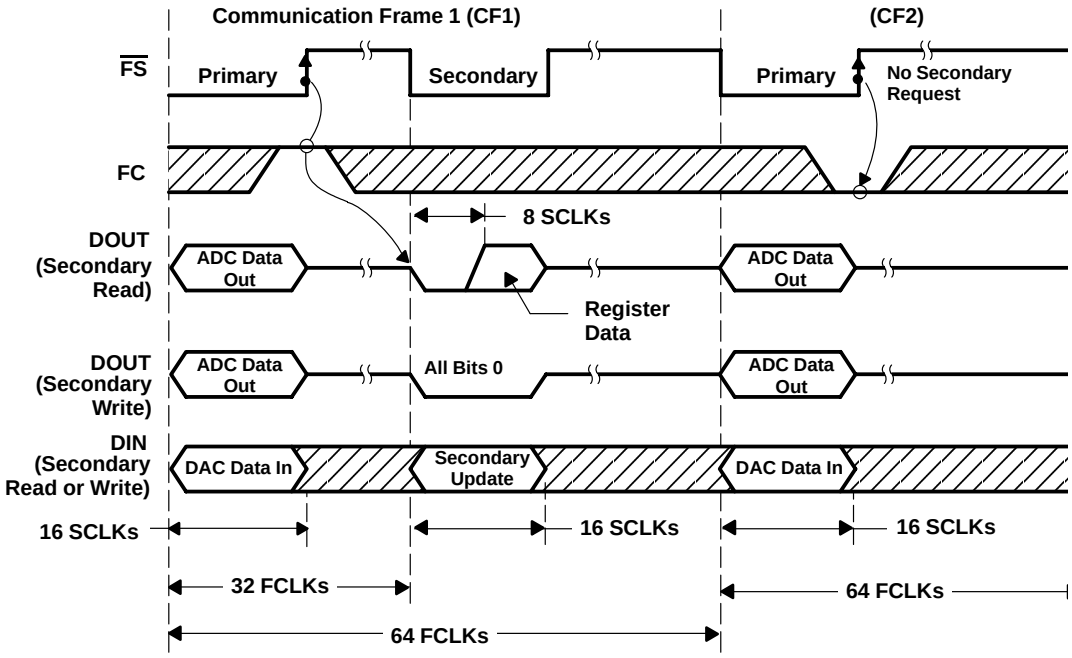
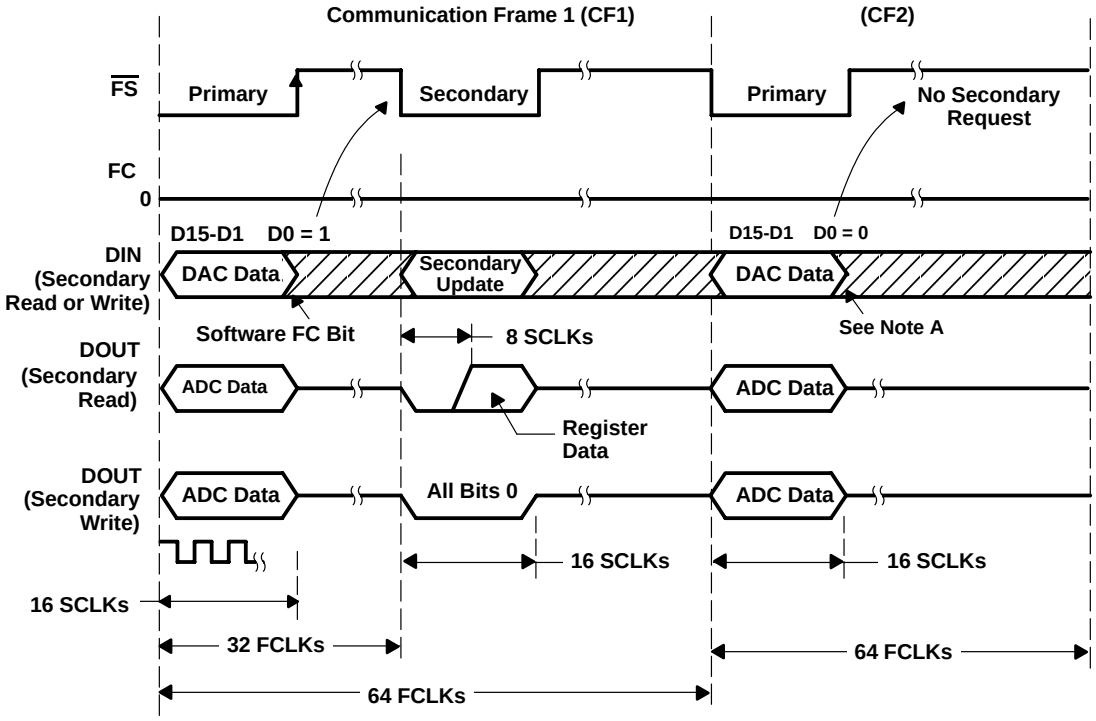


Figure 3–3. Hardware FC Secondary Request (Phone Mode Disabled)

In Figure 3–4, FC hardware terminal 15 is left in its unasserted state (0). FC is asserted through software by embedding an asserted high level (1) in the LSB of the 16-bit primary word. This is possible when not in 16-bit mode (Control 1 register, bit 2 = 0) because the user is using only 15 bits of DAC information.



NOTE A: For a read cycle, the last 8 bits are do-not-care bits.

Figure 3–4. Software FC Secondary Request (Phone Mode Disabled)

Table 3–3 shows the secondary communications format. D13 is the read/not-write (R/$\overline{W}$) bit.

D12–D8 are address bits. The register map is specified in the register set section in Appendix A. D7–D0 are data bits. The data bits are the new values for the specified register addressed by D12–D8.

Table 3–3. Secondary Communication Data Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
—	—	R/$\overline{W}$	A	A	A	A	A	D	D	D	D	D	D	D	D

3.3 Conversion Rate vs Serial Port

The SCLK frequency is set by the frequency of MCLK. There is a 2-stage clock divider that sets the SCLK frequency as MCLK/4.

3.4 Phone Mode Control

Phone mode control is provided for applications that need hardware control and monitoring of external events. By allowing the device to drive two FLAG terminals (set through the Control 2 register), the host (DSP) is capable of system control through the same serial port that connects to the device. Along with this control is the capability of monitoring the value of the ALT DATA terminal during a secondary communication cycle. One application for this function is in monitoring RING DETECT or OFFHOOK DETECT from a phone answering system. The two FLAG terminals allow response to these incoming control signals. Figure 3–6 shows the timing associated with this operating mode.

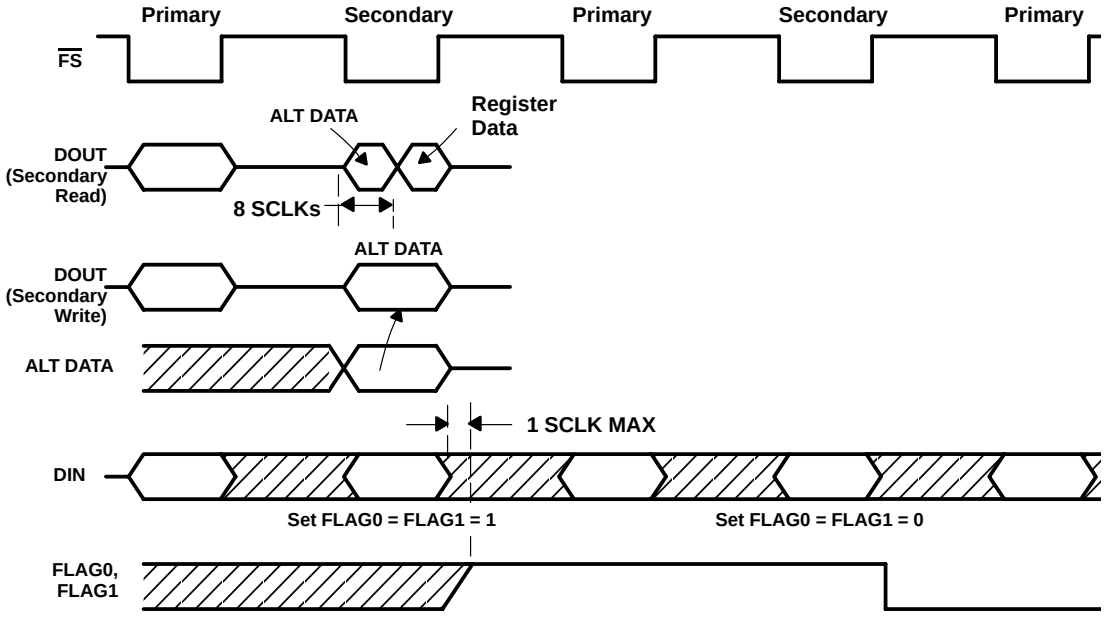


Figure 3–5. Phone Mode Timing

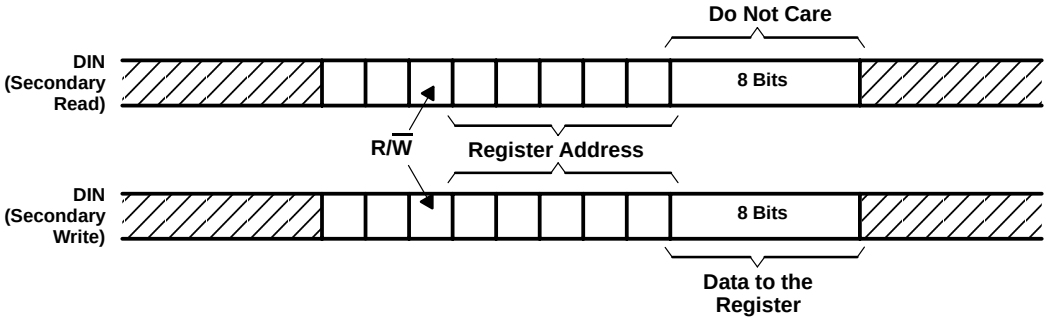


Figure 3–6. Secondary DIN Format

4 Specifications

4.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)†

Supply voltage range, DV_{DD}, AV_{DD} (see Note 1) . . . . . –0.3 V to 7 V
Output voltage range, DOUT, $\overline{FS}$, SCLK, FLAG0, FLAG1 . . . . –0.3 V to DV_{DD} + 0.3 V
Output voltage range, OUTP, OUTM . . . . . –0.3 V to V_{DD} + 0.3 V
Input voltage range, DIN, $\overline{PWRDWN}$, $\overline{RESET}$, ALT DATA, MCLK, FC . . . . . –0.3 V to DV_{DD} + 0.3 V
Input voltage range, INP, INM, AUXP, AUXM . . . . . –0.3 V to V_{DD} + 0.3 V
Case temperature for 10 seconds, T_C: DW package . . . . . 260°C
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

4.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, AV_{DD} (see Note 2)		4.75		5.25	V
Analog signal input voltage, $V_{I(analog)}$	Differential, (INP – INM) peak, for full scale operation			6	V
Resistance, IGAIN, $R_{(IGAIN)}$		20	27	54	kΩ
Load resistance, OUTP, OUTM, R_L			5/27 × $R_{(IGAIN)}$		kΩ
ADC or DAC conversion rate (sample rate)			8	22.05	kHz
Operating free-air temperature, T_A		0		70	°C

4.2.1 Recommended Operating Conditions, DV_{DD} = 5 V, AV_{DD} = 5 V

	MIN	NOM	MAX	UNIT
Supply voltage, DV_{DD} (see Note 2)	4.5		5.5	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
MCLK frequency (see Note 3)		4.096	11.29	MHz

4.2.2 Recommended Operating Conditions, DV_{DD} = 3 V, AV_{DD} = 5 V

	MIN	NOM	MAX	UNIT
Supply voltage, DV_{DD} (see Note 2)	2.7	3	3.3	V
High-level input voltage, V_{IH}	1.8			V
Low-level input voltage, V_{IL}			0.6	V
MCLK frequency (see Note 3)		4.096	11.29	MHz

NOTES: 2. Voltages at analog inputs and outputs and V_{DD} are with respect to the V_{SS} terminal.
3. The default state for an 8-kHz conversion rate requires a 4.096-MHz MCLK frequency.

4.3 Electrical Characteristics Over Recommended Operating Free-Air Temperature Range, DV_{DD} = 5 V, AV_{DD} = 5 V (Unless Otherwise Noted)

4.3.1 Digital Inputs and Outputs, MCLK = 4.096 MHz, f_S = 8 kHz, Outputs Not Loaded

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage, DOUT	I_O = 360 µA	2.4	4.6		V
V_{OL}	Low-level output voltage, DOUT	I_O = 2 mA		0.2	0.4	V
I_{IH}	High-level input current, any digital input	V_{IH} = 5 V			10	µA
I_{IL}	Low-level input current, any digital input	V_{IL} = 0.8 V			10	µA
C_i	Input capacitance			5		pF
C_o	Output capacitance			5		pF

4.3.2 Digital Inputs and Outputs, MCLK = 4.096 MHz, f_S = 8 kHz, Outputs Not Loaded, DV_{DD} = 3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage, DOUT	I_O = 360 µA	2			V
V_{OL}	Low-level output voltage, DOUT	I_O = 2 mA			0.4	V
I_{IH}	High-level input current, any digital input	V_{IH} = 3.3 V			10	µA
I_{IL}	Low-level input current, any digital input	V_{IL} = 0.6 V			10	µA
C_i	Input capacitance			5		pF
C_o	Output capacitance			5		pF

4.3.3 ADC Path Filter, MCLK = 4.096 MHz, f_S = 8 kHz (see Note 4)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Filter gain relative to gain at 1020 Hz	0 to 300 Hz	−0.5		0.2	dB
	300 Hz to 3 kHz	−0.35		0.2	
	3.3 kHz	−0.4		0.3	
	3.6 kHz			−3	
	4 kHz			−40	
	≥ 4.4 kHz			−74	

NOTE 4: The filter gain outside of the passband is measured with respect to the gain at 1020 Hz. The analog input test signal is a sine wave with 0 dB = 6 $V_{I(PP)}$ as the reference level for the analog input signal. The –1 dB pass band is 0 to 3400 Hz for an 8-kHz sample rate. This pass band scales linearly with the sample rate.

4.3.4 ADC Dynamic Performance, MCLK = 4.096 MHz, f_S = 8 kHz

4.3.4.1 ADC Signal-to-Noise (see Note 5)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-noise ratio (SNR)	V_I = −1 dB		86		dB
	V_I = −3 dB	80	84		
	V_I = −6 dB	76	81		
	V_I = −9 dB	73	78		
	V_I = −40 dB	42	47		
	V_I = −65 dB	17	22		
	V_{AUX} = −9 dB	73	78		

NOTE 5: The test condition is a 1020-Hz input signal with an 8-kHz conversion rate. Input and output voltages are referred to AV_{DD}/2.

4.3.4.2 ADC Signal-to-Distortion (see Note 5)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-total harmonic distortion (THD)	V_I = –1 dB		78		dB
	V_I = –3 dB	74	79		
	V_I = –6 dB	77	82		
	V_I = –9 dB	80	85		
	V_I = –40 dB	65	70		
	V_I = –65 dB	42	47		
	V_{AUX} = –9 dB	80	85		

NOTE 5: The test condition is a 1020-Hz input signal with an 8-kHz conversion rate. Input and output voltages are referred to $V_{DD}/2$.

4.3.4.3 ADC Signal-to-Distortion, DV_{DD} = 3 V (see Note 5)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-total harmonic distortion (THD)	V_I = –1 dB		79		dB
	V_I = –3 dB	90	95		
	V_I = –6 dB	92	100		
	V_I = –9 dB	94	103		
	V_I = –40 dB	68	76		
	V_I = –65 dB	42	52		
	V_{AUX} = –9 dB	94	103		

NOTE 5: The test condition is a 1020-Hz input signal with an 8-kHz conversion rate. Input and output voltages are referred to $V_{DD}/2$.

4.3.4.4 ADC Signal-to-Distortion+Noise (see Note 5)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Total harmonic distortion + noise (THD+N)	V_I = –1 dB		77		dB
	V_I = –3 dB	73	78		
	V_I = –6 dB	73	78		
	V_I = –9 dB	72	77		
	V_I = –40 dB	41	46		
	V_I = –65 dB	16	21		
	V_{AUX} = –9 dB	72	77		

NOTE 5: The test condition is a 1020-Hz input signal with an 8-kHz conversion rate. Input and output voltages are referred to $V_{DD}/2$.

4.3.4.5 ADC Signal-to-Distortion+Noise, DV_{DD} = 3 V (see Note 5)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Total harmonic distortion + noise (THD+N)	V_I = –1 dB		78		dB
	V_I = –3 dB	79	84		
	V_I = –6 dB	76	81		
	V_I = –9 dB	73	78		
	V_I = –40 dB	42	47		
	V_I = –65 dB	17	22		
	V_{AUX} = –9 dB	73	78		

NOTE 5: The test condition is a 1020-Hz input signal with an 8-kHz conversion rate. Input and output voltages are referred to $V_{DD}/2$.

4.3.5 ADC Channel

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{I(PP)}$	Peak-to-peak input voltage			6		V
	Dynamic range			87		dB
	Interchannel isolation			110		
E_G	Gain error	V_I = –1 dB at 1020 Hz		±0.3		
$E_{O(ADC)}$	ADC converter offset error			5		mV
CMRR	Common-mode rejection ratio at INM, INP or AUXM, AUXP	V_I = 0 dB at 1020 kHz		80		dB
	Idle channel noise (on-chip reference)			30	75	μV rms
R_i	Input resistance	T_A = 25°C		100		kΩ
	Channel delay			$17/f_S$		s

4.3.6 DAC Path Filter, MCLK = 8.192 MHz, f_S = 8 kHz (see Note 6)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Filter gain relative to gain at 1020 Hz	0 to 300 Hz	–0.5		0.2	dB
	300 Hz to 3 kHz	–0.25		0.25	
	3.3 kHz	–0.35		0.3	
	3.6 kHz			–3	
	4 kHz			–40	
	≥ 4.4 kHz			–74	

NOTE 6: The filter gain outside of the passband is measured with respect to the gain at 1020 Hz. The input signal is the digital equivalent of a sine wave (digital full scale = 0 dB). The nominal differential DAC channel output with this input condition is 6 $V_{I(PP)}$. The –1 dB pass band is 0 to 3400 Hz for an 8-kHz sample rate. This pass band scales linearly with the sample rate.

4.3.7 DAC Dynamic Performance, DV_{DD} = 5 V or 3 V

4.3.7.1 DAC Signal-to-Noise (see Note 7)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-noise ratio (SNR)	V_O = 0 dB	80	85		dB
	V_O = –9 dB	72	77		
	V_O = –40 dB	41	46		
	V_O = –65 dB	16	21		

NOTE 7: The test condition is the digital equivalent of a 1020-Hz input signal with an 8-kHz conversion rate. The test is measured at the output of a single pole RC filter with a cutoff frequency of 32 kHz. The test is conducted in 16-bit mode.

4.3.7.2 DAC Signal-to-Distortion (see Note 7)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-total harmonic distortion (THD)	V_O = 0 dB	86	92		dB
	V_O = –9 dB	90	96		
	V_O = –40 dB	60	66		
	V_O = –65 dB	40	46		

NOTE 7: The test condition is the digital equivalent of a 1020-Hz input signal with an 8-kHz conversion rate. The test is measured at the output of a single pole RC filter with a cutoff frequency of 32 kHz. The test is conducted in 16-bit mode.

4.3.7.3 DAC Signal-to-Distortion+Noise (see Note 7)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Total harmonic distortion + noise (THD+N)	V_O = 0 dB	80	84		dB
	V_O = –9 dB	72	76		
	V_O = –40 dB	41	45		
	V_O = –65 dB	16	20		

NOTE 7: The test condition is the digital equivalent of a 1020-Hz input signal with an 8-kHz conversion rate. The test is measured at the output of a single pole RC filter with a cutoff frequency of 32 kHz. The test is conducted in 16-bit mode.

4.3.8 DAC Channel, DV_{DD} = 5 V or 3 V

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Dynamic range				85		dB
	Interchannel isolation				108		
E_G	Gain error, 0 dB	V_O = 0 dB at 1020 Hz			±0.5		
	Idle channel broad-band noise	See Note 8			70	150	μV rms
	Idle channel narrow-band noise	0 – 4 kHz,	See Note 8		2	20	μV rms
	Channel delay				$18/f_S$		s
V_{OO}	Output offset voltage at OUT (differential)	DIN = zero code			2		mV
V_O	Analog output voltage, OUTP – OUTM	With internal reference and full-scale digital input, See Note 9	Differential		$\frac{9.6 \times R_{LOAD}}{R_{(IGAIN)}}$		V_{PP}

NOTES: 8. The conversion rate is 8 kHz; the out-of-band measurement is made from 4400 Hz to 3 MHz.
9. The digital input to the DAC channel at DIN is in 2's complement format. The TLC320AD56C is a current DAC and requires a load resistor for current-to-voltage conversion. This output voltage is across the load resistor (see Figures 5–1 and 5–2).

4.3.9 Power Supplies, No Load (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD} (analog)	Power supply current, ADC	Operating		18	25	mA
		Power down		0.5		mA
I_{DD} (digital1)	Power supply current, digital	Operating		2	5	mA
		Power down		3		μA
I_{DD} (digital2)	Power supply current, digital, DV_{DD} = 3.3 V	Operating		1		mA
		Power down		3		μA
P_D	Power dissipation	Operating		100	150	mW
		Power down		2.5	5	

4.3.10 Power-Supply Rejection (see Note 10)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{DD1}	Supply-voltage rejection ratio, ADC channel, DV_{DD}	f_i = 0 to 30 kHz		55		dB
V_{DD2}	Supply-voltage rejection ratio, DAC channel, DV_{DD}	f_i = 0 to 30 kHz		55		dB
V_{DD3}	Supply-voltage rejection ratio, ADC channel, AV_{DD}	f_i = 0 to 30 kHz		50		dB
V_{DD4}	Supply-voltage rejection ratio, DAC channel, AV_{DD}	Single ended, f_i = 0 to 30 kHz		50		dB
		Differential, f_i = 0 to 30 kHz		55		dB

† All typical values are at 25°C.

NOTE 10: Power supply rejection measurements are made with both the ADC and the DAC channels idle and a 200-mV peak-to-peak signal applied to the appropriate supply.

4.3.11 Timing Requirements (see Figure 3–1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d1}	Delay time, SCLK↑ to $\overline{FS}$↓	C_L = 20 pF			0	ns
t_{d2}	Delay time, SCLK↑ to DOUT valid				20	
t_{su}	DIN setup time before SCLK low		20			
t_h	DIN hold time after SCLK high				20	
t_{en}	Enable time, $\overline{FS}$↓ to DOUT valid				25	
t_{dis}	Disable time, $\overline{FS}$↑ to DOUT Hi-Z			20		
t_{d3}	Delay time, MCLK↓ to SCLK↑				50	
t_{wH}	Pulse duration, MCLK high		32			
t_{wL}	Pulse duration, MCLK low		20			

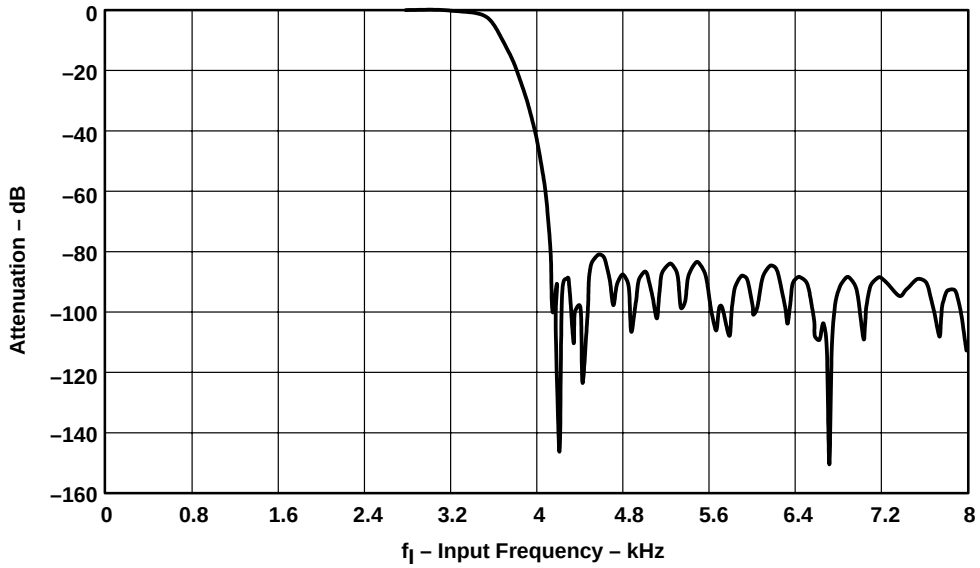


Figure 4–1. ADC Decimation Filter Response

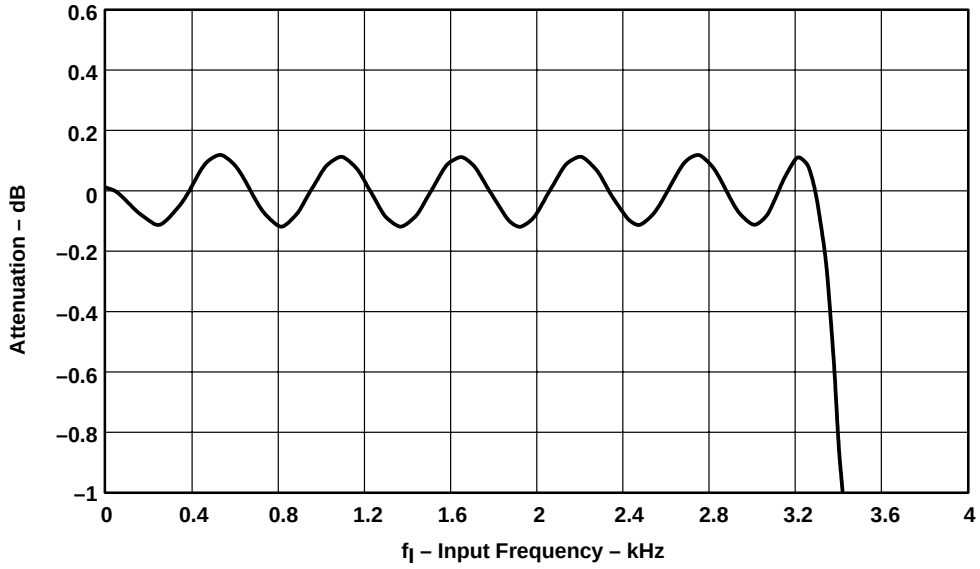


Figure 4–2. ADC Decimation Passband Ripple

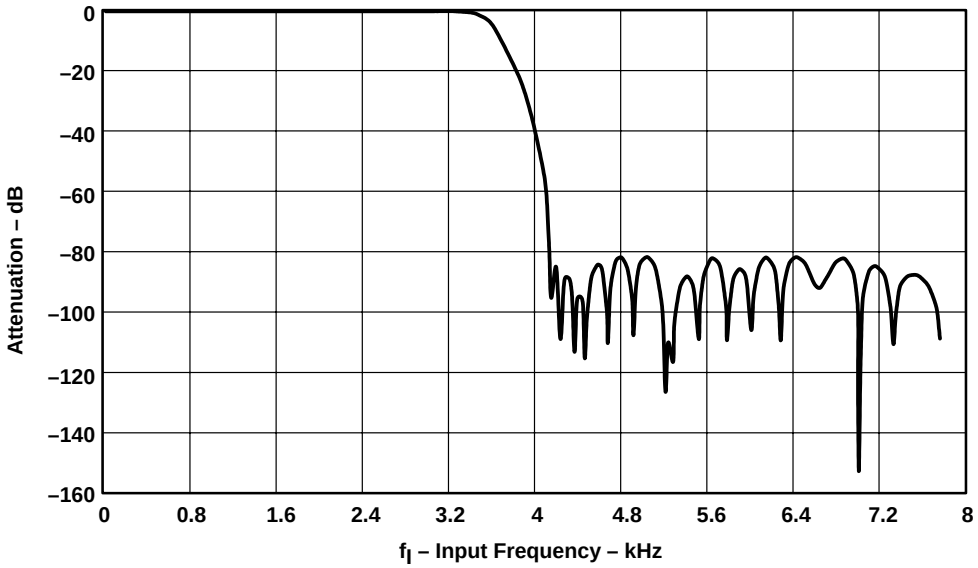


Figure 4–3. DAC Interpolation Filter Response

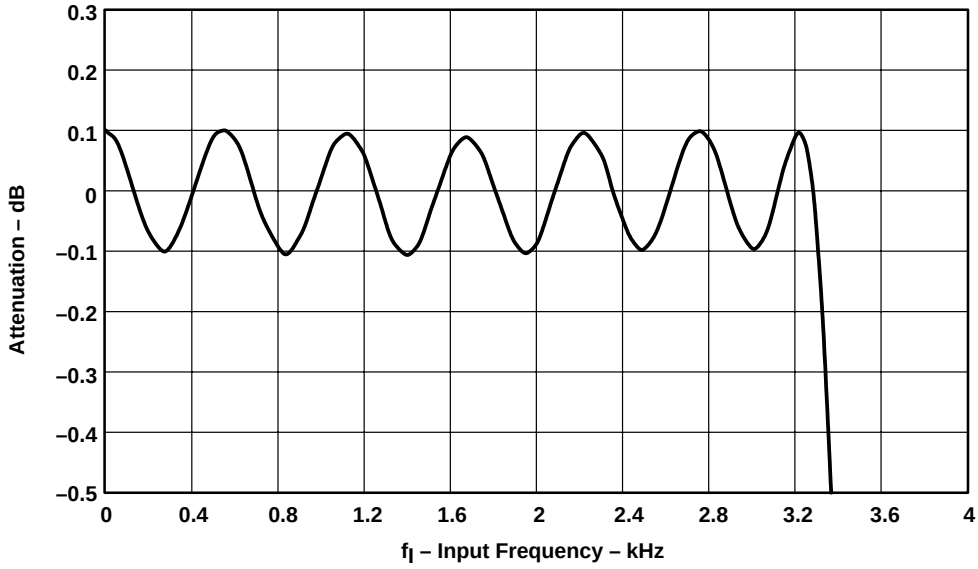


Figure 4–4. DAC Interpolation Passband Ripple

5 Application Information

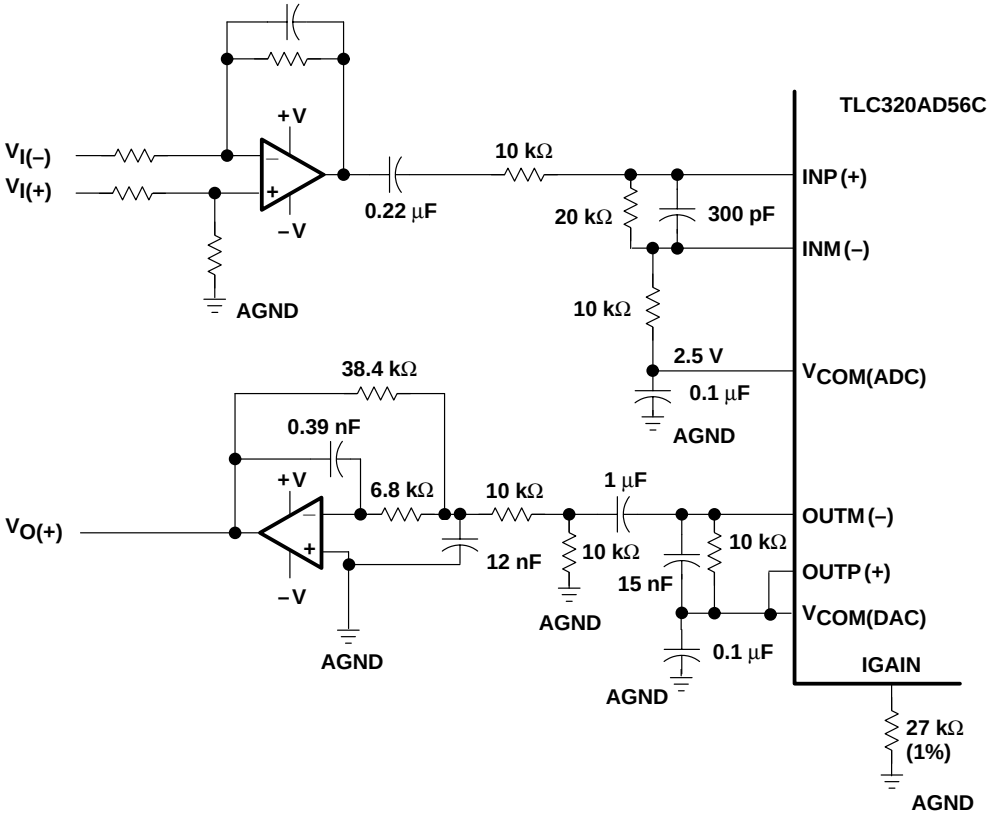


Figure 5–1. Application Schematic For Single-Ended Input/Output

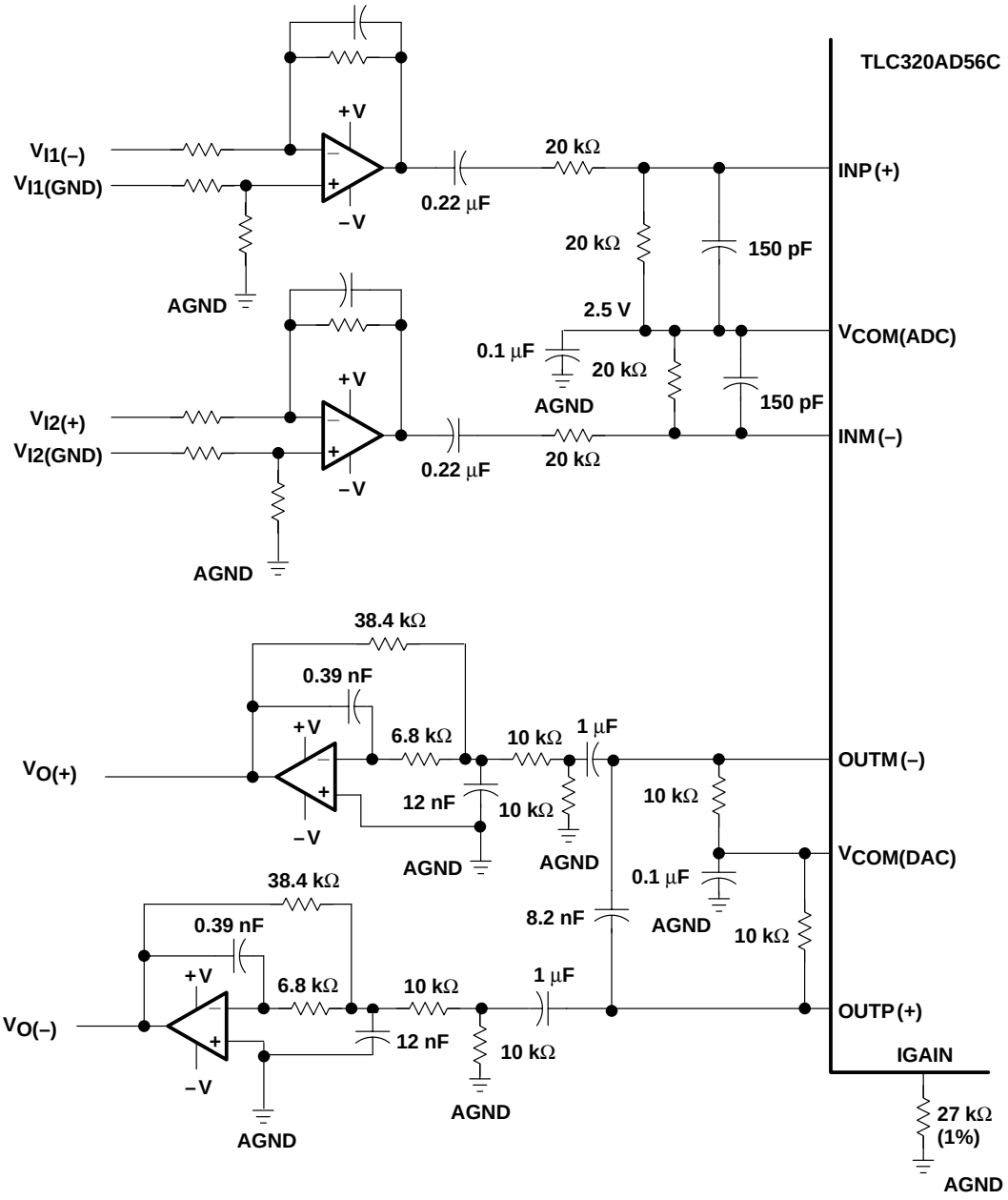


Figure 5–2. Application Schematic For Differential Input/Output

Appendix A
Register Set

Bits D12 through D8 in a secondary serial communication comprise the address of the register that is written with the data carried in D7 through D0. D13 determines a read or write cycle to the addressed register. When low, a write cycle is selected.

Table A–1 shows the register map.

Table A–1. Data and Control Registers

REGISTER NO.	BITS								REGISTER NAME
	D15	D14	D13	D12	D11	D10	D9	D8	
0	0	0	0	0	0	0	0	0	No operation
1	0	0	0	0	0	0	0	1	Control 1
2	0	0	0	0	0	0	1	0	Control 2

Table A–2. Control 1 Register

BITS								DESCRIPTION
D7	D6	D5	D4	D3	D2	D1	D0	
1	–	–	–	–	–	–	–	Software reset
0	–	–	–	–	–	–	–	Software reset not asserted
–	1	–	–	–	–	–	–	Software power down (analog and filters)
–	0	–	–	–	–	–	–	Software power down (not asserted)
–	–	1	–	–	–	–	–	Select AUXP and AUXM
–	–	0	–	–	–	–	–	Select INP and INM
–	–	–	0	–	–	–	–	Select INP and INM for monitor
–	–	–	1	–	–	–	–	Select AUXP and AUXM for monitor
–	–	–	–	1	1	–	–	Monitor amp gain = –18 dB (see Note B)
–	–	–	–	1	0	–	–	Monitor amp gain = –8 dB (see Note B)
–	–	–	–	0	1	–	–	Monitor amp gain = 0 dB (see Note B)
–	–	–	–	0	0	–	–	Monitor amp mute
–	–	–	–	–	–	1	–	Digital loopback asserted
–	–	–	–	–	–	0	–	Digital loopback not asserted
–	–	–	–	–	–	–	1	16-bit mode (hardware secondary requests)
–	–	–	–	–	–	–	0	Not 16-bit mode (software secondary requests)

NOTES: A. Default value: 00000000
B. These gains are for a single-ended input. The gain is 6 dB lower with a differential input.

The software reset is a one-shot operation and this bit is cleared to 0 after reset. It is not necessary to write a zero to end the master reset operation. Writing 0s to the reserved bits is suggested.

Table A–3. Control 2 Register

BITS								DESCRIPTION
D7	D6	D5	D4	D3	D2	D1	D0	
–	–	X	–	–	–	–	–	Decimator FIR overflow flag (valid only during read cycle)
–	–	–	X	–	–	–	–	FLAG 1 output value (valid only during read cycle)
–	–	–	–	X	–	–	–	FLAG 0 output value (valid only during read cycle)
–	–	–	–	–	1	–	–	Phone mode enabled
–	–	–	–	–	0	–	–	Phone mode disabled
X	X	–	–	–	–	X	X	Reserved

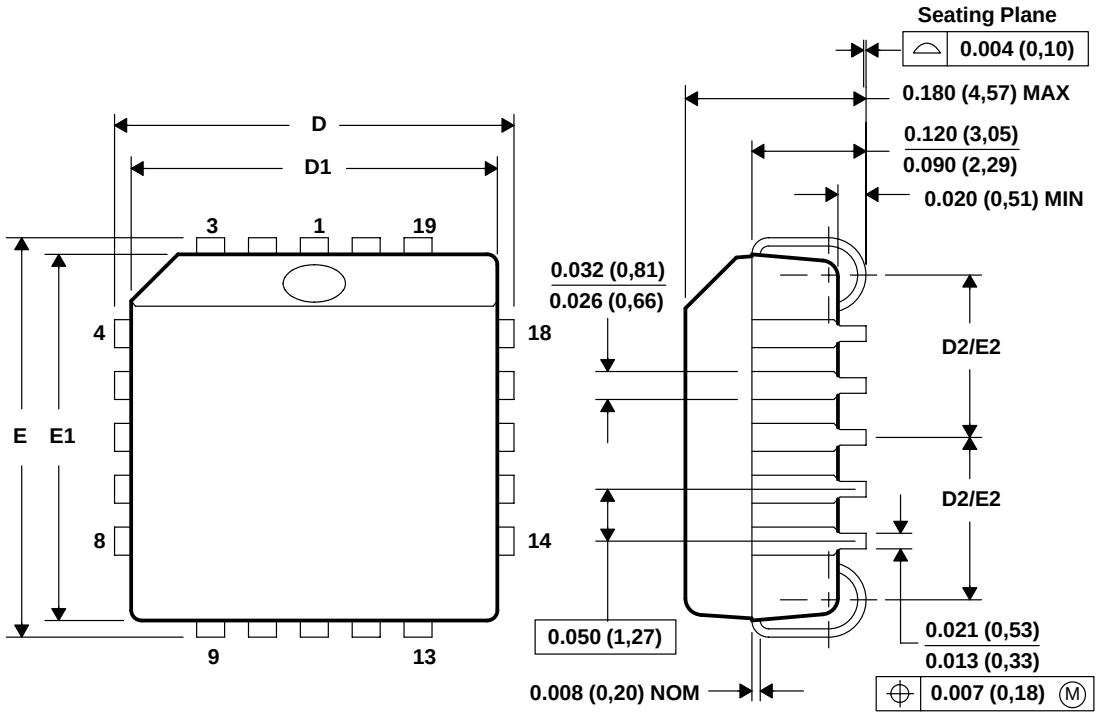
NOTES: A. Default value: 00000000
B. X = do not care

Writing 0s to the reserved bits is suggested.

Appendix B
Mechanical Data

FN (S-PQCC-J)** **PLASTIC J-LEADED CHIP CARRIER**

20 PIN SHOWN

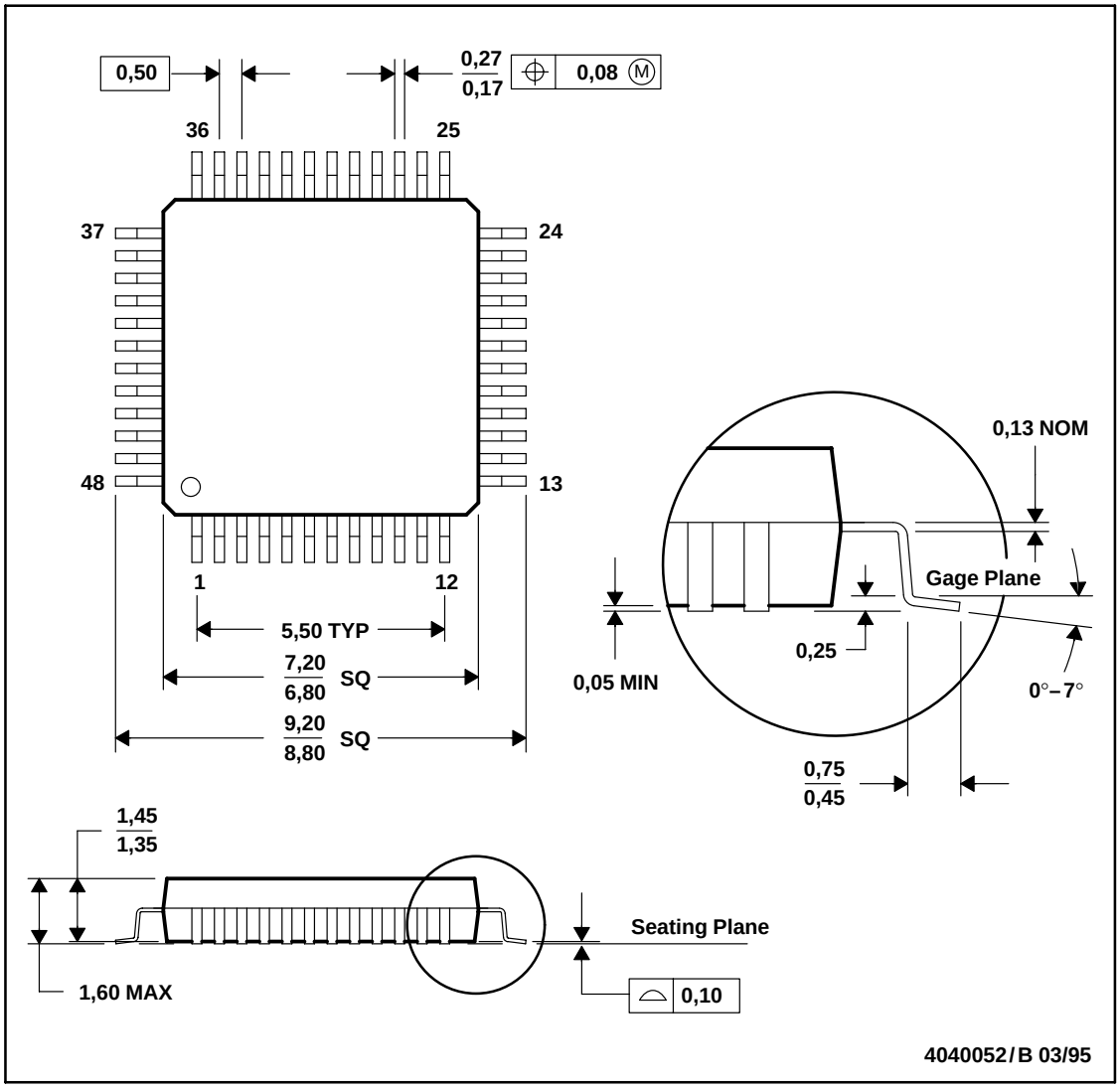


NO. OF PINS **	D / E		D1 / E1		D2 / E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

PT (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136
D. Also may be a thermally enhanced plastic package with leads conected to the die pads