TLC320AD75C
Data Manual

20-Bit Sigma-Delta Stereo ADA Circuit

SLAS144
February 1997

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Contents

Contents (Continued)

List of Illustrations

List of Tables

1 Introduction

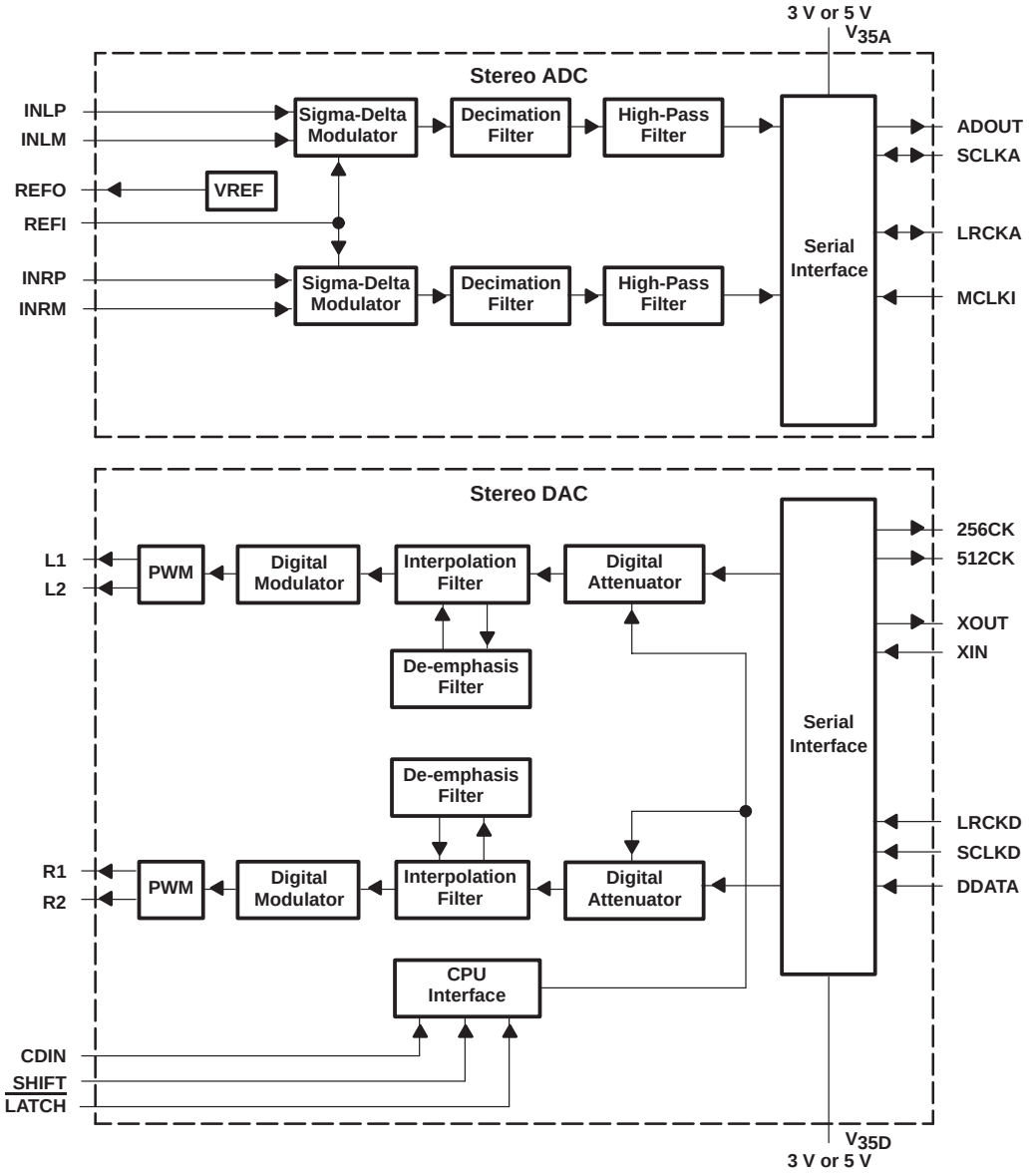
The TLC320AD75C is a high-performance stereo 20-bit analog-to-digital and digital-to-analog converter (ADA) using sigma-delta technology to provide four concurrent 20-bit resolution conversions from both analog-to-digital (A/D) and digital-to-analog (D/A) signal paths. Additional functions provided are digital attenuation, digital de-emphasis filtering, soft mute, and on-chip timing and control. Control words from a host controller or processor are used to implement these functions.

The TLC320AD75C is characterized for operation from 0°C to 70°C.

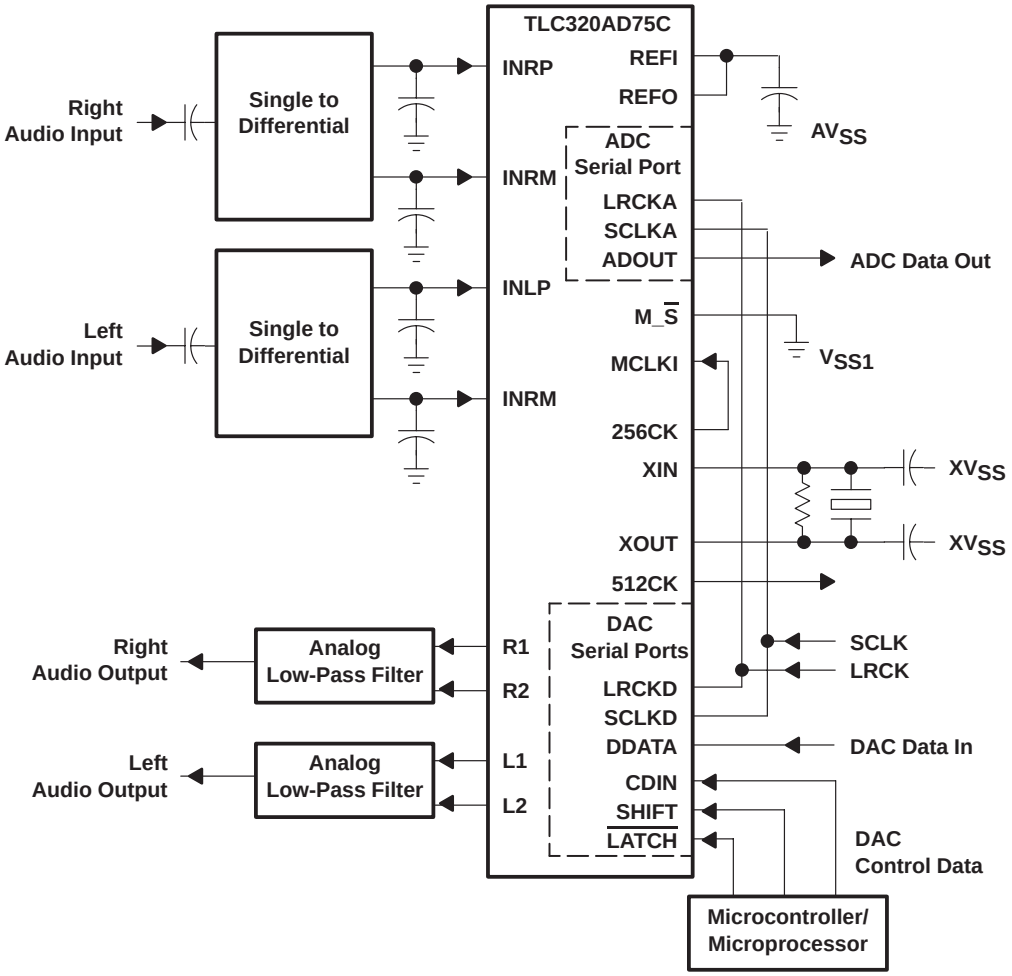
1.1 Features

- Single 5-V (Analog/Digital) Power Level and 3.3-V to 5-V Digital Interface Level
- Sample Rates up to 48 kHz
- 20-Bit Resolution Conversions
- Signal-to-Noise Ratio (EIAJ) of 100 dB for the ADC
- Total Harmonic Distortion + Noise of 0.0017% for the ADC
- Signal-to-Noise Ratio (EIAJ) of 104 dB for the DAC
- Total Harmonic Distortion + Noise of 0.0013% for the DAC
- Internal Voltage Reference (V_{ref})
- Serial Port Interface
- Differential Architecture
- DAC Provides PWM Output
- Digital De-emphasis Filtering for 32-, 44.1-, and 48-kHz Sample Rates for the DAC
- Digital Attenuation/Soft Mute Function for the DAC
- Small 56-Pin DL Plastic Small-Outline Package

1.2 Functional Block Diagram

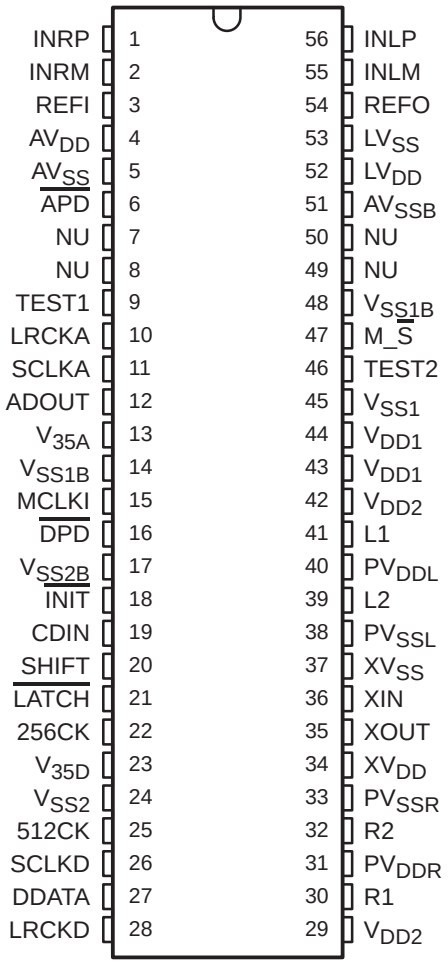


1.3 System Block Diagram



1.4 Terminal Assignments

DL PACKAGE
(TOP VIEW)



1.5 Ordering Information

T_A	PACKAGE
	SMALL OUTLINE (DL)
0°C to 70°C	TLC320AD75CDL

1.6 Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ADOUT	12	O	20-bit ADC data output. ADOUT provides the MSB first in 2's-complement data format and is left justified within the 32-bit packet for each channel. The output level is 3.3 V for V_{35A} = 3.3 V (see Figure 2–6).
$\overline{\text{APD}}$	6	I	Analog power-down mode. $\overline{\text{APD}}$ disables the ADC analog modulators. The ADC single-bit modulator outputs become invalid, rendering the outputs of the digital filters invalid. When $\overline{\text{APD}}$ is pulled high, normal operation of the device is resumed.
AV_{DD}	4		Analog power supply voltage for ADC modulators
AV_{SS}	5		Analog ground for ADC modulators
AV_{SSB}	51		Analog substrate ground for ADC modulators
CDIN	19	I	Attenuation mode and system control mode input for DAC. CDIN is a 24-bit stream with a 16-bit data word followed by an 8-bit device address. This stream is configured with the MSB first (see Section 2.15, *Sigma-Delta DAC Modulator*).
DDATA	27	I	DAC input data in 2's-complement data format. MSB/LSB first and 20-bit/16-bit input formats are selectable by using the DAC control registers (see Section 2.15, *Sigma-Delta DAC Modulator*).
$\overline{\text{DPD}}$	16	I	Digital power-down mode. The $\overline{\text{DPD}}$ shuts down the ADC digital decimation filters and clock generators, and provides a digital reset. All digital outputs of the ADC function, are brought to unasserted states. When $\overline{\text{DPD}}$ is pulled high, normal operation of the device is resumed. When in slave mode operation, after the rising edge of $\overline{\text{DPD}}$, the ADC system is synchronized.
$\overline{\text{INIT}}$	18	I	Initial DAC reset signal. The DAC device is activated on the rising edge of $\overline{\text{INIT}}$. When $\overline{\text{INIT}}$ is brought low, the DAC is reset when LRCKD is present.
INLM	55	I	Inverting input for the left channel analog modulator
INLP	56	I	Noninverting input for the left channel analog modulator
INRM	2	I	Inverting input for the right channel analog modulator
INRP	1	I	Noninverting input for the right channel analog modulator
$\overline{\text{LATCH}}$	21	I	Latch signal for the DAC control serial data. Attenuation/system-control data loads into the internal registers when $\overline{\text{LATCH}}$ is brought low.
LRCKA	10	I/O	Left/right clock for ADC. LRCKA signifies whether the serial data is associated with the left channel ADC (when LRCKA is high) or the right channel ADC (when LRCKA is low). LRCKA is normally connected to LRCKD. LRCKA is output when configured in master mode.
LRCKD	28	I	Left/right clock for DAC. LRCKD signifies whether the serial data is associated with the left channel DAC (when LRCKD is high) or the right channel DAC (when LRCKD is low). LRCKD is normally connected to LRCKA.
LV_{DD}	52		Digital power supply for analog modulators. LV_{DD} is normally connected to AV_{DD} through a 50-Ω resistor.
LV_{SS}	53		Digital ground for analog modulators. LV_{SS} is normally connected to AV_{SS} through a 50-Ω resistor.
L1	41	O	Left channel DAC PWM output 1
L2	39	O	Left channel DAC PWM output 2
MCLKI	15	I	Master clock input for ADC. MCLKI operates at 256 times the sample rate (i.e. 256 times LRCKA). MCLKI is normally connected to 256CK through a 50-Ω resistor.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
M_$\overline{S}$	47	I	Master/slave selection. The ADC serial port is configured as master mode when M_$\overline{S}$ is pulled high. M_$\overline{S}$ is connected to V_{SS1} for slave mode.
NU	7, 8, 49, 50	–	Not used
PV_{DDL}	40		PWM power supply for left channel DAC
PV_{DDR}	31		PWM power supply for right channel DAC
PV_{SSL}	38		PWM ground for left channel DAC
PV_{SSR}	33		PWM ground for right channel DAC
REFI	3	I	Input reference voltage. REFI provides reference voltage for the ADC modulator (normally connected to REFO).
REFO	54	O	Internal ADC reference voltage (normally connected to REFI).
R1	30	O	Right channel DAC PWM output 1
R2	32	O	Right channel DAC PWM output 2
SCLKA	11	I/O	Shift clock for the ADC. The shift clock clocks serial data out of the ADC, and operates at 64 times the sample rate (i.e. 64 times LRCKA). SCLKA is normally connected to SCLKD. SCLKA is output when configured in master mode.
SCLKD	26	I	Shift clock for the DAC. The shift clock clocks serial audio data into the DAC, and operates at 64 times the sample rate (i.e. 64 times LRCKD). SCLKD is normally connected to SCLKA.
SHIFT	20	I	Shift data. SHIFT clocks the control data (CDIN) into the internal control registers for the DAC.
TEST1	9	I	Factory test terminal1. TEST1 should be connected to V_{SS1} for normal operation.
TEST2	46	I	Factory test terminal2. TEST2 should be connected to V_{SS1} for normal operation.
XIN	36	I	Oscillator input terminal for 512 times the DAC sample rate. XIN derives all of the key logic signals of the DAC device. (XIN can also be driven by an external oscillator.)
XOUT	35	O	Oscillator output terminal for 512 times the DAC sample rate
V_{DD1}	43, 44		Digital power supply for ADC
V_{DD2}	29, 42		Digital power supply voltage for DAC
V_{SS1}	45		Digital ground for ADC digital flters
V_{SS1B}	14, 48		Digital substrate ground for ADC
V_{SS2}	24		Digital ground for the DAC
V_{SS2B}	17		Digital sustrate ground for DAC
V_{35A}	13		Digital power supply for ADC interface logic. V_{35A} is connected to 3 V or 5 V.
V_{35D}	23		Digital power supply for DAC interface logic. V_{35D} is connected to 3 V or 5 V.
XV_{DD}	34		Oscillator power-supply voltage for DAC
XV_{SS}	37		Oscillator circuit ground for DAC
256CK	22	O	256 times sample rate clock output. 256CK is normally connected to MCLKI through a 50-Ω resistor. 256CK is the XIN frequency divided by two.
512CK	25	O	512 times sample rate clock output (output level is 3.3 V for V_{35D} = 3.3 V). 512CK is a buffered version of XIN (master clock input).

2 Detailed Description

The sigma-delta ADC converter consists of an oversampling analog modulator and digital decimation filter.

The sigma-delta DAC incorporates an interpolation finite impulse-response (FIR) filter and oversampled modulator. The pulse-width-modulation (PWM) digital output feeds an external low-pass filter to recover the analog audio signal.

Two control registers configure the DAC. The attenuation register controls the attenuation range, de-emphasis enable, and mute selection. The system register controls the data format and de-emphasis filter-sample rate.

2.1 Power-Down and Reset Functions

2.1.1 ADC Power Down

The power-down state is comprised of a separate digital and analog power down for the ADC. The power consumption of each is detailed in the electrical characteristics section.

The digital power-down mode shuts down the digital filters and clock generators. When the digital power-down terminal is pulled high, normal operation of the device is initiated. In slave mode, the conversion process must synchronize to an input on LRCKA as well as SCLKA. Therefore, the conversion process is not initiated until the first rising edges of both SCLKA and LRCKA are detected after $\overline{\text{DPD}}$ is pulled high. This synchronizes the conversion cycle; all conversions are performed at a fixed LRCKA rate after the initial synchronization. After $\overline{\text{DPD}}$ is brought high, the output of the digital filters remains invalid for 26 LRCKA cycles which consists of group delays of the decimation and high-pass filter.

The analog power-down mode disables the analog modulators. The single-bit modulator outputs become invalid, which renders the outputs of the digital filters invalid. When the $\overline{\text{APD}}$ terminal is brought high, the modulators are brought back online; however, the settling time of the modulator stage is normally 100 ms.

2.1.2 Reset Function for ADC

The conversion process is not initiated until the first rising edges of both SCLKA and LRCKA are detected after $\overline{\text{DPD}}$ is pulled high. This synchronizes the conversion cycle; all conversions are performed at a fixed LRCKA rate after the initial synchronization.

During general operation of the ADC, $\overline{\text{APD}}$ is recommended to be pulled high ($\overline{\text{APD}}$ is not needed for a reset). When using the analog power-down mode ($\overline{\text{APD}}$ low), the following timing procedure is required to start all of the ADC since the analog modulator portion which includes the external portion needs to be settled after $\overline{\text{APD}}$ is high.

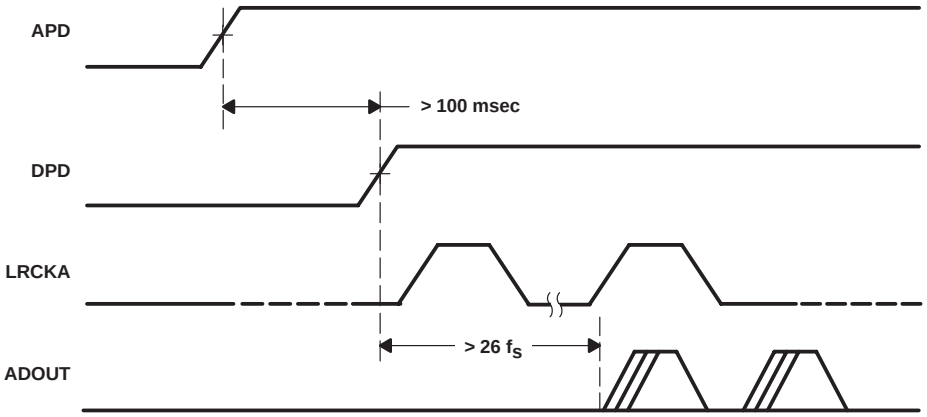


Figure 2–1. ADC Start-Up Timing

2.1.3 Reset/Initialization for DAC

When $\overline{\text{INIT}}$ is brought low, an internal reset signal becomes active approximately 120 cycles of the sampling frequency (f_S) after the falling edge of $\overline{\text{INIT}}$. Under this condition, all internal circuits are initialized and the PWM output is held at zero data (50% duty cycle). When $\overline{\text{INIT}}$ is brought high, the internal reset signal goes inactive for a maximum of five LRCKD periods after the rising edge of $\overline{\text{INIT}}$. At this point, internal clocks are synchronous with LRCKD and the PWM output is valid (see Figure 2–2). LRCKD must be applied for proper initialization.

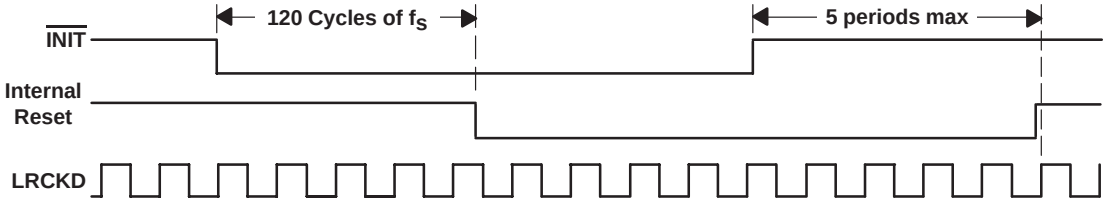


Figure 2–2. DAC-Reset Timing Relationships

2.2 Differential Input to the ADC

The input to the ADC is differential in order to provide common-mode noise rejection and increase the input dynamic range. Figure 2–3 shows the analog input signals used in a differential configuration to achieve a 6.4 $V_{I(PP)}$ differential swing with a 3.2 $V_{I(PP)}$ swing per input line.

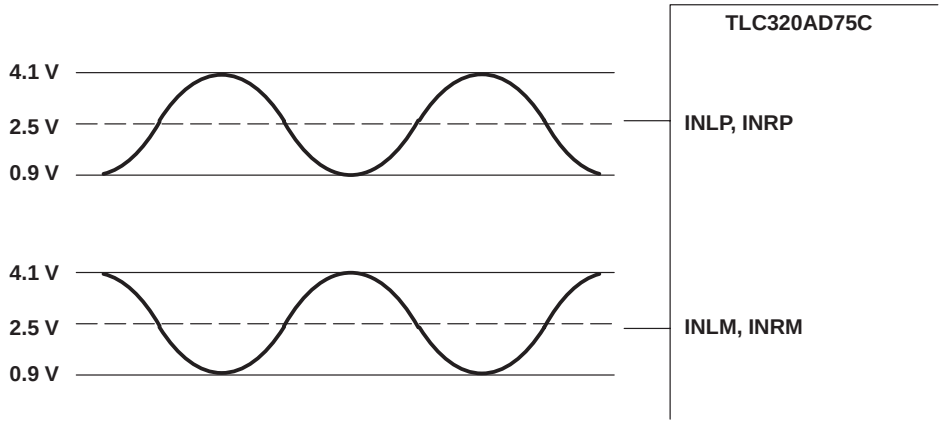


Figure 2–3. Differential Analog-Input Configuration

2.3 Sigma-Delta Modulator for the ADC

The modulator is a fourth-order sigma-delta modulator with 64 times oversampling. The ADC provides high-resolution, low-noise performance from a 1-bit converter using oversampling techniques.

2.4 Decimation Filter

The decimation filter after the sigma-delta ADC modulator reduces the digital data rate to the sampling rate of LRCKA. This is accomplished by decimating with a ratio of 1:64.

2.5 High-Pass Filter

The high-pass filter removes dc from the input of the ADC. The output of this filter is a 2's-complement data word of 20 bits serially clocked out. If the input value exceeds the full range of the converter, the output of the high-pass filter is held at the appropriate extreme until the input returns to the analog input range of the TLC320AD75C.

2.6 Master Clock

2.6.1 Master-Clock Circuit for ADC

The master-clock circuit generates and distributes necessary clocks throughout the device. MCLKI is the external master-clock input. The sample rate of the data paths is set as LRCKA = MCLKI/256. With a fixed oversampling ratio of 64 $\times$ f_S, the effect of changing MCLKI is shown in Table 2–1.

Table 2–1. ADC Master Clock to Sample-Rate Comparison

MCLKI (MHz)	SCLKA (MHz)	LRCKA (kHz)
12.2880	3.0720	48
11.2896	2.8224	44.1
8.1920	2.0480	32

When the TLC320AD75C is in master mode (M_$\overline{S}$ is pulled high) SCLKA is derived from MCLKI in order to provide clocking of the serial communications between the sigma-delta audio ADC and a digital signal processor (DSP) or control logic. This is equivalent to a clock running at 64 $\times$ LRCKA.

When the TLC320AD75C is in slave mode (M_$\overline{S}$ is connected to V_{SS1}), SCLKA is externally derived. For SCLKA use of a clock running at 64 times LRCKA is recommended.

2.6.2 Master-Clock Circuit for DAC

The timing and control circuit generates and distributes necessary clocks throughout the TLC320AD75C. XIN is the oscillator input terminal or can receive an external master-clock input. The sample rate of the data paths is set as LRCKD = XIN/512. With a fixed oversampling ratio of 32$\times$ and each PWM output value requiring 16 XIN cycles, the effect of changing XIN is shown in Table 2–2.

Table 2–2. DAC Master Clock to Sample-Rate Comparison

XIN (MHz)	256CK (MHz)	LRCKD (kHz)
24.5760	12.2880	48.0
22.5792	11.2896	44.1
16.3840	8.1920	32.0

The DAC can be operated at any conversion rate between 48 kHz and 32 kHz by choosing the appropriate master-clock frequency. Some of the functions of the converter, such as the deemphasis filter, operate only at the frequencies shown in Table 2–2.

2.7 Test

TEST1 and TEST2 are reserved for factory test and are tied to digital ground (V_{SS1}).

2.8 Master Mode for ADC

Configured as the master device (M_$\overline{S}$ is connected to V_{DD1}), the TLC320AD75C generates LRCKA and SCLKA from MCLKI. These signals are provided for synchronizing the serial port of a digital signal processor (DSP) or other control devices.

LRCKA is generated internally from MCLKI. The frequency of LRCKA is fixed at the sampling frequency, f_S (MCLKI/256). During the high period of LRCKA, the left channel data is serially shifted to the output; during the low period, the right channel data is shifted to the output (ADOUT). The conversion cycle is synchronized with the rising edge of LRCKA.

Figure 2–4 (master mode) shows 20-bit data, MSB first, ADOUT data shifted out of the TLC320AD75 during the first 20 SCLKA periods of the 32 SCLKA periods for both left and right channel data.

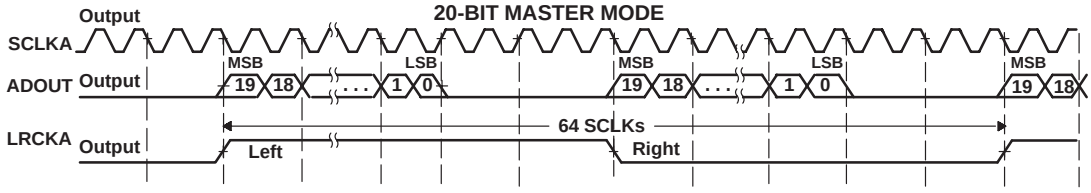


Figure 2–4. ADC Audio-Data Serial Timing – Master Mode

2.9 Slave Mode for ADC

Configured as a slave device (M_$\overline{S}$ is connected to V_{SS1}), the TLC320AD75C receives LRCKA and SCLKA as inputs. The conversion cycle is synchronized to the rising edge of LRCKA, and the data is synchronized to the falling edge of SCLKA. SCLKA must meet the setup requirements specified in the recommended operating conditions section. Synchronization of the slave mode is accomplished with the rising edge of $\overline{DPD}$.

The slave mode is shown in Figure 2–5. SCLKA and LRCKA are externally generated and sourced. The first rising edges of SCLKA and LRCKA after the rising edge of $\overline{DPD}$ initiate the conversion cycle (see Section 2.8, *Master Mode for ADC* for signal functions).

Figure 2–5 (slave mode) shows 20-bit data, MSB first, and ADOUT data shifted out of the TLC320AD75 during the first 20 SCLKA periods of the 32 SCLKA periods for both left and right channel data.

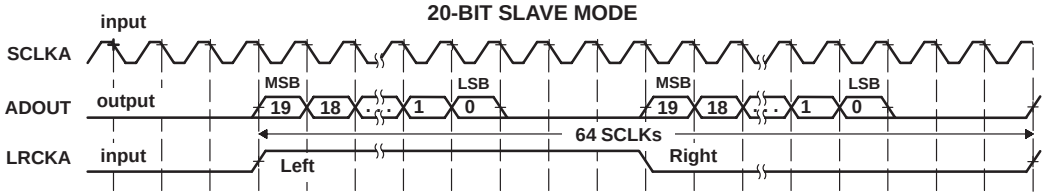


Figure 2–5. ADC Audio-Data Serial Timing – Slave Mode

2.10 Digital-Audio Data Interface for DAC

The conversion cycle is synchronized to the rising edge of LRCKD, and the data must meet the setup requirements specified in the timing requirements table. The input data is 16 or 20 bits with the MSB or LSB first as selected in the system register. The recommended SCLKD frequency is $64 \times f_S$. Figure 2–6 illustrates the input timing.

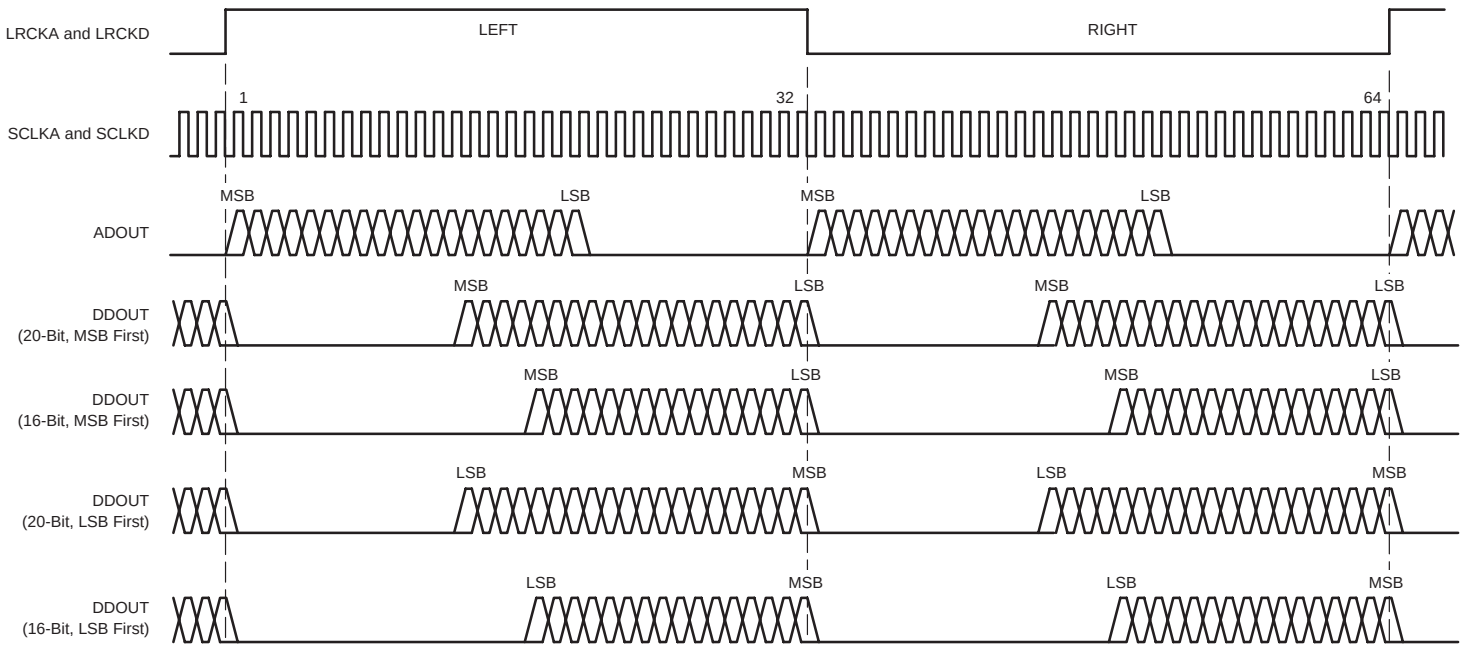


Figure 2–6. Audio-Data Serial Timing – ADC and All DAC Modes

2.11 Serial-Control Interface for DAC

The TLC320AD75C uses the most-significant-bit-first format. Therefore, for a 16-bit data word, D16 is the most significant bit (MSB) and D1 is the least significant bit (LSB).

2.11.1 Serial-Control-Data Input

The 16-bit control-data input implements the device-control functions. The TLC320AD75C has two registers for this data: the system register and the attenuation register. The system register contains most of the system configuration information, and the attenuation register controls the audio output level and deemphasis. Figure 2–7 illustrates the input timing for CDIN, SHIFT, and LATCH. The data loads internally during the low level of LATCH. The shift clock must be high or low for the LATCH setup time before LATCH goes low.

As shown in Figure 2–7, CDIN is a 24-bit data stream consisting of 16 bits of control data D16 through D1 followed by 8 bits of device, address A8 through A1. When the TLC320AD75C receives address >E7h, the control data is latched into the device by LATCH. For all other addresses, the data is ignored.

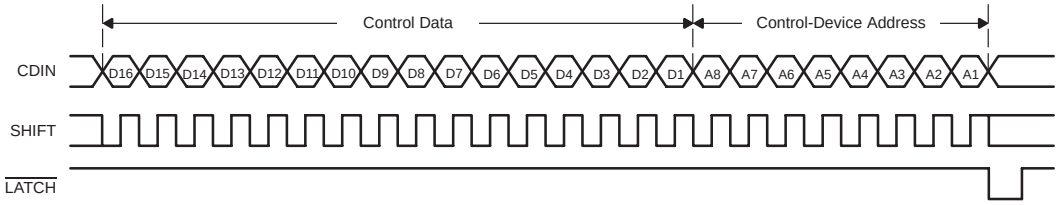


Figure 2–7. Control-Data Input Timing

2.12 DAC De-emphasis Filter

Three sets of de-emphasis-filter coefficients support the three sampling rates (f_S): 32 kHz, 44.1 kHz, and 48 kHz. Internal system-register values select the filter coefficients. The internal register values enable or disable the filter. Figure 2–8 illustrates the de-emphasis filtering characteristics.

Many audio sources have been recorded with pre-emphasis characteristics that are the inverse of the characteristics shown in Figure 2–8. This device provides reconstruction of the original frequency response.

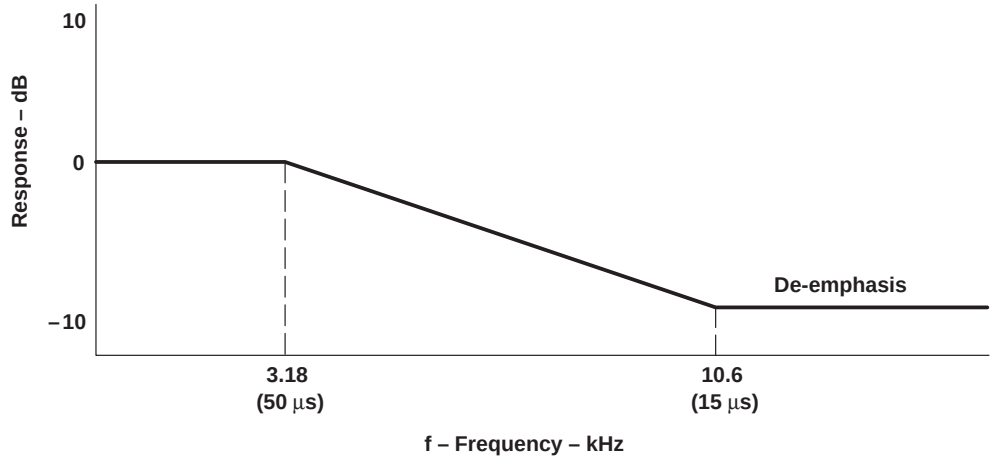


Figure 2–8. De-emphasis Filter Characteristics

2.13 Digital Filter Mute for DAC

When the mute bit in the attenuation register is set to 1, the DAC digital filter mute is active. The output of the digital filter is 0 + dc offset. Operation of the digital filter is normal during mute.

2.14 DAC Digital Attenuation/Soft Mute

A value selected in the internal attenuation register determines the attenuation of the digital-audio data input. The attenuation value is 12 bits long with a valid range of hex values from 400h to 000h. A data value of 001h corresponds to an attenuation value of –60 dB and a data value of 400h corresponds to 0 dB. The attenuation function is nonlinear. Figure 2–9 illustrates the attenuation function in dB. The default attenuation value is 400h (refer to the attenuator mode register for more detailed description).

$$\text{Attenuation} = 20 \log \left(\frac{\text{attenuation data}}{1024} \right)$$

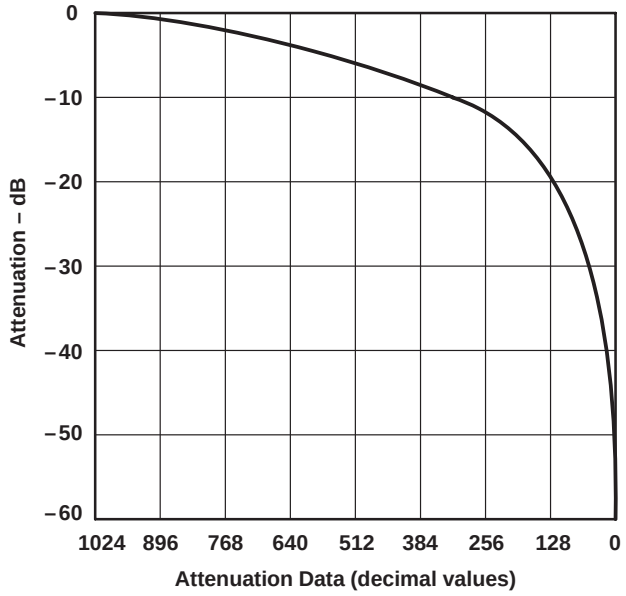


Figure 2–9. Digital Attenuation Characteristics

The attenuation operation of the DAC has a tapered gain response. It takes time T = 1024/f_S(sec) to reach the actual 000H data output after an ATT = 000H data transfer from 400H data as shown in Figure 2–10.

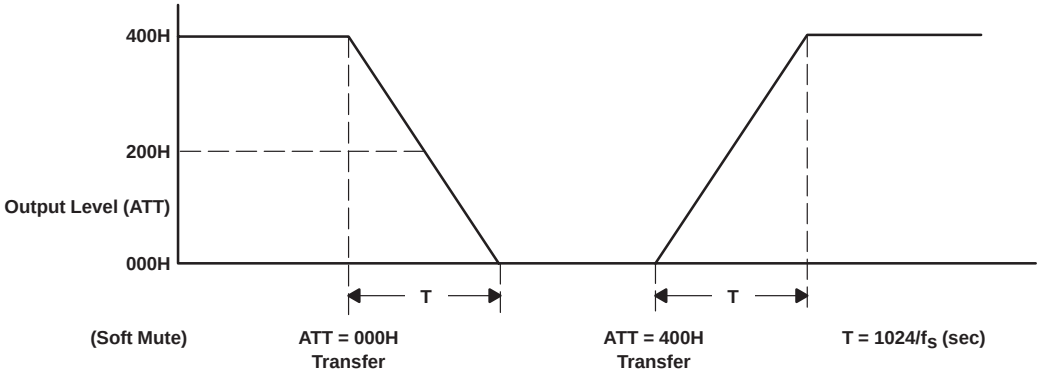
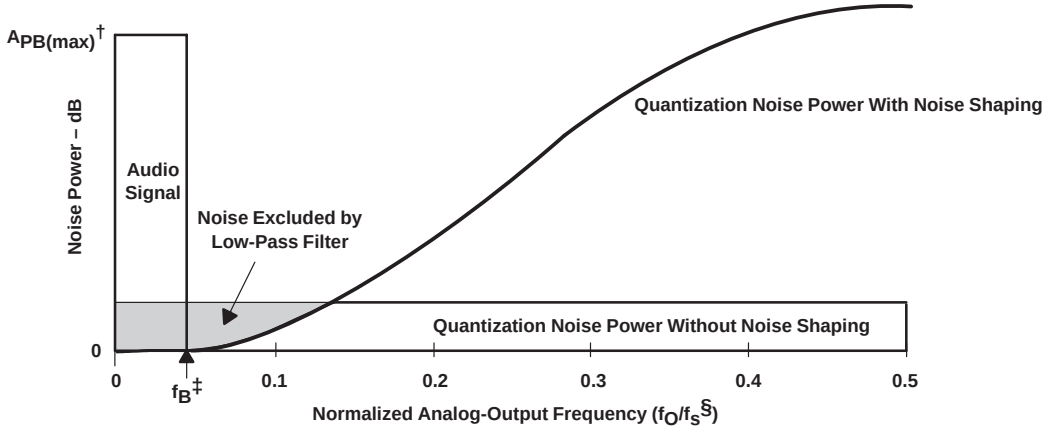


Figure 2–10. DAC Digital Attenuation Operation with Tapered Gain Response

2.15 Sigma-Delta DAC Modulator

The DAC uses a third-order modulator with 32 times oversampling. The DAC provides high-resolution, low-noise performance using a 15-value PWM output as shown in Figure 2–11.



† $A_{PB(max)}$ is the passband maximum amplitude.
‡ f_B is the highest frequency of interest within the baseband.
§ f_O is the output frequency at the external low-pass filter output.

Figure 2–11. Oversampling Noise Power With and Without Noise Shaping

2.16 DAC Interpolation Filter

The interpolation filter used prior to the DAC increases the digital-data rate from the LRCKD speed to the oversampled rate by interpolating with a ratio of 1:32. The oversampling modulator receives the output of this filter with de-emphasis as an option.

2.17 DAC PWM Output (L2 – L1 and R2 – R1)

The L2 – L1 and the R2 – R1 output pairs are PWM signals with the L2 – L1 differential pulse duration determining the left-channel analog voltage and the R2 – R1 differential pulse duration determining the right-channel analog voltage.

Each DAC left and right output consists of 15 levels of PWM and provides a differential signal as the input to two external differential amplifiers configured as a low-pass filter to produce the left and right audio outputs.

2.18 DAC Control Register Set

Tables 2–3 and 2–4 list the bit functions.

Table 2–3. Attenuation Mode Register†

D16–D5	D4	D3	D2	D1	DESCRIPTION	
0h	-	-	-	-	DAC attenuation (D5 = MSB, D16 = LSB)	Muted
1h	-	-	-	-		Digital attenuation, –60.2 dB
2h	-	-	-	-		Digital attenuation, –54.2 dB
3h	-	-	-	-		Digital attenuation, –50.7 dB
1FFh	-	-	-	-		Digital attenuation, –6.04 dB
200h	-	-	-	-		Digital attenuation, –6.02 dB
201h	-	-	-	-		Digital attenuation, –6.02 dB
3FFh	-	-	-	-		Digital attenuation, –0.01 dB
400h	-	-	-	-		Digital attenuation, 0 dB
-	0	-	-	-	D/F mute	Unmuted
-	1	-	-	-		Muted
-	-	0	-	-	De-emphasis enable	No de-emphasis
-	-	1	-	-		De-emphasis selected
-	-	-	0	-	DAC register select	Attenuator-mode register
-	-	-	1	-		System-mode register
-	-	-	-	0	DAC mode	Normal
-	-	-	-	1		Factory test only

† The initialization value is 0400h.

Table 2–4. System Mode Register†

D16	D15	D14	D13	D12–D5	D4	D3	D2	D1	DESCRIPTION	
0	-	-	-	-	-	-	-	-	Reserved	
-	0	-	-	-	-	-	-	-	Resynchronize	Off
-	1	-	-	-	-	-	-	-		On
-	-	0	0	-	-	-	-	-	Sample rate/ de-emphasis selection	44.1 kHz
-	-	0	1	-	-	-	-	-		Reserved
-	-	1	0	-	-	-	-	-		48 kHz
-	-	1	1	-	-	-	-	-		32 kHz
-	-	-	-	0	-	-	-	-	Reserved	
-	-	-	-	-	0	-	-	-	Input-data word width	20 bits audio data
-	-	-	-	-	1	-	-	-		16 bits audio data
-	-	-	-	-	-	0	-	-	Input D-data protocol	MSB first
-	-	-	-	-	-	1	-	-		LSB first
-	-	-	-	-	-	-	0	-	DAC register select	Attenuator-mode register
-	-	-	-	-	-		1	-		System-mode register
-	-	-	-	-	-	-	-	0	DAC mode	Normal
-	-	-	-	-	-	-	-	1		Factory test only

† The initialization value is 0000h.

2.19 Auto-Resynchronization Functionality

The TLC320AD75C has an auto-resynchronization function to keep the entire coversion cycle for the ADC portion and DAC portion respectively checking the LRCK cycle of the f_S rate. When the ADC is in slave mode, the ADC portion has a window of ± 4 clocks of the internal 64 f_S clock to check the LRCK cycle with the f_S rate detecting the rising edge of LRCK within this window. When an error is detected on the LRCK cycle, the ADC conversion cycle is resynchronized with an external LRCK cycle at the next rising edge of LRCK. This resynchronization occurrs automatically and the ADC portion continues processing based on the new conversion cycle timing.

The DAC portion has a window of ± 2 clocks of the internal 128 f_S clock to check the LRCK cycle detecting the rising edge of the LRCK clock. When an error is detected, the conversion cycle of the DAC is resynchronized with an external LRCK cycle automatically and the DAC portion continues processing based on the new conversion cycle timing. (The external LRCK rate should be the same as the fs rate. This functionality is to ensure the TLC320AD75C conversion operation even if LRCK has a timing problem due to noise injection for example.)

3 Specifications

3.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)†

Supply voltage range, AV_{DD}, LV_{DD} (see Note 1) . . . . . –0.3 V to 6.5 V
Supply voltage range, V_{DD1}, V_{35A} (see Note 2) . . . . . –0.3 V to 6.5 V
Supply voltage range, $PV_{DD(L/R)}$, V_{DD2}, V_{35D}, XV_{DD}(see Note 3) . . . . –0.3 V to 6.5 V
Analog input voltage range, INLP, INLM, INRP, INRM . . . . . –0.3 V to AV_{DD} + 0.3 V
Digital input voltage range . . . . . –0.3 V to $V_{DD1/2}$ + 0.3 V
Output voltage range, V_O: L1, L2, R1, R2 . . . . . –0.3 V to AV_{DD} + 0.3 V
Operating free-air temperature range, T_A . . . . . –0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Case temperature for 10 seconds . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values for maximum ratings are with respect to AV_{SS}.
2. Voltage values for maximum ratings are with respect to V_{SS1}.
3. Voltage values for maximum ratings are with respect to V_{SS2}.

3.2 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Analog supply voltage, AV_{DD} (see Note 4)	4.75	5	5.25	V
Digital supply voltage, V_{DD1}	4.75	5	5.25	V
Analog logic supply voltage, LV_{DD}	4.75	5	5.25	V
Reference voltage at REFI		3.2		V
Digital supply voltage, V_{35A}, V_{35D}	3	3.3	5.25	V
Digital supply voltage, V_{DD2}	4.75	5	5.25	V
Digital supply voltage, PV_{DDL}, PV_{DDR}	4.75	5	5.25	V
Clock supply voltage, XV_{DD}	4.75	5	5.25	V
Setup time, SCLKA/SCLKD↑ before LRCKA/LRCKD valid, t_{su1} (see Figure 4–2)	50			ns
Setup time, LRCKA/LRCKD valid before SCLKA/SCLKD↑, t_{su2} (see Figure 4–2)	50			ns
Load resistance at ADOUT, R_L	8			kΩ
Operating free-air temperature, T_A	0		70	°C

NOTE 4: Voltages at analog inputs and outputs and AV_{DD} are with respect to AV_{SS}.

3.3 Electrical Characteristics, $AV_{DD} = LV_{DD} = V_{DD1} = V_{DD2} = PV_{DDL} = PV_{DDR} = XV_{DD} = 5$ V, $V_{35A} = V_{35D} = 3.3$ V, $T_A = 25°C$

3.3.1 Digital Interface

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage			2	3.3		V
V_{IH}	High-level input voltage	XIN		4.5	5		V
V_{IL}	Low-level input voltage				0.2	0.8	V
V_{IL}	Low-level input voltage	XIN			0.2	0.8	V
V_{OH}	High-level output voltage	ADOUT	I_{OH} = 0.4 mA	2.6	3.2		V
		512CK	I_{OH} = 0.4 mA	2.6	3.2		
		256CK	I_{OH} = 0.4 mA	4.5	4.9		
		L1, L2, R1, R2	I_{OH} = 0.4 mA	4.5	4.9		
		XOUT	I_{OH} = 1.2 mA	4.5	4.9		
V_{OL}	Low-level output voltage	ADOUT	I_{OL} = 2 mA		0.2	0.4	V
		512CK	I_{OL} = 2 mA		0.2	0.4	
		256CK	I_{OL} = 2 mA		0.2	0.4	
		L1, L2, R1, R2	I_{OL} = 2 mA		0.2	0.5	
		XOUT	I_{OL} = 1.2 mA		0.2	0.5	
I_{IH}	High-level input current, any digital input				0.1		μA
I_{IL}	Low-level input current, any digital input				0.1		μA
C_i	Input capacitance				5		pF
C_o	Output capacitance				5		pF

3.3.2 Analog Interface

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{I(analog)}$	Analog input voltage, ADC	Differential		6.4		V
		0 to peak		3.2		V
Z_i	Input impedance, ADC			200		kΩ

3.3.3 ADC Performance, f_S = 44.1 kHz, Bandwidth = 22.05 kHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			20		Bits
DYNAMIC PERFORMANCE					
Signal to noise (EIAJ)	INLP = INRP = 2.5 V dc INLM = INRM = 2.5 V dc	96	100		dB
Dynamic range	– 60 dB input		100		dB
Signal to noise + distortion (THD + N)	– 0.5 dB input		0.0017%	0.003%	
Total harmonic distortion (THD)			0.001%		
Interchannel isolation			120		dB
DC ACCURACY					
Absolute gain error			±0.2		dB
	– 0.5 dB IN		±0.2	±0.5	dB
Interchannel gain mismatch			±0.2		dB
Offset drift			0		LSB/°C

3.3.4 DAC Performance, 20-Bit Mode, f_S = 44.1 kHz, Bandwidth = 22.05 kHz

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Resolution	See Note 5			20		bits
Signal-to-noise ratio	See Note 5	De-emphasis not selected	100	104		dB
Signal-to-noise + distortion (THD + N)	See Note 5			0.0013%	0.0025%	

NOTE 5: These specifications are measured at the output (V_O) of the external low-pass filter.

3.3.5 ADC Inputs

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT					
Input voltage range	Differential		6.4		V
	0 to peak		3.2		
Input impedance			200		kΩ

3.3.6 ADC High-Pass Filter, f_S = 44.1 kHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Passband (–3 dB)			0.86		Hz
Passband	5 Hz		–0.12		dB
Group delay			$1/f_S$		s

3.3.7 ADC Decimation Filter, f_S = 44.1 kHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Passband ripple	20.03 kHz		±0.01		dB
Stopband attenuation	24.07 kHz	80			dB
Group delay			$25/f_S$		s

3.3.8 DAC Filter Characteristics, f_S = 44.1 kHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	f_S = 20 kHz		±0.002		dB
Stop-band attenuation	f_S = 24.1 kHz	75			dB
Group delay			$29/f_S$		s

3.3.9 Power Supply Current, f_S = 44.1 kHz

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{DD(A)}$	Power-supply current, analog (ADC)	AV_{DD} and LV_{DD}			29	40	mA
$I_{DD(AD)}$	Power-supply current, digital (ADC)	VDD1 and V35A			22	30	mA
$I_{DD(DA1)}$	Power-supply current, digital (DAC)	VDD2 and V35D			20	25	mA
$I_{DD(DA2)}$	Power-supply current, PWM/OSC (DAC)	PVDDL, PVDDR, and XVDD			17	25	mA
$I_{DD(AST)}$	Power-down current, analog (ADC)	AVDD and LVDD			250		µA
$I_{DD(DST)}$	Power-down current, digital (ADC)	VDD1 and V35A			150		µA
P_D	Power dissipation				400		mW
PSRR	Power-supply rejection ratio		0 to 24 kHz		75		dB
			24 kHz to 2.798 MHz		85		dB

3.4 ADC Switching Characteristics (see Figures 2–1 and 4–1)

PARAMETER		MIN	TYP	MAX	UNIT
f_{MCKI}	Input clock frequency, MCKI		11.3	12.8	MHz
$t_{d(MDD)}$	Delay time, SCLKA↓ to ADOUT, master mode	0		50	ns
$t_{d(MIRD)}$	Delay time, SCLKA↓ to LRCKA, master mode	–20		20	ns
$t_{d(SDD1)}$	Delay time, LRCKA to ADOUT, slave mode			50	ns
$t_{d(SDD2)}$	Delay time, SCLKA↓ to ADOUT, slave mode			50	ns

3.5 DAC Timing Requirements (see Figures 4–1 and 4–2, and Note 6)

		MIN	TYP	MAX	UNIT
f_{XIN}	Input frequency, XIN clock		22.6	25.6	MHz
t_{w1}	Pulse duration, SCLKD	155	177		ns
t_{w2}	Pulse duration, SHIFT	100			ns
t_{w3}	Pulse duration, $\overline{\text{LATCH}}$	100			ns
t_{su3}	Setup time, DDATA valid before SCLKD↑	20			ns
t_{h1}	Hold time, DDATA valid after SCLKD↑	20			ns
t_{su4}	Setup time, CDIN valid before SHIFT↑	20			ns
t_{h2}	Hold time, CDIN valid after SHIFT↑	20			ns
t_{su5}	Setup time, $\overline{\text{LATCH}}$↑ before SHIFT↑	100			ns
t_{h3}	Hold time, $\overline{\text{LATCH}}$↓ after SHIFT↑	80			ns

NOTE 6: All timing measurements were taken at the $V_{DD}/2$ voltage level.

4 Parameter Measurement Information

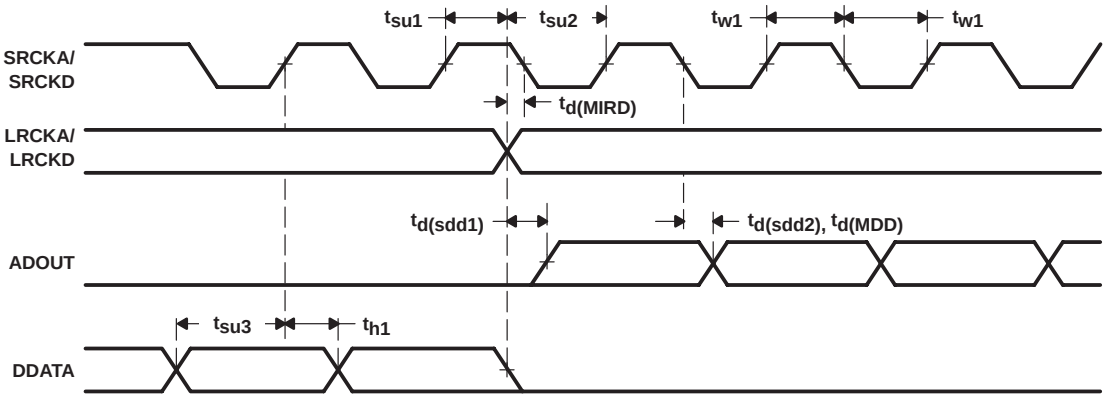


Figure 4–1. ADC Audio-Data Serial Timing

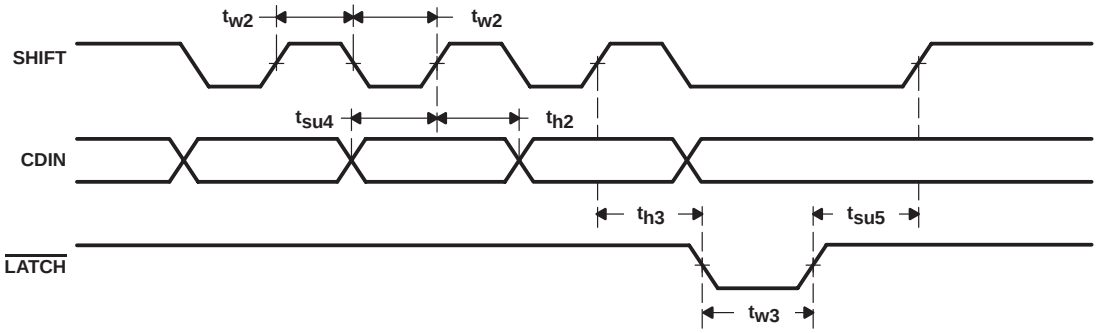


Figure 4–2. DAC Control-Data Serial Timing

5 Application Information

Table 5–1. TLC320AD75C Schematic Components

SYMBOL	DESCRIPTION
C1	220-μF capacitor
C2	4700-pF capacitor
C3	4700-pF capacitor
C4	220-μF capacitor
C5	47-μF capacitor
C6	22-μF capacitor
C7	0.1-μF capacitor
C8	100-μF capacitor
C9	0.1-μF capacitor
C10	220-μF capacitor
C12	220-μF capacitor
C13	18-pF capacitor
C14	12-pF capacitor
C15	220-μF capacitor
C16	47-μF capacitor
C17	0.1-μF capacitor
C18	4700-μF capacitor
C19	4700-μF capacitor
C20	200-pF capacitor
C21	100-μF capacitor
C22	0.1-μF capacitor
C23	200-pF capacitor
C24	100-pF capacitor
C25	47-μF capacitor
C26	22-μF capacitor
C27	220-μF capacitor
C28	220-μF capacitor
C29	47-μF capacitor
C30	100-pF capacitor
C31	47-μF capacitor
C32	30-pF capacitor
C33	120-pF capacitor
C34	30-pF capacitor
C35	30-pF capacitor
C36	120-pF capacitor

Table 5–1. TLC320AD75C Schematic Components (Continued)

SYMBOL	DESCRIPTION
C37	30-pF capacitor
C38	100-μF capacitor
C39	100-μF capacitor
C40	4700-pF capacitor
C41	1200-pF capacitor
C42	1200-pF capacitor
C43	4700-pF capacitor
C44	47-μF capacitor
C45	47-μF capacitor
C46	100-μF capacitor
C47	100-μF capacitor
C48	47-μF capacitor
C49	47-μF capacitor
C50	0.1-μF capacitor
C51	0.1-μF capacitor
C52	0.1-μF capacitor
C53	47-μF capacitor
C54	220-μF capacitor
C55	0.1-μF capacitor
R1	50-Ω resistor
R2	50-Ω resistor
R3	50-Ω resistor
R4	50-Ω resistor
R5	50-Ω resistor
R6	50-Ω resistor
R7	50-Ω resistor
R8	50-Ω resistor
R9	50-Ω resistor
R10	50-Ω resistor
R11	50-Ω resistor
R12	50-Ω resistor
R13	50-Ω resistor
R14	1-MΩ resistor
R15	50-Ω resistor
R16	50-Ω resistor
R17	50-Ω resistor
R18	5-kΩ resistor
R19	620-Ω resistor
R20	10-kΩ resistor
R21	5-kΩ resistor

Table 5–1. TLC320AD75C Schematic Components (Continued)

SYMBOL	DESCRIPTION
R22	4.7-kΩ resistor
R23	5-kΩ resistor
R24	620-Ω resistor
R25	68-kΩ resistor
R26	33-kΩ resistor
R27	18-kΩ resistor
R28	33-kΩ resistor
R29	18-kΩ resistor
R30	68-kΩ resistor
R31	68-kΩ resistor
R32	33-kΩ resistor
R33	18-kΩ resistor
R34	33-kΩ resistor
R35	18-kΩ resistor
R36	68-kΩ resistor
R37	1.5-kΩ resistor
R38	1.5-kΩ resistor
R39	1.5-kΩ resistor
R40	1.5-kΩ resistor
R41	100-Ω resistor
R42	100-Ω resistor
R43	100-Ω resistor
R44	100-Ω resistor
R45	330-kΩ resistor
R46	330-kΩ resistor
R47	10-kΩ resistor
R48	10-kΩ resistor
R49	10-kΩ resistor
R50	10-kΩ resistor

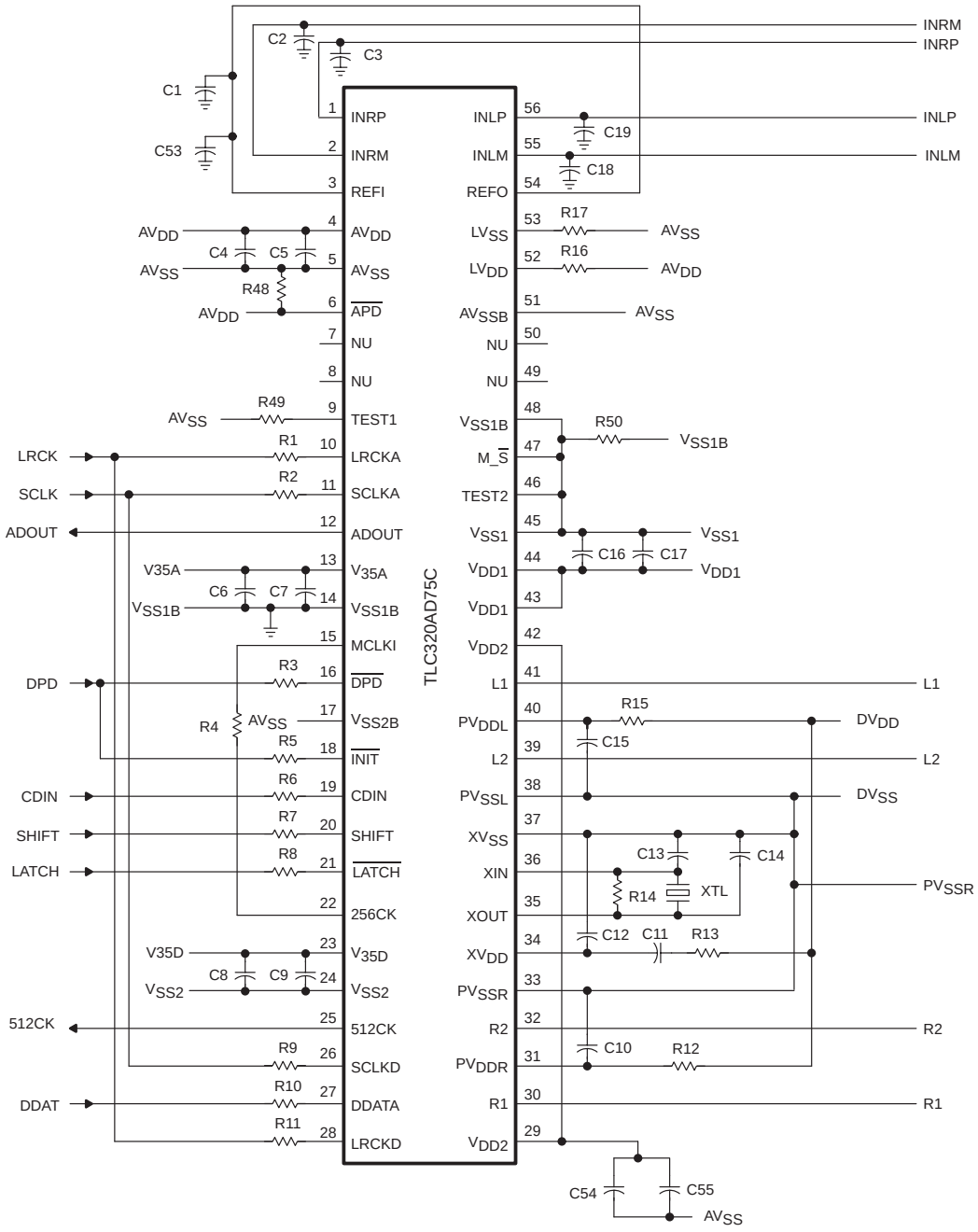


Figure 5–1. TLC320AD75C Application Schematic

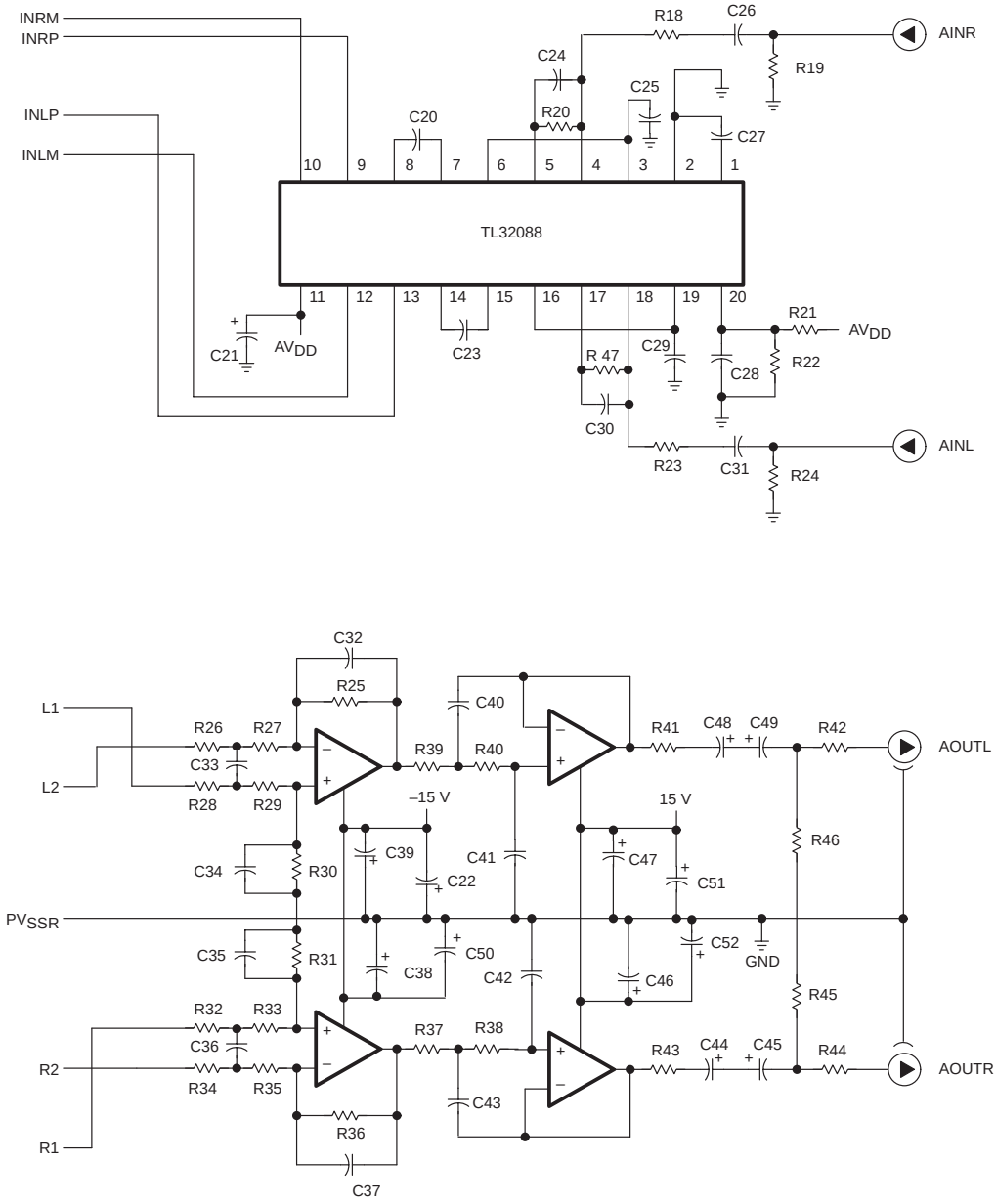


Figure 5–1. TLC320AD75C Application Schematic (Continued)

Table 5–2. A-Weighted Data

FREQUENCY	A WEIGHTING (dB)	FREQUENCY	A WEIGHTING (dB)
25	–44.6 ±2	800	–0.1 ±1
31.5	–39.2 ±2	1000	0 ±0
40	–34.5 ±2	1250	0.6 ±1
50	–30.2 ±2	1600	1.0 ±1
63	–26.1 ±2	2000	1.2 ±1
80	–22.3 ±2	2500	1.2 ±1
100	–19.1 ±1	3150	1.2 ±1
125	–16.1 ±1	4000	1.0 ±1
160	–13.2 ±1	5000	0.5 ±1
200	–10.8 ±1	6300	–0.1 ±1
250	–8.6 ±1	8000	–1.1 ±1
315	–6.5 ±1	10000	–2.4 ±1
400	–4.8 ±1	12500	–4.2 ±2
500	–3.2 ±1	16000	–6.5 ±2
630	–1.9 ±1		

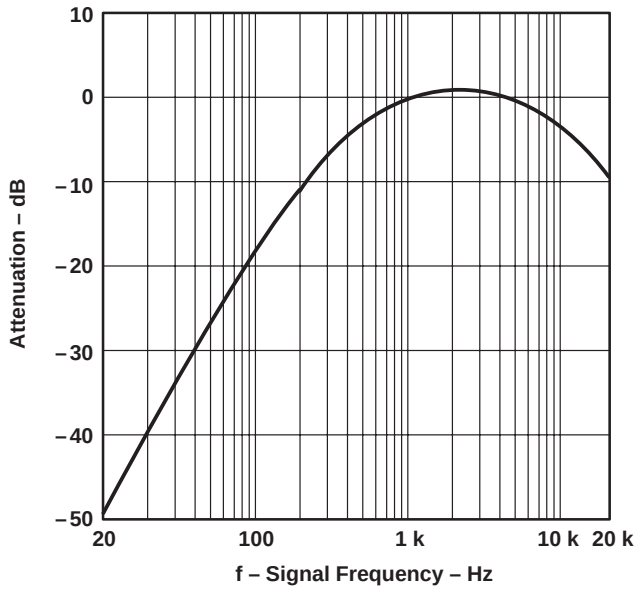


Figure 5–2. A-Weighted Function

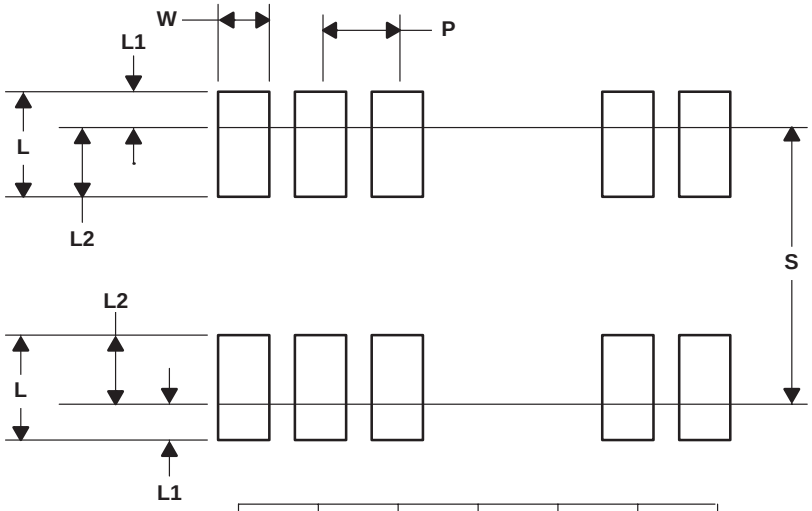
5.1 Circuit And Layout Considerations

The designer should follow these guidelines for the best device performance.

- Separate digital and analog ground planes should be used. All digital device functions should be over the digital ground plane, and all analog device functions should be over the analog ground plane. The ground planes should be connected at only one point to the direct power supply, and this is usually at the connector edge of the board.
- A single crystal-controlled clock should synchronously generate all digital signals.
- All power supply lines should include a 0.1-μF and a 1-μF capacitor. When clock noise is excessive, a toroidal inductance of 10 μH should be placed in series with XV_{DD} before connecting to DV_{DD}.
- The digital input control signals should be buffered when they are generated off of the card.
- Clock jitter should be minimized, and precautions taken to prevent clock overshoot. This minimizes any high-frequency coupling to the analog output.

5.2 PCB Footprint

Figure 5–3 shows the printed-circuit-board (PCB) land pattern for the TLC320AD75C small-outline package.



P	S	W	L	L1	L2
1.27	9.53	0.76	1.55	0.64	0.91

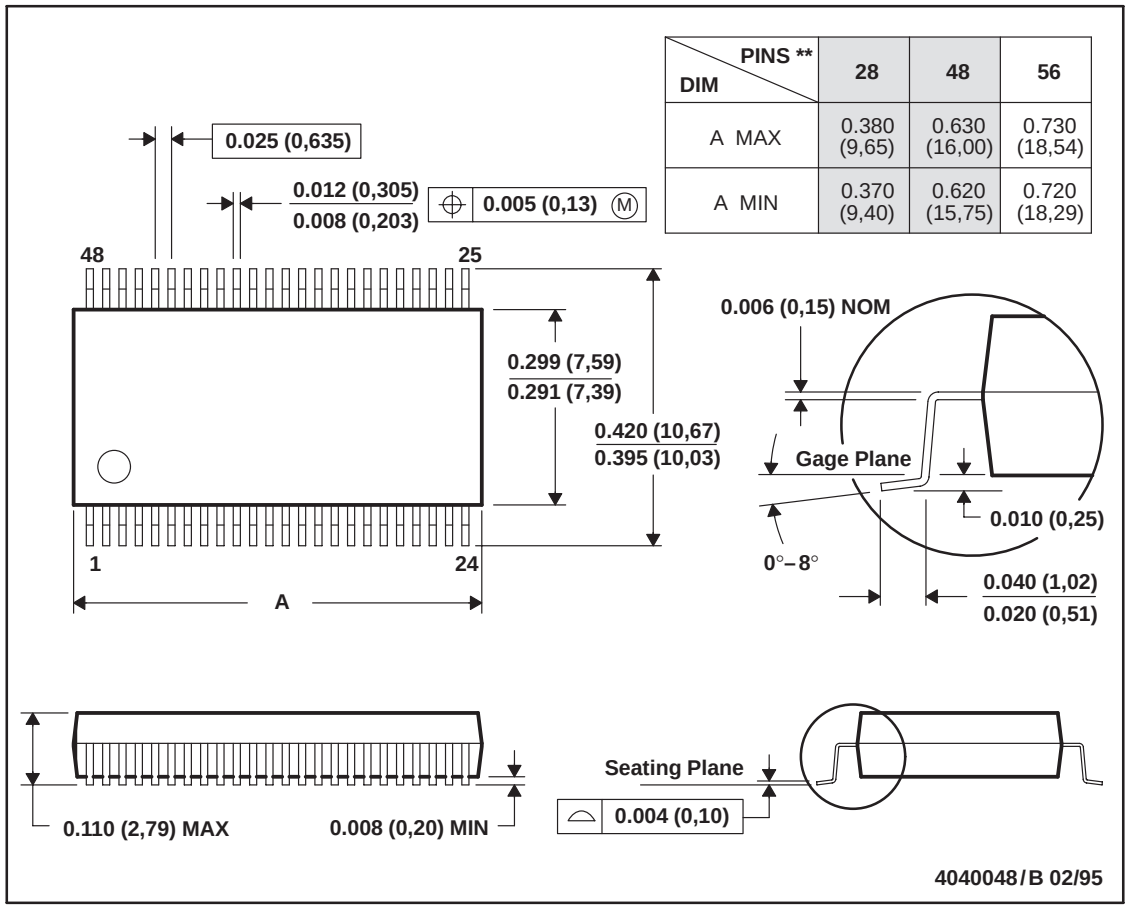
NOTE A: All linear dimensions are in millimeters.

Figure 5–3. Land Pattern for PCB Layout

Appendix A
Mechanical Data

DL (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PIN SHOWN



DIM \ PINS **	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TLC320AD75CDL	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.