# 16-CHANNEL CONSTANT-CURRENT LED SINK DRIVERS

## FEATURES

- **16 Constant-Current Output Channels**
- **Output Current Adjusted By External Resistor**
- **Constant Output Current Range: 5 mA to 120 mA**
- **Constant Output Current Invariant to Load Voltage Change**
- **Open-Load, Shorted-Load and Overtemperature Detection**
- **256-Step Programmable Global Current Gain**
- **Excellent Output-Current Accuracy:**
  - **Between Channels: < ±6% (Max), 10 mA to 50 mA**
  - **Between ICs: < ±6% (Max), 10 mA to 50 mA**

- **30-MHz Clock Frequency**
- **Schmitt-Trigger Input**
- **3.3-V or 5-V Supply Voltage**
- **Thermal Shutdown for Overtemperature Protection**
- **ESD Performance: 2-kV HBM**

## APPLICATIONS

- **General LED Lighting Applications**
- **LED Display Systems**
- **LED Signage**
- **Automotive LED Lighting**
- **White Goods**

## DESCRIPTION/ORDERING INFORMATION

The TLC5926/TLC5927 is designed for LED displays and LED lighting applications with open-load, shorted-load, and overtemperature detection, and constant-current control. The TLC5926/TLC5927 contains a 16-bit shift register and data latches, which convert serial input data into parallel output format. At the TLC5926/TLC5927 output stage, 16 regulated-current ports provide uniform and constant current for driving LEDs within a wide range of VF (Forward Voltage) variations. Used in systems designed for LED display applications (e.g., LED panels), TLC5926/TLC5927 provides great flexibility and device performance. Users can adjust the output current from 5 mA to 120 mA through an external resistor, $R_{ext}$, which gives flexibility in controlling the light intensity of LEDs. TLC5926/TLC5927 is designed for up to 17 V at the output port. The high clock frequency, 30 MHz, also satisfies the system requirements of high-volume data transmission.

The TLC5926/TLC5927 provides a Special Mode in which two functions are included, Error Detection and Current Gain Control. In the TLC5926/TLC5927 there are two operation modes and three phases: Normal Mode phase, Mode Switching transition phase, and Special mode phase. The signal on the multiple-function pin $\overline{OE}$(ED2) is monitored, and when an one-clock-wide short pulse appears on $\overline{OE}$(ED2), TLC5926/TLC5927 enters the Mode Switching phase. At this time, the voltage level on LE(ED1) determines the next mode into which the TLC5926/TLC5927 switches.

In the Normal Mode phase, the serial data is transferred into TLC5926/TLC5927 via SDI, shifted in the shift register, and transferred out via SDO. LE(ED1) can latch the serial data in the shift register to the output latch. $\overline{OE}$(ED2) enables the output drivers to sink current.

In the Special Mode phase, the low-voltage-level signal $\overline{OE}$(ED2) can enable output channels and detect the status of the output current, to tell if the driving current level is enough or not. The detected error status is loaded into the 16-bit shift register and shifted out via SDO, along with the CLK signal. The system controller can read the error status to determine whether or not the LEDs are properly lit. In the Special Mode phase, TLC5926/TLC5927 also allows users to adjust the output current level by setting a runtime-programmable Configuration Code. The code is sent into TLC5926/TLC5927 via SDI. The positive pulse of LE(ED1) latches the code in the shift register into a built-in 8-bit configuration latch, instead of the output latch. The code affects the voltage at R-EXT and controls the output-current regulator. The output current can be adjusted finely by a gain ranging from 1/12 to 127/128 in 256 steps. Therefore, the current skew between ICs can be compensated within less than 1%, and this feature is suitable for white balancing in LED color-display panels.

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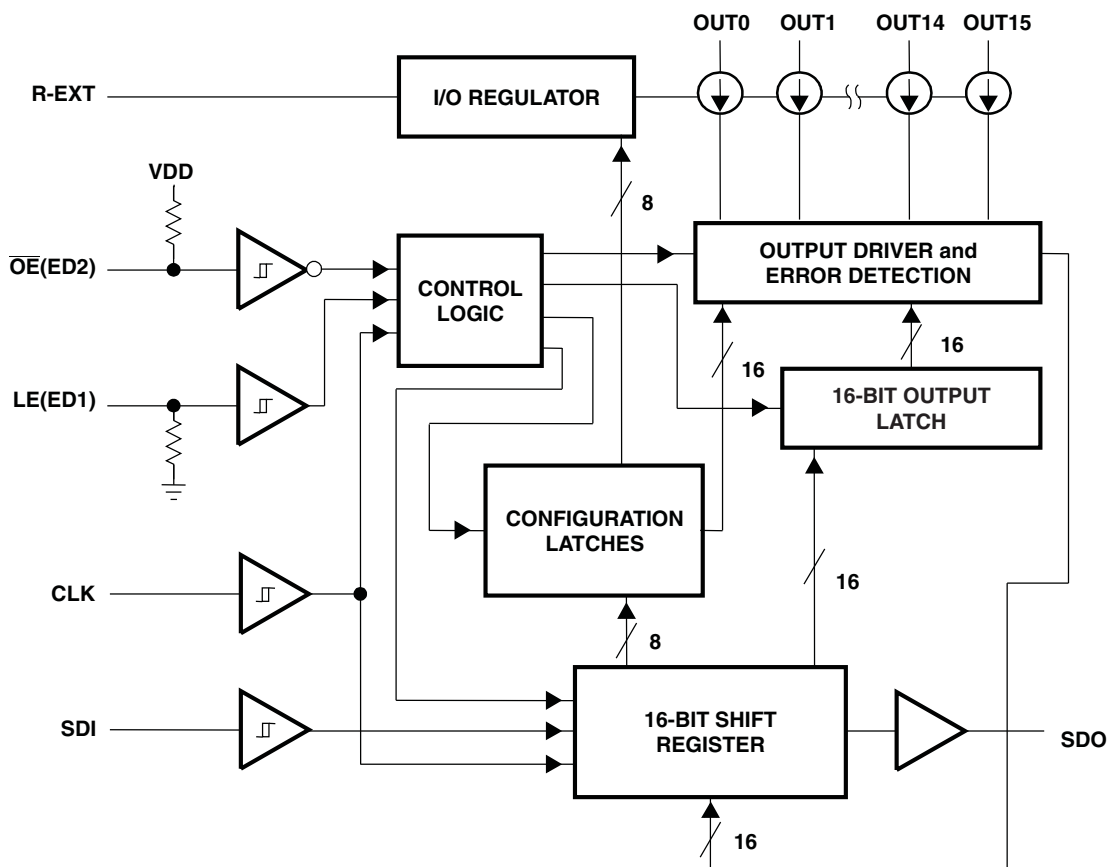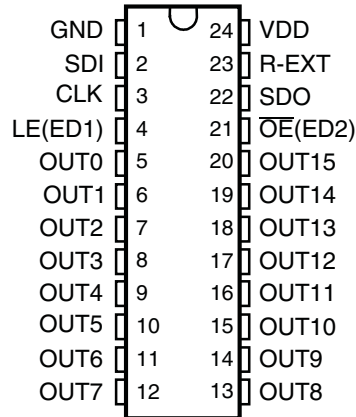
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## ORDERING INFORMATION[1]

| T$_A$ | PACKAGE[2] | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| −40°C to 85°C | PowerPAD™ – PWP | Reel of 2000 | TLC5926IPWPR | Y5926 |
| | | | TLC5927IPWPR | Y5927 |
| | W-SOIC – DW | Reel of 2000 | TLC5926IDWR | TLC5926I |
| | | | TLC5927IDWR | TLC5927I |
| | SSOP – DBQ | Reel of 2000 | TLC5926IDBQR | TLC5926I |
| | | | TLC5927IDBQR | TLC5927I |

(1)  For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2)  Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

## BLOCK DIAGRAM

Product Folder Link(s): *TLC5926  TLC5927*

**DBQ, DW, OR PWP PACKAGE**
**(TOP VIEW)**

| | | | |
|---|---|---|---|
| GND | 1 | 24 | VDD |
| SDI | 2 | 23 | R-EXT |
| CLK | 3 | 22 | SDO |
| LE(ED1) | 4 | 21 | $\overline{OE}$(ED2) |
| OUT0 | 5 | 20 | OUT15 |
| OUT1 | 6 | 19 | OUT14 |
| OUT2 | 7 | 18 | OUT13 |
| OUT3 | 8 | 17 | OUT12 |
| OUT4 | 9 | 16 | OUT11 |
| OUT5 | 10 | 15 | OUT10 |
| OUT6 | 11 | 14 | OUT9 |
| OUT7 | 12 | 13 | OUT8 |

## Pin Descriptions

| PIN NAME | DESCRIPTION |
|---|---|
| CLK | Clock input pin for data shift on rising edge |
| GND | Ground pin for control logic and current sink |
| LE(ED1) | Data strobe input pn<br>Serial data is transferred to the respective latch when LE(ED1) is high. The data is latched when LE(ED1) goes low. Also, a control signal input for an Error Detection mode and Current Adjust mode (See Timing Diagram). LE(ED1) has an internal pulldown. |
| $\overline{OE}$(ED2) | Output enable pin. When $\overline{OE}$ (ED2)(active) is low, the output drivers are enabled; when $\overline{OE}$(ED2) is high, all output drivers are turned OFF (blanked). Also, a control signal input for an Error Detection mode and Current Adjust mode (See Timing Diagram). $\overline{OE}$(ED2) has an internal pull-up. |
| OUT0–OUT15 | Constant-current output pins |
| R-EXT | Input pin used to connect an external resistor for setting up all output currents |
| SDI | Serial-data input to the Shift register |
| SDO | Serial-data output to the following SDI of next driver IC or to the microcontroller |
| VDD | Supply voltage pin |

## Diagnostic Features

| DEVICE[1] | OPEN-LOAD DETECTION | SHORT TO GND DETECTION | SHORT TO $V_{LED}$ DETECTION |
|---|---|---|---|
| TLC5926 | x | x | |
| TLC5927 | x | x | x |

(1)   The device has one single error register for all these conditions (one error bit per channel)
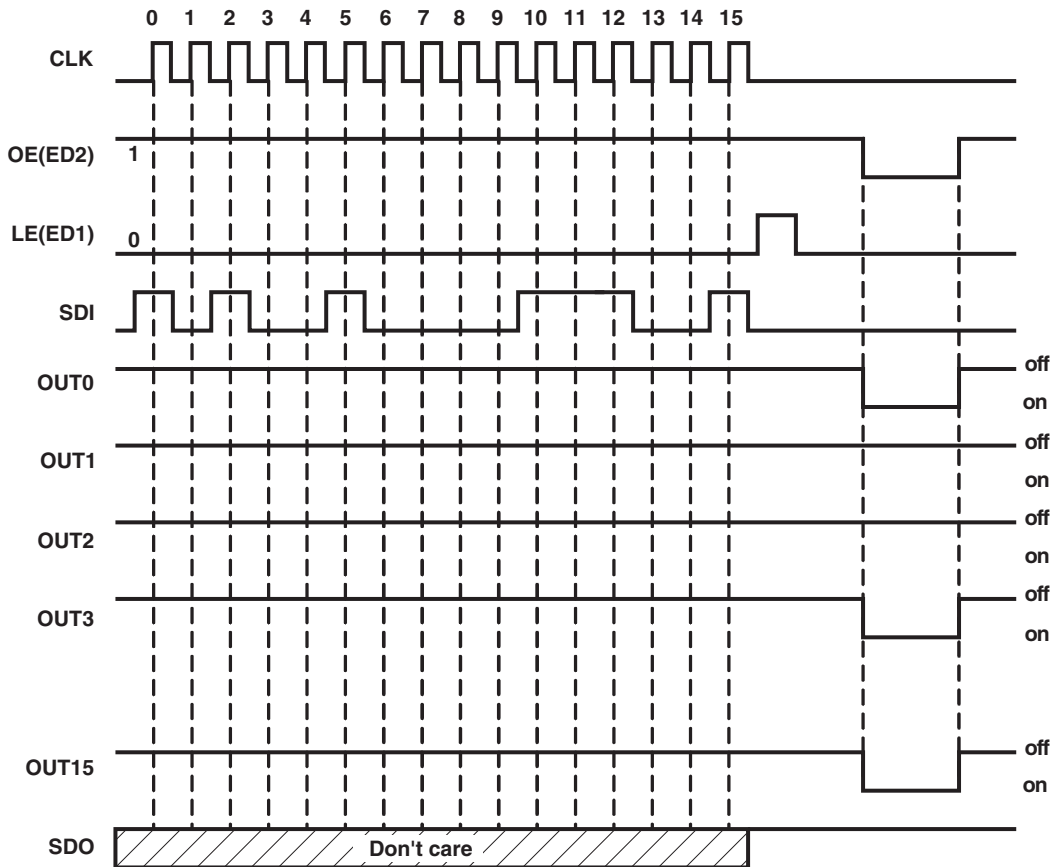
## Timing Diagrams



**Figure 1. Normal Mode**

**Truth Table in Normal Mode**

| CLK | LE(ED1) | $\overline{OE}$(ED2) | SDI | OUT0...OUT15 | SDO |
|-----|---------|---------|-----|--------------|-----|
| ↑ | H | L | Dn | Dn...Dn − 7...Dn − 15 | Dn − 15 |
| ↑ | L | L | Dn + 1 | No change | Dn − 14 |
| ↑ | H | L | Dn + 2 | Dn + 2...Dn − 5...Dn − 13 | Dn − 13 |
| ↓ | X | L | Dn + 3 | Dn + 2...Dn − 5...Dn − 13 | Dn − 13 |
| ↓ | X | H | Dn + 3 | off | Dn − 13 |

The signal sequence shown in Figure 2 makes the TLC5926/TLC5927 enter Current Adjust and Error Detection mode.
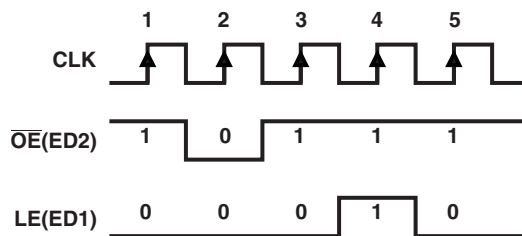


**Figure 2. Switching to Special Mode**

In the Current Adjust mode, sending the positive pulse of LE(ED1), the content of the shift register (a current adjust code) is written to the 16-bit configuration latch (see Figure 3).
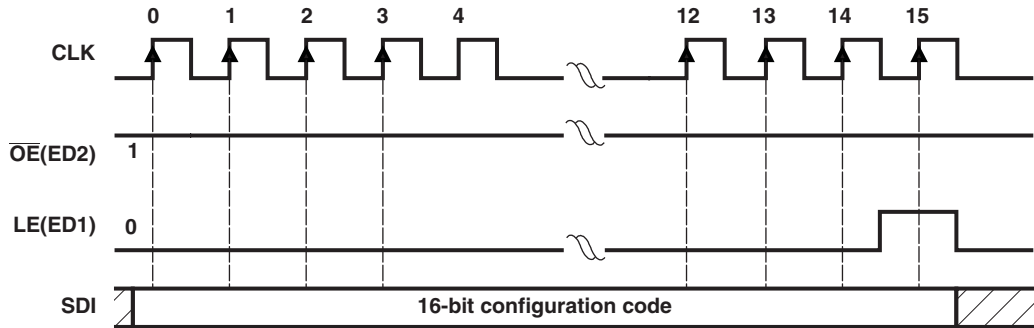


**Figure 3. Writing Configuration Code**

When the TLC5926/TLC5927 is in the error detection mode, the signal sequence shown in Figure 4 enables a system controller to read error status codes through SDO.
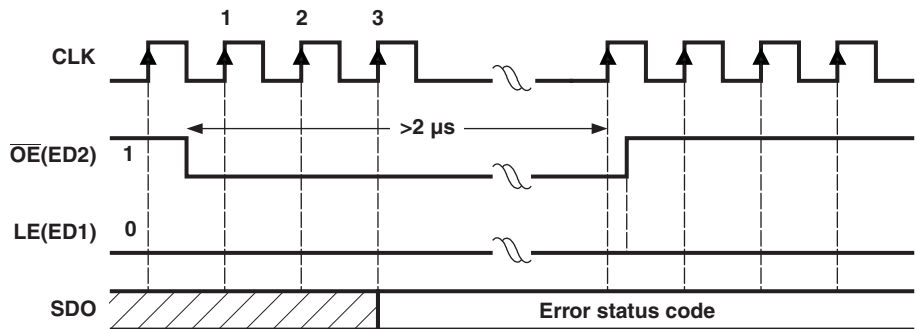


**Figure 4. Reading Error Status Code**

The signal sequence shown in Figure 5 makes TLC5926/TLC5927 resume the Normal mode. Switching to Normal mode resets all internal Error Status registers. OE (ED2) always enables the output port, whether the TLC5926/TLC5927 enters current adjust mode or not.
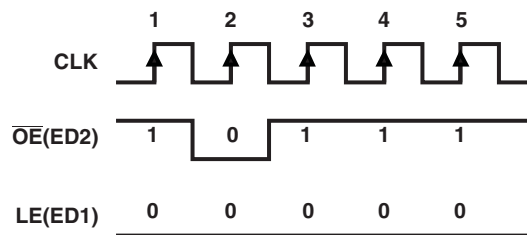


**Figure 5. Switching to Normal Mode**

## Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

|  |  | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 0 | 7 | V |
| $V_I$ | Input voltage | −0.4 | $V_{DD}$ + 0.4 | V |
| $V_O$ | Output voltage | −0.5 | 20 | V |
| $I_{OUT}$ | Output current |  | 120 | mA |
| $I_{GND}$ | GND terminal current |  | 1920 | mA |
| $T_A$ | Free-air operating temperature range | −40 | 85 | °C |
| $T_J$ | Operating junction temperature range | −40 | 150 | °C |
| $T_{stg}$ | Storage temperature range | −55 | 150 | °C |
| ESD | Electrostatic-Discharge Capability $V_{(HBMESD)}$ (100 pF, 1.5 kΩ) |  | 2 | kV |

## Power Dissipation and Thermal Impedance

|  |  |  |  | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $P_D$ | Power dissipation | Mounted on JEDEC 4-layer board (JESD 51-7), No airflow, $T_A$ = 25°C, $T_J$ = 125°C | DBQ package |  | 1.6 | W |
|  |  |  | DW package |  | 2.2 |  |
|  |  |  | PWP package |  | 2.3 |  |
|  |  | Mounted on JEDEC 4-layer board (JESD 51-5), No airflow, $T_A$ = 25°C, $T_J$ = 125°C | PWP package |  | 2.9 |  |
| $θ_{JA}$ | Thermal impedance, junction to free air | Mounted on JEDEC 1-layer board (JESD 51-3), No airflow | DBQ package |  | 99.8 | °C/W |
|  |  |  | DW package |  | 80.5 |  |
|  |  |  | PWP package |  | 63.9 |  |
|  |  | Mounted on JEDEC 4-layer board (JESD 51-7), No airflow | DBQ package |  | 61.0 |  |
|  |  |  | DW package |  | 45.5 |  |
|  |  |  | PWP package |  | 42.7 |  |
|  |  | Mounted on JEDEC 4-layer board (JESD 51-5), No airflow | PWP package |  | 34.5 |  |
| $θ_{JP}$ | Thermal impedance, junction to pad |  | PWP package |  | 2.0 | °C/W |

## Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|  |  | TEST CONDITIONS |  | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage |  |  | 3 | 5.5 | V |
| $V_O$ | Supply voltage to the output pins | OUT0–OUT15 |  |  | 17 | V |
| $I_O$ | Output current | DC test circuit | $V_O$ ≥ 0.6 V | 5 |  | mA |
|  |  |  | $V_O$ ≥ 1 V |  | 120 |  |
| $I_{OH}$ | High-level output current | SDO |  |  | −1 | mA |
| $I_{OL}$ | Low-level output current | SDO |  |  | 1 | mA |
| $V_{IH}$ | High-level input voltage | CLK, $\overline{OE}$(ED2), LE(ED1), and SDI |  | 0.7 × $V_{DD}$ | $V_{DD}$ | V |
| $V_{IL}$ | Low-level input voltage | CLK, $\overline{OE}$(ED2), LE(ED1), and SDI |  | 0 | 0.3 × $V_{DD}$ | V |

Product Folder Link(s): *TLC5926  TLC5927*

## Recommended Timing

$V_{DD}$ = 3 V to 5.5 V (unless otherwise noted)

| | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{w(L)}$ | LE(ED1) pulse duration | Normal mode | 20 | | ns |
| $t_{w(CLK)}$ | CLK pulse duration | Normal mode | 20 | | ns |
| $t_{w(OE)}$ | $\overline{OE}$(ED2) pulse duration | Normal mode | 1000 | | ns |
| $t_{su(D)}$ | Setup time for SDI | Normal mode | 7 | | ns |
| $t_{h(D)}$ | Hold time for SDI | Normal mode | 3 | | ns |
| $t_{su(L)}$ | Setup time for LE(ED1) | Normal mode | 18 | | ns |
| $t_{h(L)}$ | Hold time for LE(ED1) | Normal mode | 18 | | ns |
| $t_{w(CLK)}$ | CLK pulse duration | Error Detection mode | 20 | | ns |
| $t_{w(ED2)}$ | $\overline{OE}$(ED2) pulse duration | Error Detection mode | 2000 | | ns |
| $t_{su(ED1)}$ | Setup time for LE(ED1) | Error Detection mode | 7 | | ns |
| $t_{h(ED1)}$ | Hold time for LE(ED1) | Error Detection mode | 10 | | ns |
| $t_{su(ED2)}$ | Setup time for $\overline{OE}$(ED2) | Error Detection mode | 7 | | ns |
| $t_{h(ED2)}$ | Hold time for $\overline{OE}$(ED2) | Error Detection mode | 10 | | ns |
| $f_{CLK}$ | Clock frequency | Cascade operation, $V_{DD}$ = 3 V to 5.5 V | | 30 | MHz |

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## Electrical Characteristics

$V_{DD}$ = 3 V, $T_J$ = –40°C to 125°C (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_O$ | Supply voltage to the output pins | | | | | 17 | V |
| $I_O$ | Output current | $V_O \geq$ 0.6 V | | 5 | | | mA |
| | | $V_O \geq$ 1 V | | | | 120 | |
| $V_{IH}$ | High-level input voltage | | | $0.7 \times V_{DD}$ | | $V_{DD}$ | V |
| $V_{IL}$ | Low-level input voltage | | | GND | | $0.3 \times V_{DD}$ | |
| $I_{leak}$ | Output leakage current | $V_{OH}$ = 17 V | $T_J$ = 25°C | | | 0.5 | μA |
| | | | $T_J$ = 125°C | | | 1 | |
| $V_{OH}$ | High-level output voltage | SDO, $I_{OL}$ = –1 mA | | $V_{DD}$ – 0.4 | | | V |
| $V_{OL}$ | Low-level output voltage | SDO, $I_{OH}$ = 1 mA | | | | 0.4 | V |
| $I_{O(1)}$ | Output current 1 | $V_{OUT}$ = 0.6 V, $R_{ext}$ = 720 Ω, CG = 0.992 | | | 26 | | mA |
| | Output current error, die-die | $I_{OL}$ = 26 mA, $V_O$ = 0.6 V, $R_{ext}$ = 720 Ω, $T_J$ = 25°C | | | | ±6 | % |
| | Output current error, channel-to-channel | $I_{OL}$ = 26 mA, $V_O$ = 0.6 V, $R_{ext}$ = 720 Ω, $T_J$ = 25°C | | | | ±6 | % |
| $I_{O(2)}$ | Output current 2 | $V_O$ = 0.8 V, $R_{ext}$ = 360 Ω, CG = 0.992 | | | 52 | | mA |
| | Output current error, die-die | $I_{OL}$ = 52 mA, $V_O$ = 0.8 V, $R_{ext}$ = 360 Ω, $T_J$ = 25°C | | | | ±6 | % |
| | Output current error, channel-to-channel | $I_{OL}$ = 52 mA, $V_O$ = 0.8 V, $R_{ext}$ = 360 Ω, $T_J$ = 25°C | | | | ±6 | % |
| $I_{OUT}$ vs $V_{OUT}$ | Output current vs output voltage regulation | $V_O$ = 1 V to 3 V, $I_O$ = 26 mA | | | ±0.1 | | %/V |
| $I_{OUT}$ vs $V_{DD}$ | Output current vs supply voltage | $V_{DD}$ = 3.0 V to 5.5 V, $I_O$ = 26 mA/120 mA | | | ±1 | | |
| | Pullup resistance | $\overline{OE}$(ED2) | | 250 | 500 | 800 | kΩ |
| | Pulldown resistance | LE(ED1) | | 250 | 500 | 800 | kΩ |
| $T_{sd}$ | Overtemperature shutdown[1] | | | 150 | 175 | 200 | °C |
| $T_{hys}$ | Restart temperature hysteresis | | | | 15 | | °C |
| $I_{OUT,Th}$ | Threshold current for open error detection | $I_{OUT,target}$ = 5 mA to 120 mA | | | $0.5 \times I_{target}$ | | % |
| $V_{OUT,TTh}$ | Trigger threshold voltage for short-error detection (TLC5927 only) | $I_{OUT,target}$ = 5 mA to 120 mA | | 2.4 | 2.6 | 3.1 | V |
| $V_{OUT,RTh}$ | Return threshold voltage for short-error detection (TLC5927 only) | $I_{OUT,target}$ = 5 mA to 120 mA | | 2.2 | | | V |
| $I_{DD}$ | Supply current | OUT0–OUT15 = off, $R_{ext}$ = Open, $\overline{OE}$ = $V_{IH}$ | | | | 10 | mA |
| | | OUT0–OUT15 = off, $R_{ext}$ = 720 Ω, $\overline{OE}$ = $V_{IH}$ | | | | 14 | |
| | | OUT0–OUT15 = off, $R_{ext}$ = 360 Ω, $\overline{OE}$ = $V_{IH}$ | | | | 18 | |
| | | OUT0–OUT15 = off, $R_{ext}$ = 180 Ω, $\overline{OE}$ = $V_{IH}$ | | | | 20 | |
| | | OUT0–OUT15 = on, $R_{ext}$ = 720 Ω, $\overline{OE}$ = $V_{IL}$ | | | | 14 | |
| | | OUT0–OUT15 = on, $R_{ext}$ = 360 Ω, $\overline{OE}$ = $V_{IL}$ | | | | 18 | |
| | | OUT0–OUT15 = on, $R_{ext}$ = 180 Ω, $\overline{OE}$ = $V_{IL}$ | | | | 20 | |

(1)  Specified by design

Product Folder Link(s): TLC5926  TLC5927

## Electrical Characteristics

$V_{DD}$ = 5.5 V, $T_J$ = –40°C to 125°C (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_O$ | Supply voltage to the output pins | | | | | 17 | V |
| $I_O$ | Output current | $V_O ≥ 0.6$ V | | 5 | | | mA |
| | | $V_O ≥ 1$ V | | | | 120 | |
| $V_{IH}$ | High-level input voltage | | | $0.7 × V_{DD}$ | | $V_{DD}$ | V |
| $V_{IL}$ | Low-level input voltage | | | GND | | $03 × V_{DD}$ | |
| $I_{leak}$ | Output leakage current | $V_{OH} = 17$ V | $T_J = 25°C$ | | | 0.5 | μA |
| | | | $T_J = 125°C$ | | | 1 | |
| $V_{OH}$ | High-level output voltage | SDO, $I_{OL} = −1$ mA | | $V_{DD} − 0.4$ | | | V |
| $V_{OL}$ | Low-level output voltage | SDO, $I_{OH} = 1$ mA | | | | 0.4 | V |
| $I_{O(1)}$ | Output current 1 | $V_{OUT} = 0.6$ V, $R_{ext} = 720$ Ω, CG = 0.992 | | | 26 | | mA |
| | Output current error, die-die | $I_{OL} = 26$ mA, $V_O = 0.6$ V, $R_{ext} = 720$ Ω, $T_J = 25°C$ | | | | ±6 | % |
| | Output current error, channel-to-channel | $I_{OL} = 26$ mA, $V_O = 0.6$ V, $R_{ext} = 720$ Ω, $T_J = 25°C$ | | | | ±6 | % |
| $I_{O(2)}$ | Output current 2 | $V_O = 0.8$ V, $R_{ext} = 360$ Ω, CG = 0.992 | | | 52 | | mA |
| | Output current error, die-die | $I_{OL} = 52$ mA, $V_O = 0.8$ V, $R_{ext} = 360$ Ω, $T_J = 25°C$ | | | | ±6 | % |
| | Output current error, channel-to-channel | $I_{OL} = 52$ mA, $V_O = 0.8$ V, $R_{ext} = 360$ Ω, $T_J = 25°C$ | | | | ±6 | % |
| $I_{OUT}$ vs $V_{OUT}$ | Output current vs output voltage regulation | $V_O = 1$ V to 3 V , $I_O = 26$ mA | | | ±0.1 | | %/V |
| $I_{OUT}$ vs $V_{DD}$ | Output current vs supply voltage | $V_{DD} = 3.0$ V to 5.5 V, $I_O = 26$ mA/120 mA | | | ±1 | | |
| | Pullup resistance | $\overline{OE}$(ED2), | | 250 | 500 | 800 | kΩ |
| | Pulldown resistance | LE(ED1), | | 250 | 500 | 800 | kΩ |
| $T_{sd}$ | Overtemperature shutdown[1] | | | 150 | 175 | 200 | °C |
| $T_{hys}$ | Restart temperature hysteresis | | | | 15 | | °C |
| $I_{OUT,Th}$ | Threshold current for open error detection | $I_{OUT,target} = 5$ mA to 120 mA | | | $0.5 × I_{target}$ | | % |
| $V_{OUT,TTh}$ | Trigger threshold voltage for short-error detection (TLC5927 only) | $I_{OUT,target} = 5$ mA to 120 mA | | 2.4 | 2.6 | 3.1 | V |
| $V_{OUT,RTh}$ | Return threshold voltage for short-error detection (TLC5927 only) | $I_{OUT,target} = 5$ mA to 120 mA | | 2.2 | | | V |
| $I_{DD}$ | Supply current | OUT0–OUT15 = off, $R_{ext}$ = Open, $\overline{OE}$ = $V_{IH}$ | | | | 11 | mA |
| | | OUT0–OUT15 = off, $R_{ext} = 720$ Ω, $\overline{OE}$ = $V_{IH}$ | | | | 17 | |
| | | OUT0–OUT15 = off, $R_{ext} = 360$ Ω, $\overline{OE}$ = $V_{IH}$ | | | | 18 | |
| | | OUT0–OUT15 = off, $R_{ext} = 180$ Ω, $\overline{OE}$ = $V_{IH}$ | | | | 25 | |
| | | OUT0–OUT15 = on, $R_{ext} = 720$ Ω, $\overline{OE}$ = $V_{IL}$ | | | | 17 | |
| | | OUT0–OUT15 = on, $R_{ext} = 360$ Ω, $\overline{OE}$ = $V_{IL}$ | | | | 18 | |
| | | OUT0–OUT15 = on, $R_{ext} = 180$ Ω, $\overline{OE}$ = $V_{IL}$ | | | | 25 | |

(1)  Specified by design

Product Folder Link(s): *TLC5926  TLC5927*

## Switching Characteristics

$V_{DD}$ = 3 V, $T_J$ = −40°C to 125°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH1}$ | Low-to-high propagation delay time, CLK to OUTn | | 35 | 65 | 105 | ns |
| $t_{PLH2}$ | Low-to-high propagation delay time, LE(ED1) to OUTn | | 35 | 65 | 105 | ns |
| $t_{PLH3}$ | Low-to-high propagation delay time, $\overline{OE}$(ED2) to OUTn | | 35 | 65 | 105 | ns |
| $t_{PLH4}$ | Low-to-high propagation delay time, CLK to SDO | | | 20 | 45 | ns |
| $t_{PHL1}$ | High-to-low propagation delay time, CLK to OUTn | | 200 | 300 | 470 | ns |
| $t_{PHL2}$ | High-to-low propagation delay time, LE(ED1) to OUTn | | 200 | 300 | 470 | ns |
| $t_{PHL3}$ | High-to-low propagation delay time, $\overline{OE}$(ED2) to OUTn | | 200 | 300 | 470 | ns |
| $t_{PHL4}$ | High-to-low propagation delay time, CLK to SDO | | | 20 | 40 | ns |
| $t_{w(CLK)}$ | Pulse duration, CLK | | 20 | | | ns |
| $t_{w(L)}$ | Pulse duration LE(ED1) | $V_{IH} = V_{DD}$, $V_{IL}$ = GND, $R_{ext}$ = 360 Ω, $V_L$ = 4 V, $R_L$ = 44 Ω, $C_L$ = 70 pF, CG = 0.992 | 20 | | | ns |
| $t_{w(OE)}$ | Pulse duration, $\overline{OE}$(ED2) | | 1000 | | | ns |
| $t_{w(ED2)}$ | Pulse duration, $\overline{OE}$(ED2) in Error Detection mode | | 2 | | | μs |
| $t_{h(ED1,ED2)}$ | Hold time, LE(ED1), and $\overline{OE}$(ED2) | | 10 | | | ns |
| $t_{h(D)}$ | Hold time, SDI | | 5 | | | ns |
| $t_{su(D,ED1,ED2)}$ | Setup time, SDI, LE(ED1), and $\overline{OE}$(ED2) | | 7 | | | ns |
| $t_{h(L)}$ | Hold time, LE(ED1), Normal mode | | 18 | | | ns |
| $t_{su(L)}$ | Setup time, LE(ED1), Normal mode | | 18 | | | ns |
| $t_r$ | Rise time, CLK[1] | | | | 500 | ns |
| $t_f$ | Fall time, CLK[1] | | | | 500 | ns |
| $t_{or}$ | Rise time, outputs (off) | | | | 245 | ns |
| $t_{of}$ | Rise time, outputs (on) | | | | 600 | ns |
| $f_{CLK}$ | Clock frequency | Cascade operation | | | 30 | MHz |

(1) If the devices are connected in cascade and $t_r$ or $t_f$ is large, it may be critical to achieve the timing required for data transfer between two cascaded devices.

Product Folder Link(s): *TLC5926  TLC5927*

## Switching Characteristics

$V_{DD}$ = 5.5 V, $T_J$ = –40°C to 125°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH1}$ | Low-to-high propagation delay time, CLK to OUTn | | 27 | 65 | 95 | ns |
| $t_{PLH2}$ | Low-to-high propagation delay time, LE(ED1) to OUTn | | 27 | 65 | 95 | ns |
| $t_{PLH3}$ | Low-to-high propagation delay time, $\overline{OE}$(ED2) to OUTn | | 27 | 65 | 95 | ns |
| $t_{PLH4}$ | Low-to-high propagation delay time, CLK to SDO | | | 20 | 30 | ns |
| $t_{PHL1}$ | High-to-low propagation delay time, CLK to OUTn | | 180 | 300 | 445 | ns |
| $t_{PHL2}$ | High-to-low propagation delay time, LE(ED1) to OUTn | | 180 | 300 | 445 | ns |
| $t_{PHL3}$ | High-to-low propagation delay time, $\overline{OE}$(ED2) to OUTn | | 180 | 300 | 445 | ns |
| $t_{PHL4}$ | High-to-low propagation delay time, CLK to SDO | | | 20 | 30 | ns |
| $t_{w(CLK)}$ | Pulse duration, CLK | | 20 | | | ns |
| $t_{w(L)}$ | Pulse duration LE(ED1) | $V_{IH}$ = $V_{DD}$, $V_{IL}$ = GND, $R_{ext}$ = 360 Ω, $V_L$ = 4 V, $R_L$ = 44 Ω, $C_L$ = 70 pF, CG = 0.992 | 20 | | | ns |
| $t_{w(OE)}$ | Pulse duration, $\overline{OE}$(ED2) | | 1000 | | | ns |
| $t_{w(ED2)}$ | Pulse duration, $\overline{OE}$(ED2) in Error Detection mode | | 2 | | | µs |
| $t_{h(ED1,ED2)}$ | Hold time, LE(ED1), and $\overline{OE}$(ED2) | | 10 | | | ns |
| $t_{h(D)}$ | Hold time, SDI | | 3 | | | ns |
| $t_{su(D,ED1,ED2)}$ | Setup time, SDI, LE(ED1), and $\overline{OE}$(ED2) | | 4 | | | ns |
| $t_{h(L)}$ | Hold time, LE(ED1), Normal mode | | 15 | | | ns |
| $t_{su(L)}$ | Setup time, LE(ED1), Normal mode | | 15 | | | ns |
| $t_r$ | Rise time, CLK[1] | | | | 500 | ns |
| $t_f$ | Fall time, CLK[1] | | | | 500 | ns |
| $t_{or}$ | Rise time, outputs (off) | | | | 245 | ns |
| $t_{of}$ | Rise time, outputs (on) | | | | 570 | ns |
| $f_{CLK}$ | Clock frequency | Cascade operation | | | 30 | MHz |

(1) If the devices are connected in cascade and $t_r$ or $t_f$ is large, it may be critical to achieve the timing required for data transfer between two cascaded devices.

## PARAMETER MEASUREMENT INFORMATION
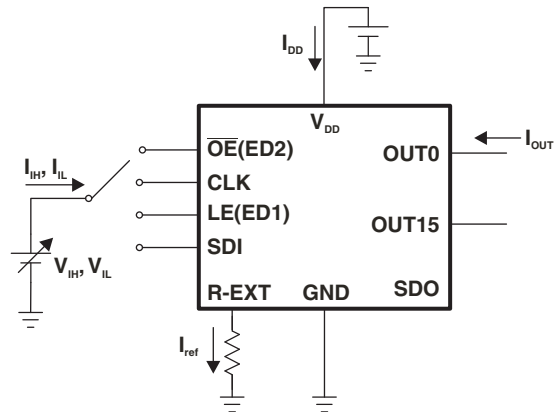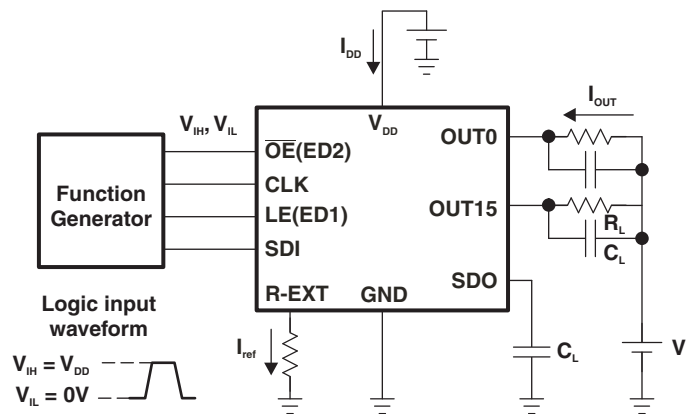


**Figure 6. Test Circuit for Electrical Characteristics**



**Figure 7. Test Circuit for Switching Characteristics**

Product Folder Link(s): *TLC5926  TLC5927*

## PARAMETER MEASUREMENT INFORMATION (continued)
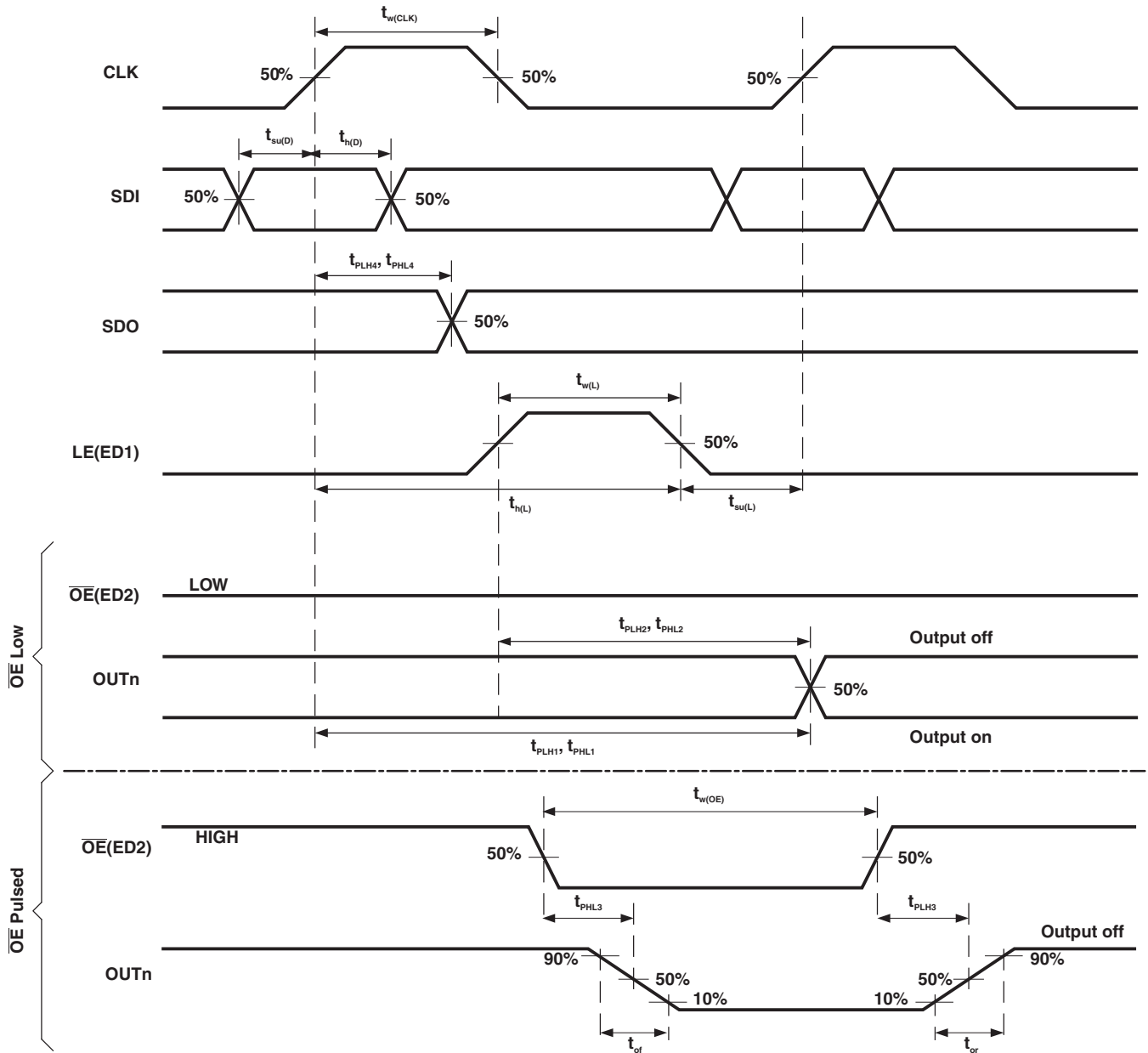


**Figure 8. Normal Mode Timing Waveforms**

Product Folder Link(s): *TLC5926  TLC5927*

## PARAMETER MEASUREMENT INFORMATION (continued)
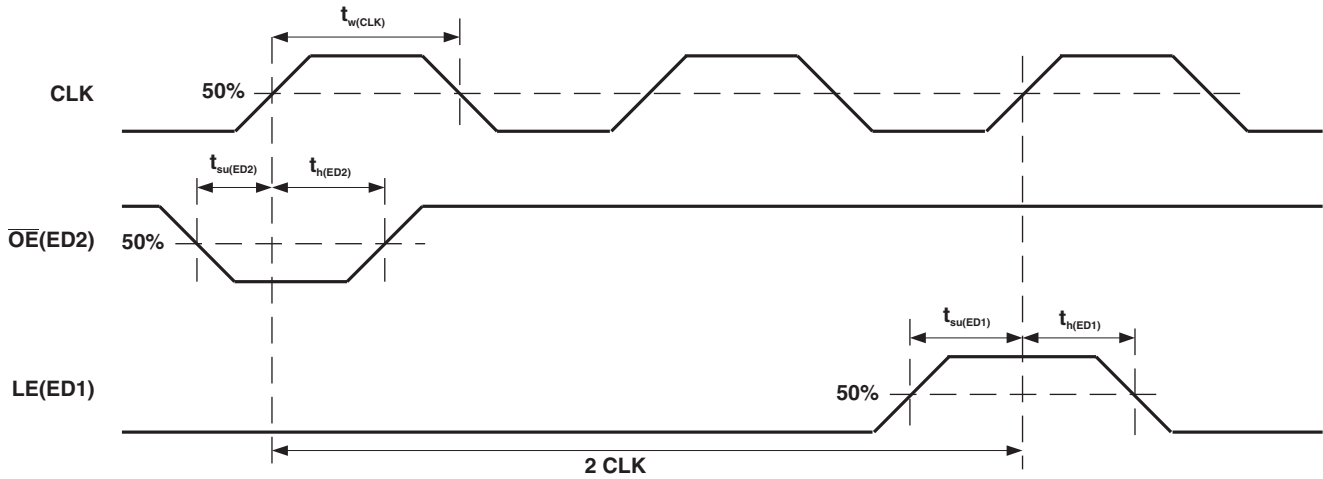


**Figure 9. Switching to Special Mode Timing Waveforms**
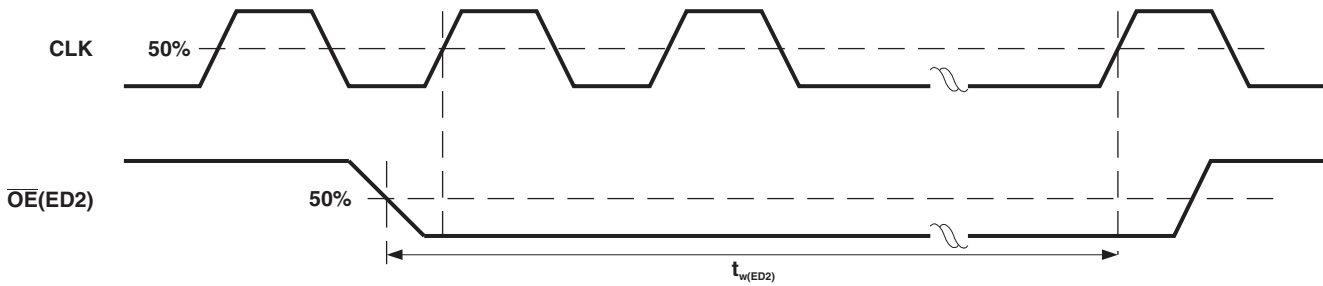


**Figure 10. Reading Error Status Code Timing Waveforms**

Product Folder Link(s): *TLC5926  TLC5927*

# APPLICATION INFORMATION

## Operating Principles

### Constant Current

In LED display applications, TLC5926/TLC5927 provides nearly no current variations from channel to channel and from IC to IC. While $I_{OUT}$ ≤ 50 mA, the maximum current skew between channels is less than ±6% and between ICs is less than ±6%.

### Adjusting Output Current

TLC5926/TLC5927 scales up the reference current, $I_{ref}$, set by the external resistor $R_{ext}$ to sink a current, $I_{out}$, at each output port. Users can follow the below formulas to calculate the target output current $I_{OUT,target}$ in the saturation region:

$V_{R\text{-}EXT}$ = 1.26 V × VG

$I_{ref}$ = $V_{R\text{-}EXT}$/$R_{ext}$, if another end of the external resistor $R_{ext}$ is connected to ground.

$I_{OUT,target}$ = $I_{ref}$ × 15 × $3^{CM-1}$

Where $R_{ext}$ is the resistance of the external resistor connected to the R-EXT terminal, and $V_{R\text{-}EXT}$ is the voltage of R-EXT, which is controlled by the programmable voltage gain (VG), which is defined by the Configuration Code. The Current Multiplier (CM) determines that the ratio $I_{OUT,target}$/$I_{ref}$ is 15 or 5. After power on, the default value of VG is 127/128 = 0.992, and the default value of CM is 1, so that the ratio $I_{OUT,target}$/$I_{ref}$ = 15. Based on the default VG and CM.

$V_{R\text{-}EXT}$ = 1.26 V × 127/128 = 1.25 V

$I_{OUT,target}$ = (1.25 V/$R_{ext}$) × 15

Therefore, the default current is approximately 52 mA at 360 Ω and 26 mA at 720 Ω. The default relationship after power on between $I_{OUT,target}$ and $R_{ext}$ is shown in Figure 11.
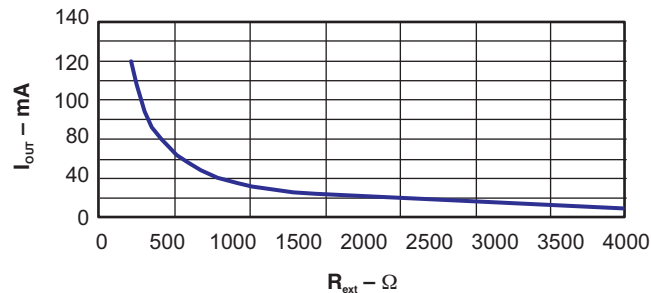


**Figure 11. Default Relationship Curve Between $I_{OUT,target}$ and $R_{ext}$**

Product Folder Link(s): *TLC5926  TLC5927*

## Operation Phases

### Operation Mode Switching

In order to switch between its two modes, TLC5926/TLC5927 monitors the signal $\overline{OE}$(ED2). When a one-clock-wide pulse of $\overline{OE}$(ED2) appears, TLC5926/TLC5927 enters the two-clock-period transition phase, the Mode Switching phase. After power on, the default operation mode is the Normal Mode (see Figure 12).
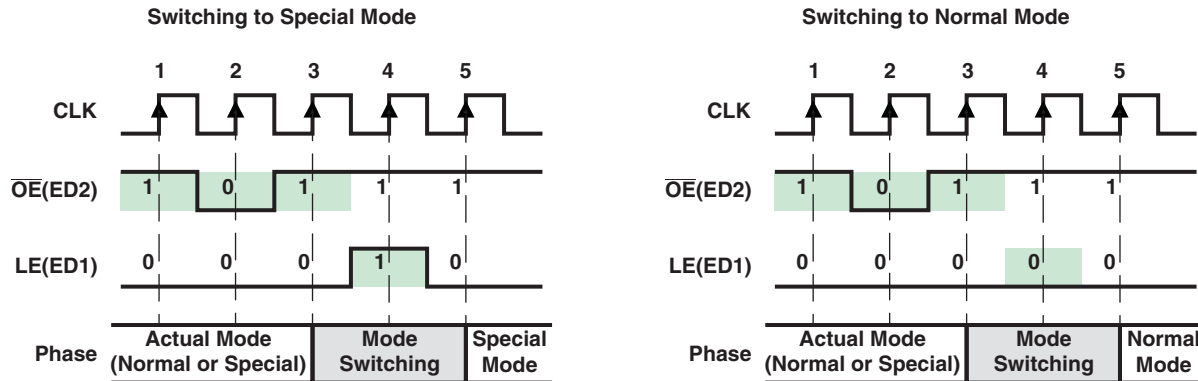


**Figure 12. Mode Switching**

As shown in Figure 12, once a one-clock-wide short pulse (101) of $\overline{OE}$(ED2) appears, TLC5926/TLC5927 enters the Mode Switching phase. At the fourth rising edge of CLK, if LE(ED1) is sampled as voltage high, TLC5926/TLC5927 switches to Special mode; otherwise, it switches to Normal mode.The signal LE(ED1) between the third and the fifth rising edges of CLK cannot latch any data. Its level is used only to determine into which mode to switch. However, the short pulse of $\overline{OE}$(ED2) can still enable the output ports. During mode switching, the serial data can still be transferred through SDI and shifted out from SDO.

NOTES:
1. The signal sequence for the mode switching may be used frequently to ensure that the TLC5926/TLC5927 is in the proper mode.
2. The 1 and 0 on the LE(ED1) signal are sampled at the rising edge of CLK. The X means its level does not affect the result of mode switching mechanism.
3. After power on, the default operation mode is Normal mode.

### Normal Mode Phase

Serial data is transferred into TLC5926/TLC5927 via SDI, shifted in the Shift Register, and output via SDO. LE(ED1) can latch the serial data in the Shift Register to the Output Latch. $\overline{OE}$(ED2) enables the output drivers to sink current. These functions differ only as described in Operation Mode Switching, in which case, a short pulse triggers TLC5926/TLC5927 to switch the operation mode. However, as long as LE(ED1) is high in the Mode Switching phase, TLC5926/TLC5927 remains in the Normal mode, as if no mode switching occurred.

### Special Mode Phase

In the Special mode, as long as $\overline{OE}$(ED2) is not low, the serial data is shifted to the Shift Register via SDI and shifted out via SDO, as in the Normal mode. However, there are two differences between the Special Mode and the Normal Mode, as shown in the following sections.

**Reading Error Status Code in Special Mode**

When $\overline{OE}$(ED2) is pulled low while in Special mode, error detection and load error status codes are loaded into the Shift Register, in addition to enabling output ports to sink current. Figure 13 shows the timing sequence for error detection. The 0 and 1 signal levels are sampled at the rising edge of each CLK. At least three zeros must be sampled at the voltage low signal $\overline{OE}$(ED2). Immediately after the second 0 is sampled, the data input source of the Shift Register changes to the 16-bit parallel Error Status Code register, instead of from the serial data on SDI. Normally, the error status codes are generated at least 2 µs after the falling edge of $\overline{OE}$(ED2). The occurrence of the third or later 0 saves the detected error status codes into the Shift Register. Therefore, when $\overline{OE}$(ED2) is low, the serial data cannot be shifted into TLC5926/TLC5927 via SDI. When $\overline{OE}$(ED2) is pulled high, the data input source of the Shift Register is changed back to SDI. At the same time, the output ports are disabled and the error detection is completed. Then, the error status codes saved in the Shift Register can be shifted out via SDO bit-by-bit along with CLK, as well as the new serial data can be shifted into TLC5926/TLC5927 via SDI.

While in Special mode, the TLC5926/TLC5927 cannot simultaneously transfer serial data and detect LED load error status.
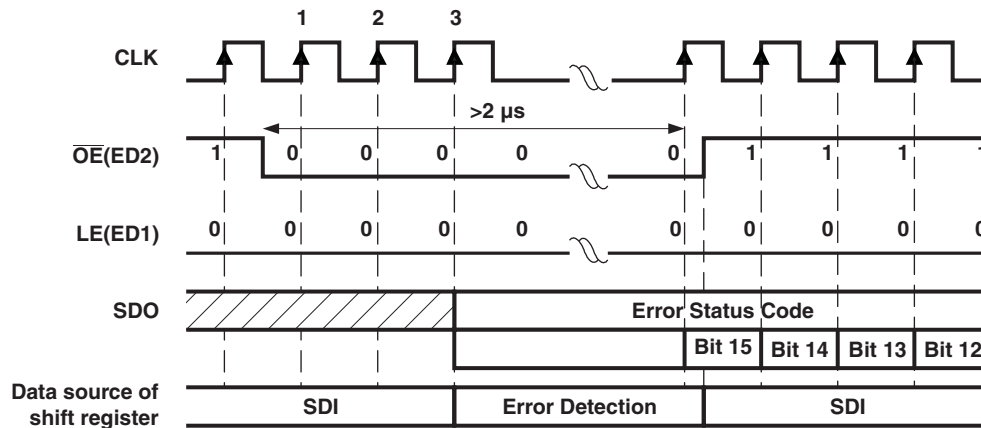


**Figure 13. Reading Error Status Code**

**Writing Configuration Code in Special Mode**

When in Special mode, the active high signal LE(ED1) latches the serial data in the Shift Register to the Configuration Latch, instead of the Output Latch. The latched serial data is used as the Configuration Code.

The code is stored until power off or the Configuration Latch is rewritten. As shown in Figure 14, the timing for writing the Configuration Code is the same as the timing in the Normal Mode to latching output channel data. Both the Configuration Code and Error Status Code are transferred in the common 16-bit Shift Register. Users must pay attention to the sequence of error detection and current adjustment to avoid the Configuration Code being overwritten by Error Status Code.
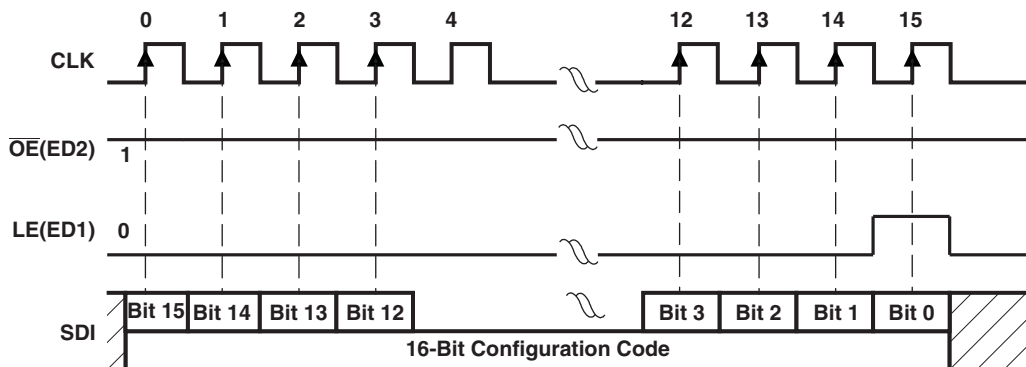


**Figure 14. Writing Configuration Code**

Product Folder Link(s): *TLC5926  TLC5927*

## Open-Circuit Detection Principle

The LED Open-Circuit Detection compares the effective current level $I_{OUT}$ with the open load detection threshold current $I_{OUT,Th}$. If $I_{OUT}$ is below the $I_{OUT,Th}$ threshold, the TLC5926/TLC5927 detects an open-load condition. This error status can be read as an error status code in the Special mode. For open-circuit error detection, a channel must be on.

**Table 1. Open-Circuit Detection**

| STATE OF OUTPUT PORT | CONDITION OF OUTPUT CURRENT | ERROR STATUS CODE | MEANING |
|---|---|---|---|
| Off | $I_{OUT}$ = 0 mA | 0 | Detection not possible |
| On | $I_{OUT} < I_{OUT,Th}$[1] | 0 | Open circuit |
| | $I_{OUT} \geq I_{OUT,Th}$[1] | Channel n error status bit 1 | Normal |

(1)  $I_{OUT,Th} = 0.5 \times I_{OUT,target}$ (typical)

## Short-Circuit Detection Principle (TLC5927 Only)

The LED short-circuit detection compares the effective voltage level $V_{OUT}$ with the shorted-load detection threshold voltages $V_{OUT,TTh}$ and $V_{OUT,RTh}$. If $V_{OUT}$ is above the $V_{OUT,TTh}$ threshold, the TLC5927 detects an shorted-load condition. If the $V_{OUT}$ is below $V_{OUT,RTh}$ threshold, no error is detected and the error bit is reset. This error status can be read as an error status code in the Special mode. For short-circuit error detection, a channel must be on.

**Table 2. Short-Circuit Detection**

| STATE OF OUTPUT PORT | CONDITION OF OUTPUT VOLTAGE | ERROR STATUS CODE | MEANING |
|---|---|---|---|
| Off | $I_{OUT}$ = 0 mA | 0 | Detection not possible |
| On | $V_{OUT} < V_{OUT,TTh}$[1] | 0 | Short circuit |
| | $V_{OUT} < V_{OUT,RTh}$[1] | Channel n error status bit 1 | Normal |

(1)  $I_{OUT,Th} = 0.5 \times I_{OUT,target}$ (typical)

## Overtemperature Detection and Shutdown

The TLC5926/TLC5927 is equipped with a global overtemperature sensor and 16 individual, channel-specific overtemperature sensors.

- When the global sensor reaches the trip temperature, all output channels are shutdown, and the error status is stored in the internal Error Status register of every channel. After shutdown, the channels automatically restart after cooling down, if the control signal (output latch) remains on. The stored error status is not reset after cooling down and can be read out as the error status code in the Special mode.

- When one of the channel-specific sensors reaches trip temperature, only the affected output channel is shut down, and the error status is stored only in the internal Error Status register of the affected channel. After shutdown, the channel automatically restarts after cooling down, if the control signal (output latch) remains on. The stored error status is not reset after cooling down and can be read out as error status code in the Special mode.

For channel-specific overtemperature error detection, a channel must be on.

The error status code is reset when the TLC5926/TLC5927 returns to Normal mode.

**Table 3. Overtemperature Detection[1]**

| STATE OF OUTPUT PORT | CONDITION | ERROR STATUS CODE | MEANING |
|---|---|---|---|
| Off | $I_{OUT}$ = 0 mA | 0 | |
| On<br>On → all channels<br>Off | $T_j < T_{j,trip}$ global | 1 | Normal |
| | $T_j > T_{j,trip}$ global | All error status bits = 0 | Global overtemperature |
| On<br>On → Off | $T_j < T_{j,trip}$ channel n | 1 | Normal |
| | $T_j > T_{j,trip}$ channel n | Channel n error status bit = 0 | Channel n overtemperature |

(1) The global shutdown threshold temperature is approximately 170°C.

## 16-Bit Configuration Code and Current Gain

Bit definition of the Configuration Code in the Configuration Latch is shown in Table 4.

**Table 4. Bit Definition of 8-Bit Configuration Code**

| | Bit 0 | Bit 1 | Bit 2 | Bit 3 | Bit 4 | Bit 5 | Bit 6 | Bit 7 | Bit 8–15 |
|---|---|---|---|---|---|---|---|---|---|
| Meaning | CM | HC | CC0 | CC1 | CC2 | CC3 | CC4 | CC5 | Don't care |
| Default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | X |

Bit 7 is first sent into TLC5926/TLC5927 via SDI. Bits 1 to 7 {HC, CC[0:5]} determine the voltage gain (VG) that affects the voltage at R-EXT and indirectly affects the reference current, $I_{ref}$, flowing through the external resistor at R-EXT. Bit 0 is the Current Multiplier (CM) that determines the ratio $I_{OUT,target}/I_{ref}$. Each combination of VG and CM gives a specific Current Gain (CG).

- VG: the relationship between {HC,CC[0:5]} and the voltage gain is calculated as shown below:

  VG = (1 + HC) × (1 + D/64) / 4

  $D = CC0 \times 2^5 + CC1 \times 2^4 + CC2 \times 2^3 + CC3 \times 2^2 + CC4 \times 2^1 + CC5 \times 2^0$

  Where HC is 1 or 0, and D is the binary value of CC[0:5]. So, the VG could be regarded as a floating-point number with 1-bit exponent HC and 6-bit mantissa CC[0:5]. {HC,CC[0:5]} divides the programmable voltage gain VG into 128 steps and two sub-bands:

  Low voltage sub-band (HC = 0): VG = 1/4 ~ 127/256, linearly divided into 64 steps

  High voltage sub-band (HC = 1): VG = 1/2 ~ 127/128, linearly divided into 64 steps

- CM: In addition to determining the ratio $I_{OUT,target}/I_{ref}$, CM limits the output current range.

  High Current Multiplier (CM = 1): $I_{OUT,target}/I_{ref}$ = 15, suitable for output current range $I_{OUT}$ = 10 mA to 120 mA.

  Low Current Multiplier (CM = 0): $I_{OUT,target}/I_{ref}$ = 5, suitable for output current range $I_{OUT}$ = 5 mA to 40 mA

- CG: The total Current Gain is defined as the following.

  $V_{R-EXT}$ = 1.26 V × VG

  $I_{ref} = V_{R-EXT}/R_{ext}$, if the external resistor, $R_{ext}$, is connected to ground.

  $I_{OUT,target} = I_{ref} \times 15 \times 3^{CM-1}$ = 1.26 V/$R_{ext}$ × VG × 15 × $3^{CM-1}$ = (1.26 V/$R_{ext}$ × 15) × CG

  $CG = VG \times 3^{CM-1}$

  Therefore, CG = (1/12) to (127/128) divided into 256 steps.

**Examples**

- Configuration Code {CM, HC, CC[0:5]} = {1,1,111111}

  $VG = 127/128 = 0.992$ and $CG = VG \times 3^0 = VG = 0.992$
- Configuration Code = {1,1,000000}

  VG = (1 + 1) × (1 + 0/64)/4 = 1/2 = 0.5, and CG = 0.5
- Configuration Code = {0,0,000000}

  VG = (1 + 0) × (1 + 0/64)/4 = 1/4, and $CG = (1/4) \times 3^{-1} = 1/12$

After power on, the default value of the Configuration Code {CM, HC, CC[0:5]} is {1,1,111111}. Therefore, VG = CG = 0.992. The relationship between the Configuration Code and the Current Gain is shown in Figure 15.
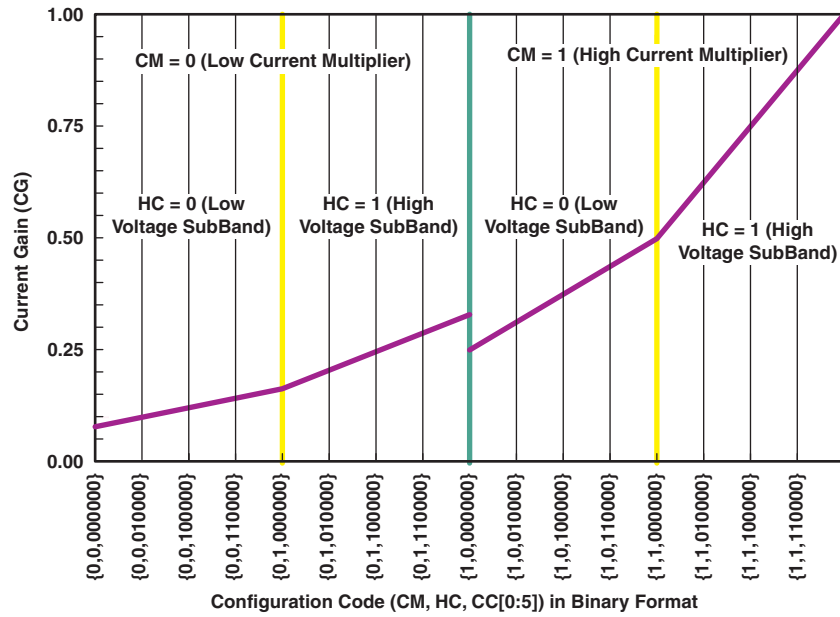
**Figure 15. Current Gain vs Configuration Code**

## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/ Ball Finish | MSL Peak Temp [3] | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| TLC5926IDBQR | ACTIVE | SSOP | DBQ | 24 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| TLC5926IDBQRG4 | ACTIVE | SSOP | DBQ | 24 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| TLC5926IDWR | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TLC5926IPWPR | ACTIVE | HTSSOP | PWP | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| TLC5926IPWPRG4 | ACTIVE | HTSSOP | PWP | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| TLC5927IDBQR | ACTIVE | SSOP | DBQ | 24 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| TLC5927IDBQRG4 | ACTIVE | SSOP | DBQ | 24 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| TLC5927IDWR | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TLC5927IPWPR | ACTIVE | HTSSOP | PWP | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| TLC5927IPWPRG4 | ACTIVE | HTSSOP | PWP | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |

**[1]** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**[2]** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br)  and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**OTHER QUALIFIED VERSIONS OF TLC5926, TLC5927 :**

● Automotive: TLC5926-Q1, TLC5927-Q1

NOTE: Qualified Version Definitions:

　　　● Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**TAPE AND REEL INFORMATION**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLC5926IDBQR | SSOP | DBQ | 24 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLC5926IDWR | SOIC | DW | 24 | 2000 | 330.0 | 24.4 | 10.75 | 15.7 | 2.7 | 12.0 | 24.0 | Q1 |
| TLC5926IPWPR | HTSSOP | PWP | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |
| TLC5927IDBQR | SSOP | DBQ | 24 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLC5927IDWR | SOIC | DW | 24 | 2000 | 330.0 | 24.4 | 10.75 | 15.7 | 2.7 | 12.0 | 24.0 | Q1 |
| TLC5927IPWPR | HTSSOP | PWP | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLC5926IDBQR | SSOP | DBQ | 24 | 2500 | 367.0 | 367.0 | 38.0 |
| TLC5926IDWR | SOIC | DW | 24 | 2000 | 367.0 | 367.0 | 45.0 |
| TLC5926IPWPR | HTSSOP | PWP | 24 | 2000 | 367.0 | 367.0 | 38.0 |
| TLC5927IDBQR | SSOP | DBQ | 24 | 2500 | 367.0 | 367.0 | 38.0 |
| TLC5927IDWR | SOIC | DW | 24 | 2000 | 367.0 | 367.0 | 45.0 |
| TLC5927IPWPR | HTSSOP | PWP | 24 | 2000 | 367.0 | 367.0 | 38.0 |

DW (R−PDSO−G24)                                    PLASTIC SMALL OUTLINE



0.614 (15,60)
0.598 (15,20)

24                                          13

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

1                                           12

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ | 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040000−5/G 01/11

NOTES:   A.   All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MS−013 variation AD.

DW (R−PDSO−G24)                                   PLASTIC SMALL OUTLINE
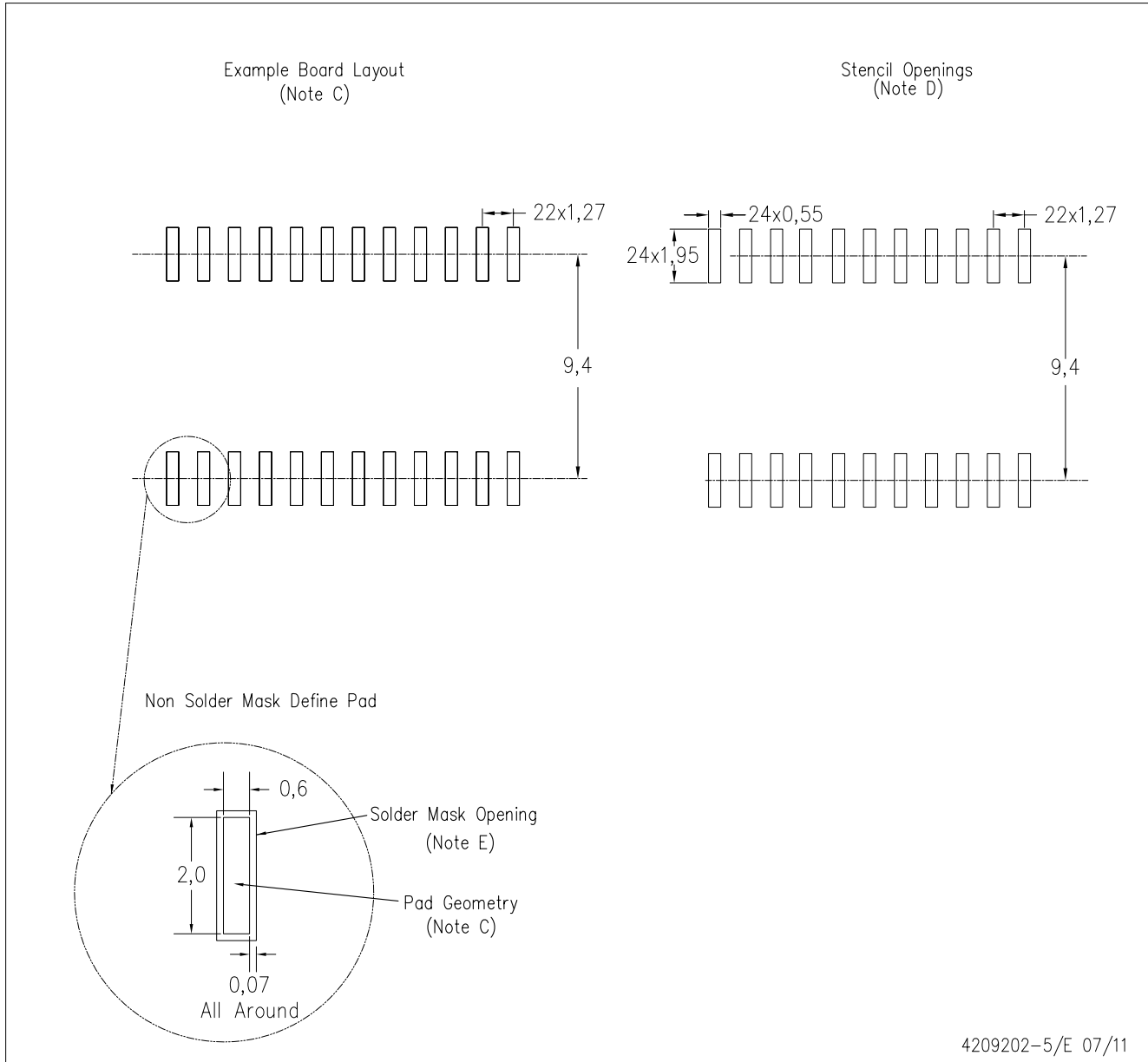
Example Board Layout
(Note C)

Stencil Openings
(Note D)

22x1,27

24x0,55          22x1,27

24x1,95

9,4

9,4

Non Solder Mask Define Pad

0,6

2,0

Solder Mask Opening
(Note E)

Pad Geometry
(Note C)

0,07
All Around

4209202−5/E 07/11

NOTES:   A.  All linear dimensions are in millimeters.
         B.  This drawing is subject to change without notice.
         C.  Refer to IPC7351 for alternate board design.
         D.  Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
             contact their board assembly site for stencil design recommendations.  Refer to IPC−7525
         E.  Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DBQ (R−PDSO−G24)                    PLASTIC SMALL−OUTLINE PACKAGE

0.344 (8,75)
0.337 (8,55)

24                                    13

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

Pin 1
Index Area

1                                     12

0.025 (0,635)

0.012 (0,30)
0.008 (0,20)

⊕ 0.005 (0,13) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)        0°−8°

0.035 (0,89)
0.016 (0,40)

4073301−4/H   10/2008

NOTES:  A.  All linear dimensions are in inches (millimeters).
        B.  This drawing is subject to change without notice.
        C.  Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
        D.  Falls within JEDEC MO−137 variation AE.

DBQ (R−PDSO−G24)         PLASTIC SMALL OUTLINE PACKAGE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

24x0,35 →| |←          →| |←22x0,635

5,2

→| |← 24x0,3          →| |←22x0,635

24x1,75

5,2

|← 0,35

1,90    1,8    — Solder Mask Opening

— Pad Geometry

0,05

0,40

4210335−4/C 07/11

NOTES:    A.    All linear dimensions are in millimeters.
          B.    This drawing is subject to change without notice.
          C.    Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
          D.    Publication IPC−7351 is recommended for alternate designs.
          E.    Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
                contact their board assembly site for stencil design recommendations.  Example stencil design based on a 50% volumetric
                metal load solder paste.  Refer to IPC−7525 for other stencil recommendations.

PWP (R−PDSO−G24)  PowerPAD™ PLASTIC SMALL OUTLINE

0,65

0,30
0,19  ⊕ 0,10Ⓜ

24    13

THERMAL PAD

SIZE AND SHAPE
SHOWN ON
SEPARATE SHEET

4,50
4,30

6,60
6,20

1    12

7,90
7,70

0,15 NOM

Gauge Plane

Seating Plane

0,25

0°−8°

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

0,10

4073225−5/I 05/11

NOTES:   A.  All linear dimensions are in millimeters.
         B.  This drawing is subject to change without notice.
         C.  Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
         D.  This package is designed to be soldered to a thermal pad on the board.  Refer to Technical Brief, PowerPad
             Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding
             recommended board layout.  This document is available at www.ti.com <http://www.ti.com>.
         E.  See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
         E.  Falls within JEDEC MO−153

**PowerPAD is a trademark of Texas Instruments.**

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PWP (R−PDSO−G24)     PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions
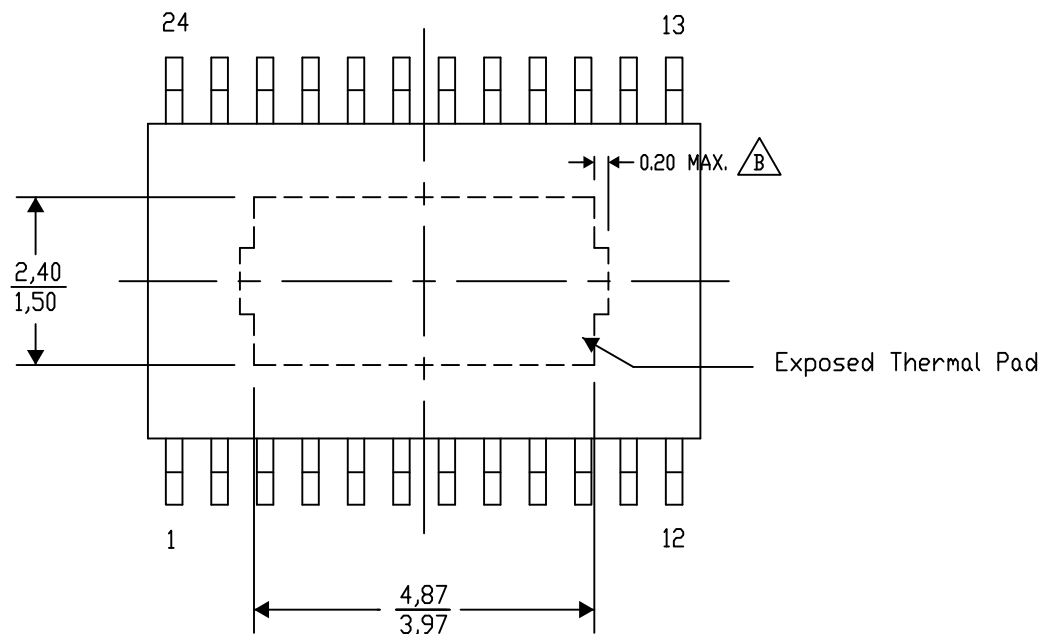
4206332−29/AC 07/12

NOTE:   A. All linear dimensions are in millimeters

/B\ Exposed tie strap features may not be present.

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## PWP (R-PDSO-G24)  PowerPAD™ PLASTIC SMALL OUTLINE

Example Board Layout
Via pattern and copper pad size
may vary depending on layout constraints

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).
Reference table below for other
solder stencil thicknesses

18x⌀0,3

15x1,3

22x0,65

Increasing copper area will
enhance thermal performance
(See Note D)

24x0,25

1,55

12x1,3

5,6

2,4  3,4

(See Note E)   Y   2,4

X

5,6

4,87

Solder mask
over copper

4,87

Example Solder Mask
Defined Pad
(See Note C, D)

22x0,65

7,8

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note F)

0,3

1,6

Pad Geometry

0,07
All Around

| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 5.4 | 2.6 |
| 0.127mm | 4.87 | 2.4 |
| 0.152mm | 4.6 | 2.2 |
| 0.178mm | 4.3 | 2.1 |

4207609-16/R 07/12

NOTES:  A.  All linear dimensions are in millimeters.
B.  This drawing is subject to change without notice.
C.  Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D.  This package is designed to be soldered to a thermal pad on the board.  Refer to Technical Brief, PowerPad
Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets
for specific thermal information, via requirements, and recommended board layout.  These documents are available at
www.ti.com <http://www.ti.com>.  Publication IPC-7351 is recommended for alternate designs.
E.  Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
contact their board assembly site for stencil design recommendations.  Example stencil design based on a 50% volumetric
metal load solder paste.  Refer to IPC-7525 for other stencil recommendations.
F.  Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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