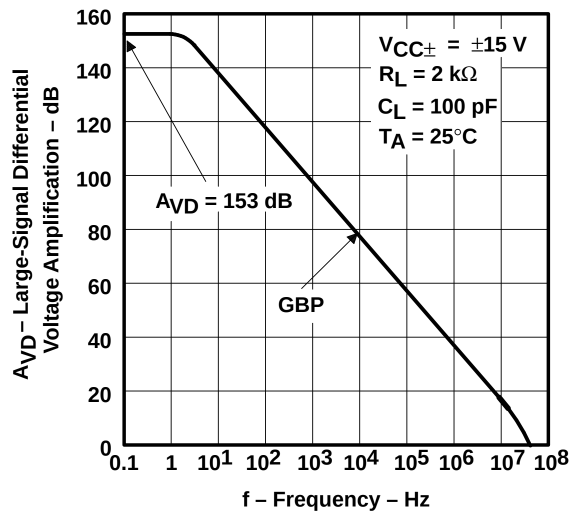
- **Outstanding Combination of DC Precision and AC Performance:**
  Gain-Bandwidth Product . . . 50 MHz Typ
  V_n . . . 3.3 nV/√Hz at f = 10 Hz Typ,
  2.5 nV/√Hz at f = 1 kHz Typ
  V_{IO} . . . 25 μV Max at T_A = 25°C
  A_{VD} . . . 45 V/μV Typ With R_L = 2 kΩ,
  19 V/μV Typ With R_L = 600 Ω
- **Available in Standard Pinout Small-Outline Package**
- **Output Features Saturation Recovery Circuitry**
- **Macromodels and Statistical information Included**

description

The TLE2037 and TLE2037A combine innovative circuit design expertise and high-quality process control techniques to produce a level of ac performance and dc precision previously unavailable in single operational amplifiers. Using the Texas Instruments state-of-the-art Excalibur process, these devices allow upgrades to systems that use lower-precision devices.

The TLE2037 and TLE2037A are decompensated versions of the TLE2027 and TLE2027A and are stable to a close-loop gain of 5. In the area of dc precision, these parts offer maximum offset voltages of 100 μV and 25 μV, respectively, common-mode rejection ratio of 131 dB (typ), supply voltage rejection ratio of 144 dB (typ), and dc gain of 45 V/μV (typ).

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY



The ac performance is highlighted by a typical gain-bandwidth product specification of 50 MHz, 50° of phase margin, and noise voltage specifications of 3.3 nV/√Hz and 2.5 nV/√Hz at frequencies of 10 Hz and 1 kHz, respectively.

Both the TLE2037 and TLE2037A are available in a wide variety of packages, including the industry-standard 8-pin small-outline version for high-density system applications. The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from – 40°C to 105°C. The M-suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C.

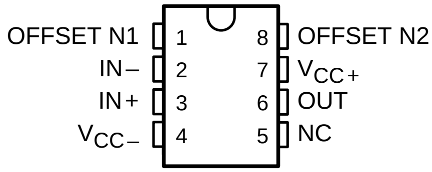
AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES				CHIP FORM (Y)
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	
0°C to 70°C	25 μV 100 μV	TLE2037ACD TLE2037CD	–	–	TLE2037ACP TLE2037CP	TLE2037Y –
−40°C to 105°C	25 μV 100 μV	TLE2037AID TLE2037ID	–	–	TLE2037AIP TLE2037IP	–
−55°C to 125°C	25 μV 100 μV	TLE2037AMD TLE2037MD	TLE2037AMFK TLE2037MFK	TLE2037AMJG TLE2037MJG	TLE2037AMP TLE2037MP	–

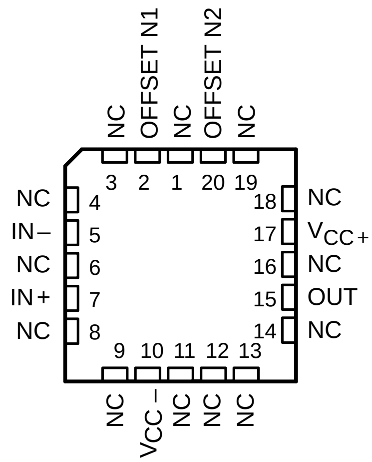
The D packages are available taped and reeled. Add R suffix to device type (e.g., TLE2037ACDR). Chips are tested at 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

D, JG, OR P PACKAGE
(TOP VIEW)

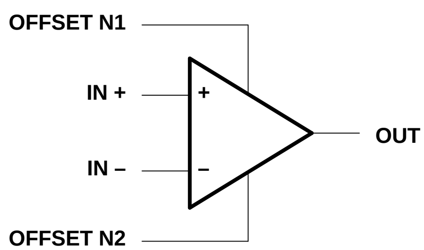


FK PACKAGE
(TOP VIEW)



NC – No internal connection

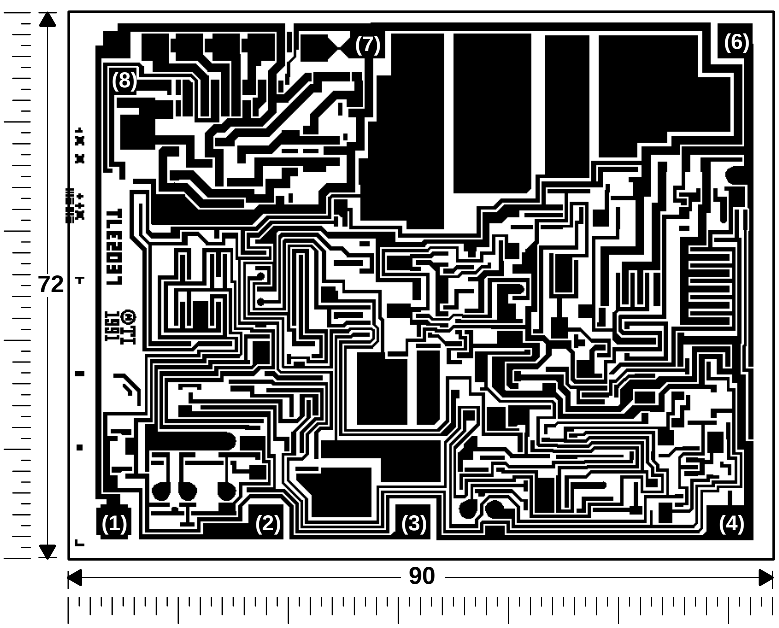
symbol

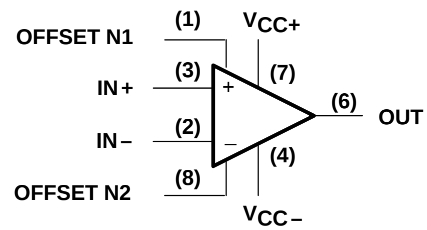


TLE2037 chip information

This chip, when properly assembled, displays characteristics similar to the TLE2037C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

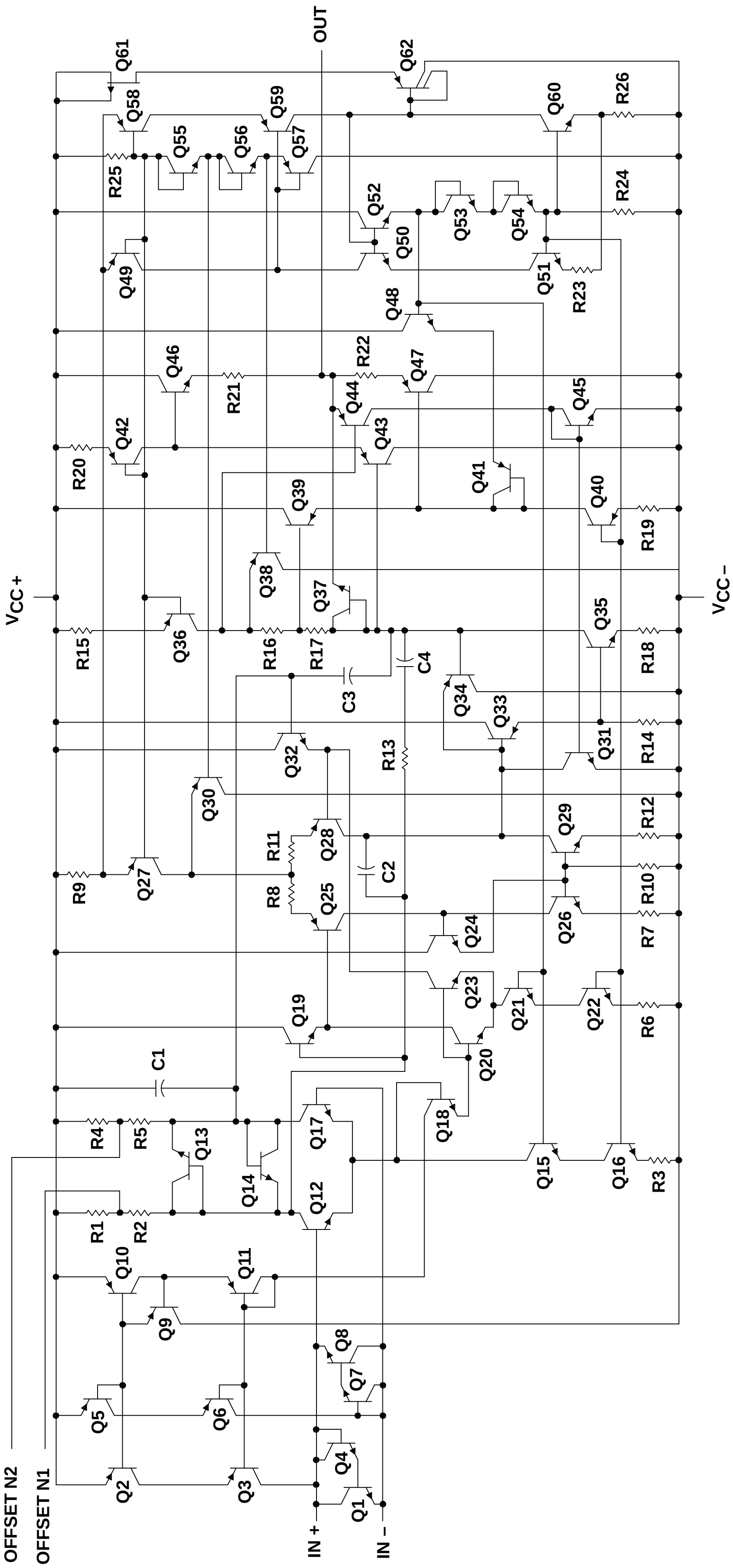
T_J max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

equivalent schematic



COMPONENT COUNT	
Transistors	61
Resistors	26
Capacitors	4
epi FET	1

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) . . . . 19 V
Supply voltage, V_{CC-} . . . . –19 V
Differential input voltage, V_{ID} (see Note 2) . . . . ±1.2 V
Input voltage range, V_I (any input) . . . . $\pm V_{CC}$
Input current, I_I (each input) . . . . ±1 mA
Output current, I_O . . . . ± 50 mA
Total current into V_{CC+} . . . . 50 mA
Total current out of V_{CC-} . . . . 50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . unlimited
Continuous total power dissipation . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix . . . . 0°C to 70°C
I suffix . . . . –40°C to 105°C
M suffix . . . . –55°C to 125°C
Storage temperature range . . . . –65°C to 150°C
Case temperature for 60 seconds: FK package . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN–. Excessive current will flow if a differential input voltage in excess of approximately ±1.2 V is applied between the inputs unless some limiting resistance is used.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 105°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	261 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	495 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	378 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	360 mW	200 mW

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		± 4	±19	± 4	±19	±4	±19	V
Common-mode input voltage, V_{IC}	T_A = 25°C	–11	11	–11	11	–11	11	V
	T_A = Full range†	–10.5	10.5	–10.4	10.4	–10.2	10.2	
Operating free-air temperature, T_A		0	70	–40	105	–55	125	°C

† Full range is 0°C to 70°C for C-suffix devices, –40°C to 105°C for the I-suffix devices, and –55°C to 125°C for the M-suffix devices.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2037C MIN	TLE2037C TYP	TLE2037C MAX	TLE2037AC MIN	TLE2037AC TYP	TLE2037AC MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		20	100		10	25	μV
			Full range			145			70	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.4	1		0.2	1	μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.006	1		0.006	1	μV/mo
I_{IO}	Input offset current		25°C		6	90		6	90	nA
			Full range			150			150	
I_{IB}	Input bias current		25°C		15	90		15	90	nA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	–11 to 11	–13 to 13		–11 to 11	–13 to 13		V
			Full range	–10.5 to 10.5			–10.5 to 10.5			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 600 Ω	25°C	10.5	12.9		10.5	12.9		V
			Full range	10			10			
		R_L = 2 kΩ	25°C	12	13.2		12	13.2		
			Full range	11			11			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 600 Ω	25°C	–10.5	–13		–10.5	–13		V
			Full range	–10			–10			
		R_L = 2 kΩ	25°C	–12	–13.5		–12	–13.5		
			Full range	11			11			
A_{VD}	Large-signal differential voltage amplification	V_O = ±11 V, R_L = 2 kΩ	25°C	5	45		10	45		V/μV
		V_O = ±10 V, R_L = 2 kΩ	Full range	2			4			
		V_O = ±10 V, R_L = 1 kΩ	25°C	3.5	38		8	38		
			Full range	1			2.5			
		V_O = ±10 V, R_L = 600 kΩ	25°C	2	19		5	19		
			Full range	0.5			2			
c_i	Input capacitance		25°C		8			8		pF
z_o	Open-loop output impedance	I_O = 0	25°C		50			50		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	100	131		117	131		dB
			Full range	98			114			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±4 V to ±18 V, R_S = 50 Ω	25°C	94	144		110	144		dB
		$V_{CC\pm}$ = ±4 V to ±18 V, R_S = 50 Ω	Full range	92			106			
I_{CC}	Supply current	V_O = 0, No load	25°C		3.8	5.3		3.8	5.3	mA
			Full range			5.6			5.6	

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm15$ V

PARAMETER		TEST CONDITIONS	T_A†	TLE2037C			TLE2037AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate	$A_{VD} = 5$, $R_L = 2$ kΩ, $C_L = 100$ pF, See Figure 1	25°C	6	7.5		6	7.5		V/μs
			Full range	5			5			
V_n	Equivalent input noise voltage (see Figure 2)	$R_S = 20$ Ω, f = 10 Hz	25°C		3.3	8		3.3	4.5	nV/√Hz
		$R_S = 20$ Ω, f = 1 kHz			2.5	4.5		2.5	3.8	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		50	250		50	130	nV
I_n	Equivalent input noise current	f = 10 Hz	25°C		1.5	4		1.5	4	pA/√Hz
		f = 1 kHz			0.4	0.6		0.4	0.6	
THD	Total harmonic distortion	$V_O = \pm10$ V, $A_{VD} = 5$, See Note 5	25°C		< 0.002%			< 0.002%		
	Gain-bandwidth product	f = 100 kHz, $R_L = 2$ kΩ, $C_L = 100$ pF	25°C	35	50		35	50		MHz
B_{OM}	Maximum output-swing bandwidth	$R_L = 2$ kΩ	25°C		80			80		kHz
ϕ_m	Phase margin	$R_L = 2$ kΩ, $C_L = 100$ pF	25°C		50°			50°		

† Full range is 0°C to 70°C.

NOTE 5: Measured distortion of the source used in the analysis was 0.002%.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2037I MIN	TLE2037I TYP	TLE2037I MAX	TLE2037AI MIN	TLE2037AI TYP	TLE2037AI MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		20	100		10	25	µV
			Full range			180			105	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.4	1		0.2	1	µV/°C
	Input bias voltage long-term drift (see Note 4)		25°C		0.006	1		0.006	1	µV/mo
I_{IO}	Input offset current		25°C		6	90		6	90	nA
			Full range			150			150	
I_{IB}	Input bias current		25°C		15	90		15	90	nA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	–11 to 11	–13 to 13		–11 to 11	–13 to 13		V
			Full range	–10.4 to 10.4			–10.4 to 10.4			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 600 Ω	25°C	10.5	12.9		10.5	12.9		V
			Full range	10			10			
		R_L = 2 kΩ	25°C	12	13.2		12	13.2		
			Full range	11			11			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 600 Ω	25°C	–10.5	–13		–10.5	–13		V
			Full range	–10			–10			
		R_L = 2 kΩ	25°C	–12	–13.5		–12	–13.5		
			Full range	–11			–11			
A_{VD}	Large-signal differential voltage amplification	V_O = ±11 V, R_L = 2 kΩ	25°C	5	45		10	45		V/µV
		V_O = ±10 V R_L = 2 kΩ	Full range	2.5			3.5			
		V_O = ±10 V, R_L = 1 kΩ	25°C	3.5	38		8	38		
			Full range	1.8			2.2			
		V_O = ±10 V, R_L = 600 Ω	25°C	2	19		5	19		
			Full range	0.5			1.1			
c_i	Input capacitance		25°C		8			8		pF
z_o	Open-loop output impedance	I_O = 0	25°C		50			50		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	100	131		117	131		dB
			Full range	96			113			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±4 V to ±18 V, R_S = 50 Ω	25°C	94	144		110	144		dB
		$V_{CC\pm}$ = ±4 V to ±18 V, R_S = 50 Ω	Full range	90			105			
I_{CC}	Supply current	V_O = 0, No load	25°C		3.8	5.3		3.8	5.3	mA
			Full range			5.6			5.6	

† Full range is –40°C to 105°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm15$ V

PARAMETER		TEST CONDITIONS	T_A†	TLE2037I MIN	TLE2037I TYP	TLE2037I MAX	TLE2037AI MIN	TLE2037AI TYP	TLE2037AI MAX	UNIT
SR	Slew rate	A_{VD} = 5, R_L = 2 kΩ, C_L = 100 pF, See Figure 1	25°C	6	7.5		6	7.5		V/μs
			Full range	4.7			4.7			
V_n	Equivalent input noise voltage (see Figure 2)	R_S = 20 Ω, f = 10 Hz	25°C		3.3	8		3.3	4.5	nV/√Hz
		R_S = 20 Ω, f = 1 kHz			2.5	4.5		2.5	3.8	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		50	250		50	130	nV
I_n	Equivalent input noise current	f = 10 Hz	25°C		1.5	4		1.5	4	pA/√Hz
		f = 1 kHz			0.4	0.6		0.4	0.6	
THD	Total harmonic distortion	V_O = ±10 V, A_{VD} = 5, See Note 5	25°C		< 0.002%			< 0.002%		
	Gain-bandwidth product	f = 100 kHz, R_L = 2 kΩ, C_L = 100 pF	25°C	35	50		35	50		MHz
B_{OM}	Maximum output-swing bandwidth	R_L = 2 kΩ	25°C		80			80		kHz
ϕ_m	Phase margin	R_L = 2 kΩ, C_L = 100 pF	25°C		50°			50°		

† Full range is –40°C to 105°C.

NOTE 5: Measured distortion of the source used in the analysis was 0.002%.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2037M MIN	TLE2037M TYP	TLE2037M MAX	TLE2037AM MIN	TLE2037AM TYP	TLE2037AM MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		20	100		10	25	μV
			Full range			200			105	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.4	1*		0.2	1*	μV/°C
	Input bias voltage long-term drift (see Note 4)		25°C		0.006	1		0.006	1	μV/mo
I_{IO}	Input offset current		25°C		6	90		6	90	nA
			Full range			150			150	
I_{IB}	Input bias current		25°C		15	90		15	90	nA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	–11 to 11	–13 to 13		–11 to 11	–13 to 13		V
			Full range	–10.3 to 10.3			–10.4 to 10.4			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 600\ \Omega$	25°C	10.5	12.9		10.5	12.9		V
			Full range	10			10			
		$R_L = 2\ k\Omega$	25°C	12	13.2		12	13.2		
			Full range	11			11			
		$R_L = 1\ k\Omega$	–55°C	10			10			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 600\ \Omega$	25°C	–10.5	–13		–10.5	–13		V
			Full range	–10			–10			
		$R_L = 2\ k\Omega$	25°C	–12	–13.5		–12	–13.5		
			Full range	–11			–11			
		$R_L = 1\ k\Omega$	–55°C	–10			–10			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm11$ V, $R_L = 2\ k\Omega$	25°C	5	45		10	45		V/μV
		$V_O = \pm10$ V, $R_L = 2\ k\Omega$	Full range	2.5			3.5			
		$V_O = \pm10$ V $R_L = 1\ k\Omega$	25°C	3.5	38		8	38		
			Full range	1.8			2.2			
		$V_O = \pm10$ V, $R_L = 600\ \Omega$	25°C	2	19		5	19		
c_i	Input capacitance		25°C		8			8		pF
z_o	Open-loop output impedance	$I_O = 0$	25°C		50			50		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$, $R_S = 50\ \Omega$	25°C	100	131		117	131		dB
			Full range	96			113			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm4$ V to ±18 V, $R_S = 50\ \Omega$	25°C	94	144		110	144		dB
		$V_{CC\pm} = \pm4$ V to ±18 V, $R_S = 50\ \Omega$	Full range	90			105			
I_{CC}	Supply current	$V_O = 0$, No load	25°C		3.8	5.3		3.8	5.3	mA
			Full range			5.6			5.6	

*On products compliant to MIL-PRF-38535, this parameter is not production tested.
† Full range is – 55°C to 125°C.
NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm15$ V

PARAMETER		TEST CONDITIONS	T_A†	TLE2037M			TLE2037AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate	A_{VD} = 5, R_L = 2 kΩ, C_L = 100 pF, See Figure 1	25°C	6*	7.5		6*	7.5		V/μs
			Full range	4.4*			4.4*			
V_n	Equivalent input noise voltage (see Figure 2)	R_S = 20 Ω, f = 10 Hz	25°C		3.3	8*		3.3	4.5*	nV/√Hz
		R_S = 20 Ω, f = 1 kHz			2.5	4.5*		2.5	3.8*	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		50	250*		50	130*	nV
I_n	Equivalent input noise current	f = 10 Hz	25°C		1.5	4*		1.5	4*	pA/√Hz
		f = 1 kHz			0.4	0.6*		0.4	0.6*	
THD	Total harmonic distortion	V_O = ±10 V, A_{VD} = 5, See Note 5	25°C		< 0.002%			<0.002%		
	Gain-bandwidth product	f = 100 kHz, R_L = 2 kΩ, C_L = 100 pF	25°C	35	50		35	50		MHz
B_{OM}	Maximum output-swing bandwidth	R_L = 2 kΩ	25°C		80			80		kHz
ϕ_m	Phase margin	R_L = 2 kΩ, C_L = 100 pF	25°C		50°			50°		

*On products compliant to MIL-PRF-38535, this parameter is not production tested.
† Full range is – 55°C to 125°C.
NOTE 5: Measured distortion of the source used in the analysis was 0.002%.

electrical characteristics, $V_{CC\pm} = \pm15$ V, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLE2037Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$,	$R_S = 50\ \Omega$		20	100	µV
	Input offset voltage long-term drift (see Note 4)				0.006	1	µV/mo
I_{IO}	Input offset current				6	90	nA
I_{IB}	Input bias current				15	90	nA
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$		–11 to 11	–13 to 13		V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 600\ \Omega$		10.5	12.9		V
		$R_L = 2\ k\Omega$		12	13.2		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 600\ \Omega$		–10.5	–13		V
		$R_L = 2\ k\Omega$		–12	–13.5		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm11$ V,	$R_L = 2\ k\Omega$	5	45		V/µV
		$V_O = \pm10$ V,	$R_L = 1\ k\Omega$	3.5	38		
		$V_O = \pm10$ V,	$R_L = 600\ \Omega$	2	19		
C_i	Input capacitance				8		pF
z_o	Open-loop output impdance	$I_O = 0$			50		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$,	$R_S = 50\ \Omega$	100	131		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm$ 4 V to $\pm$ 18 V,	$R_S = 50\ \Omega$	94	144		dB
I_{CC}	Supply current	$V_O = 0$,	No load		3.8	5.3	mA

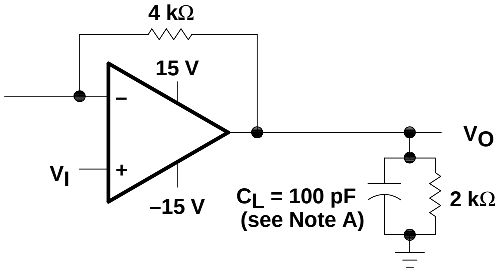
NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics, $V_{CC\pm} = \pm15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS			TLE3027Y			UNIT
					MIN	TYP	MAX	
SR	Slew rate	$A_{VD} = 5$, See Figure 1	$R_L = 2\ k\Omega$,	$C_L = 100$ pF,	6	7.5		V/µs
V_n	Equivalent input noise voltage (see Figure 2)	$R_S = 20\ \Omega$,	f = 10 Hz			3.3	8	nV/√Hz
		$R_S = 20\ \Omega$,	f = 1 kHz			2.5	4.5	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz				50	250	nV
I_n	Equivalent input noise current	f = 10 Hz				1.5	4	pA/√Hz
		f = 1 kHz				0.4	0.6	
THD	Total harmonic distortion	$V_O = \pm10$ V,	$A_{VD} = 5$,	See Note 5		< 0.002%		
	Gain-bandwidth product	f = 100 kHz,	$R_L = 2\ k\Omega$,	$C_L = 100$ pF	35	50		MHz
B_{OM}	Maximum output-swing bandwidth	$R_L = 2\ k\Omega$				80		kHz
ϕ_m	Phase margin	$R_L = 2\ k\Omega$,	$C_L = 100$ pF			50°		

NOTE 5: Measured distortion of the source used in the analysis was 0.002%.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

Figure 1. Slew-Rate Test Circuit

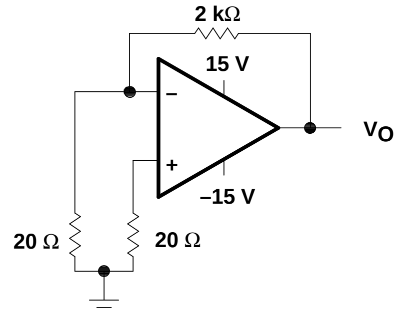


Figure 2. Noise-Voltage Test Circuit

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

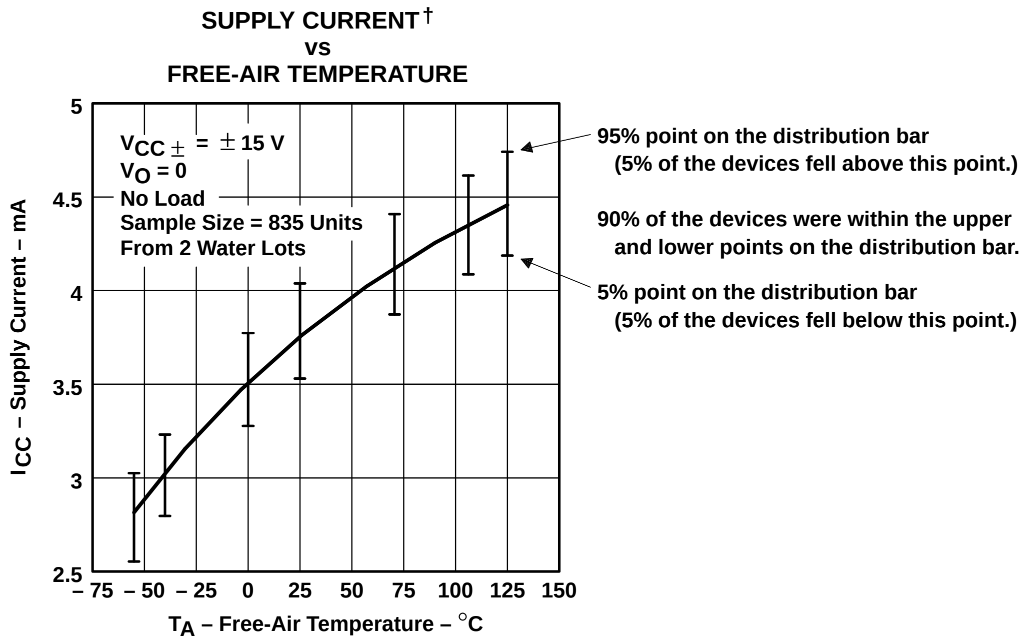
initial estimates of parameter distributions

In the on-going program of improving data sheets and supplying more information to our customer, Texas Instruments has added an estimate of not only the typical values but also the spread around these values. These are in the form of distribution bars that show the 95% (upper) points and the 5% (lower) points from our characterization of the initial wafer lots of this new device type (see Figure 3). The distribution bars are shown at the points where data was actually collected. The 95% and 5% points are used instead of ±3 sigma since some of the distributions are not true Gaussian distributions.

The number of units tested and the number of different wafer lots used are on all of the graphs where distribution bars are shown. As noted in Figure 3, there were a total of 835 units from 2 wafer lots. In this case, there is a very good estimate for the within-lot variability and a possibly poor estimate of the lot-to-lot variability. This will always be the case on newly released products, since there will only be data available from a few wafer lots.

The distribution bars are not intended to replace the minimum and maximum limits in the electrical tables. Each distribution bar represents 90% of the total units tested at a specific temperature. And, while 10% of the units tested fell outside any given distribution bar, this should not be interpreted to mean that the same individual devices fell outside every distribution bar.

PARAMETER MEASUREMENT INFORMATION



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 3. Sample Graph With Distribution Bars

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	4
ΔV_{IO}	Input offset voltage change	vs Time after power on	5,6
I_{IO}	Input offset current	vs Free-air temperature	7
I_{IB}	Input bias current	vs Common-mode input voltage vs Free-air temperature	8 9
I_I	Input current	vs Differential input voltage	10
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	11
V_{OM}	Maximum positive peak output voltage	vs Load resistance vs Free-air temperature	12 14
V_{OM}	Maximum negative peak output voltage	vs Load resistance vs Free-air temperature	13 15
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage vs Load resistance vs Frequency vs Free-air temperature	16 17 18,19 20
z_o	Output impedance	vs Frequency	21
CMRR	Common-mode rejection ratio	vs Frequency	22
k_{SVR}	Supply voltage rejection ratio	vs Frequency	23
I_{OS}	Short-circuit output current	vs Supply voltage vs Elasped time vs Free-air temperature	24, 25 26, 27 28, 29
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature	30 31
	Pulse response	Small signal Large signal	32 33
V_n	Equivalent input noise voltage	vs Frequency	34
	Noise voltage (referred to input)	0.1 to 10 Hz	35
	Gain-bandwidth product	vs Supply voltage vs Load capacitance	36 37
SR	Slew rate	vs Free-air temperature	38
ϕ_m	Phase margin	vs Supply voltage vs Load capacitance vs Free-air temperature	39 40 41
	Phase shift	vs Frequency	18, 19

TYPICAL CHARACTERISTICS

TLE2037
DISTRIBUTION OF
INPUT OFFSET VOLTAGE

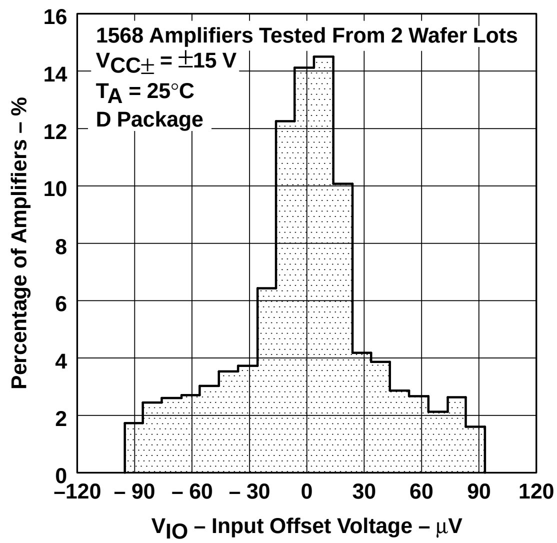


Figure 4

INPUT OFFSET VOLTAGE CHANGE
vs
TIME AFTER POWER ON

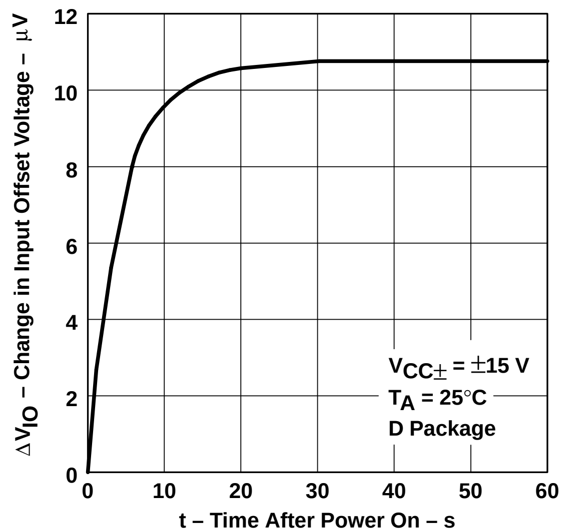


Figure 5

INPUT OFFSET VOLTAGE CHANGE
vs
TIME AFTER POWER ON

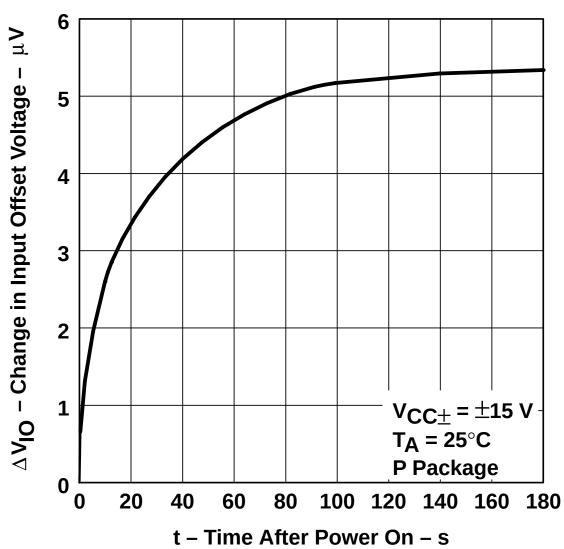
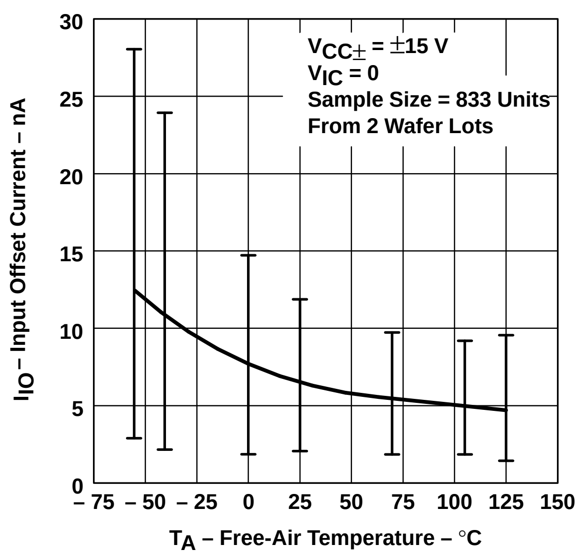


Figure 6

INPUT OFFSET CURRENT†
vs
FREE-AIR TEMPERATURE



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 7

TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

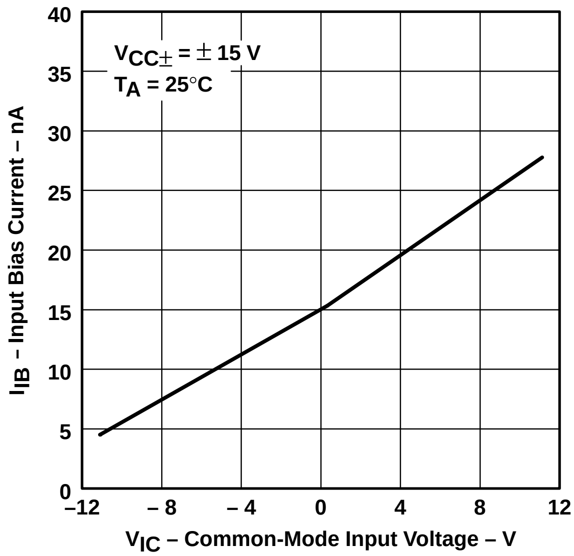
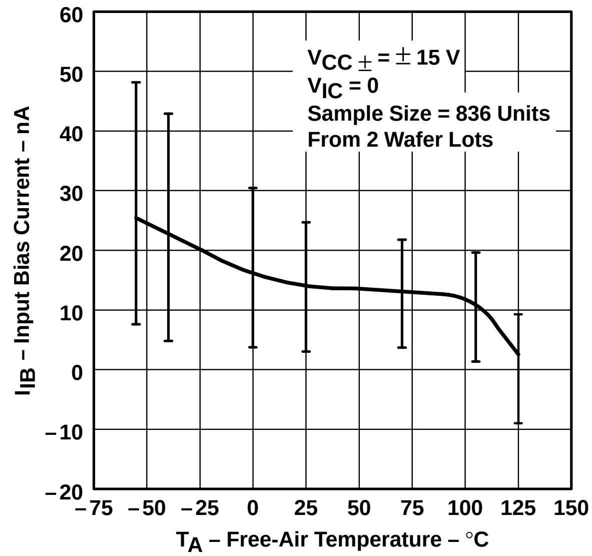


Figure 8

INPUT BIAS CURRENT†
vs
FREE-AIR TEMPERATURE



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 9

TYPICAL CHARACTERISTICS

INPUT CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE

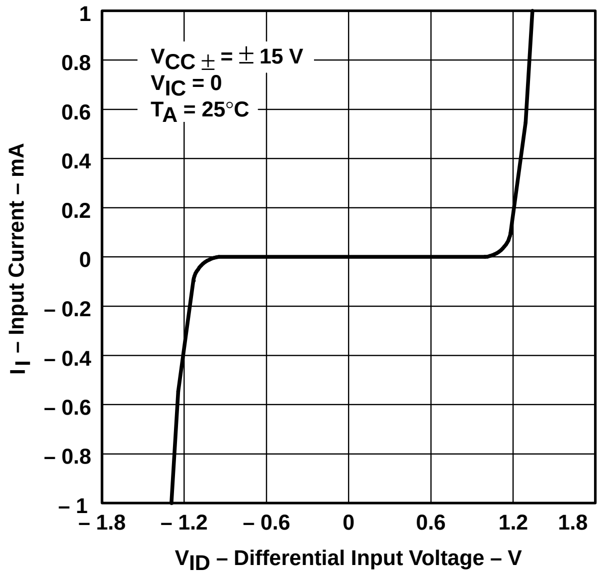
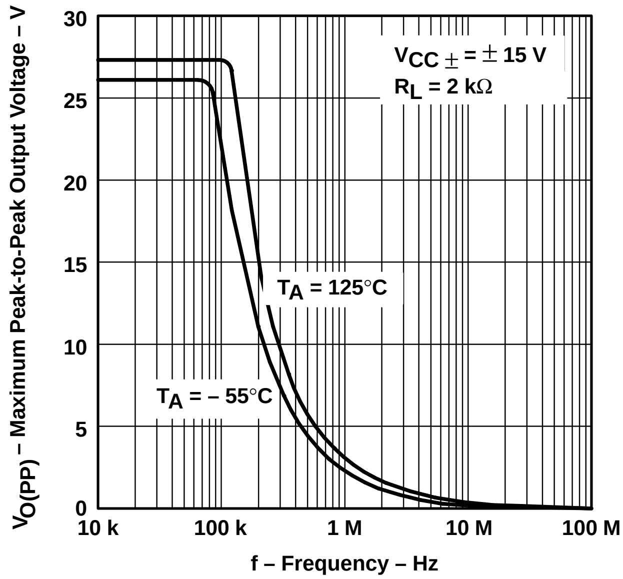


Figure 10

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE†
vs
FREQUENCY



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 11

MAXIMUM POSITIVE PEAK
OUTPUT VOLTAGE
vs
LOAD RESISTANCE

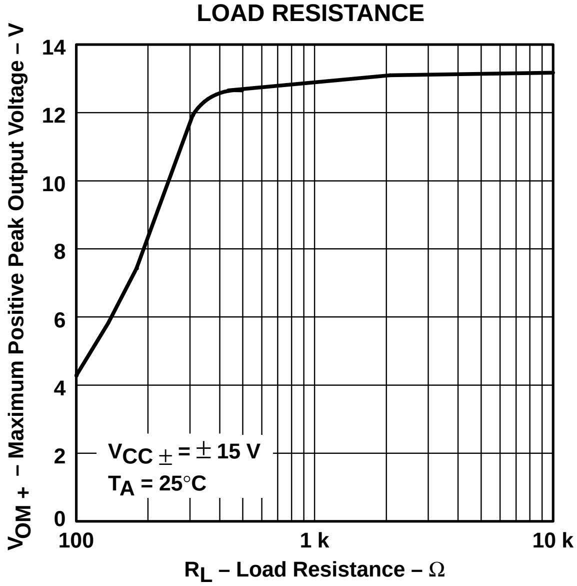


Figure 12

MAXIMUM NEGATIVE PEAK
OUTPUT VOLTAGE
vs
LOAD RESISTANCE

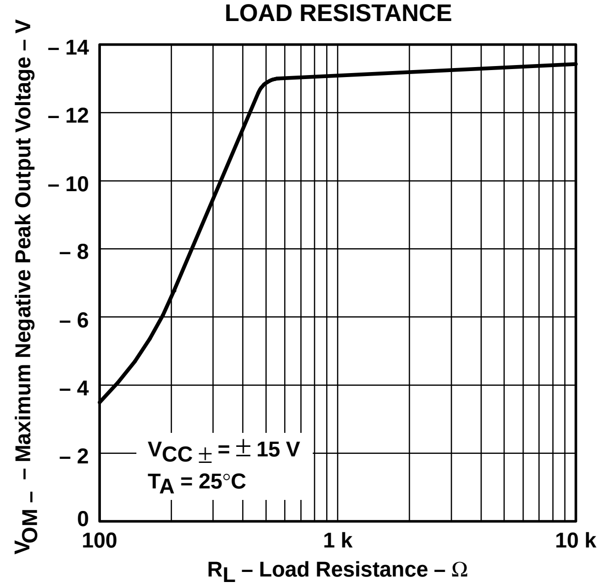
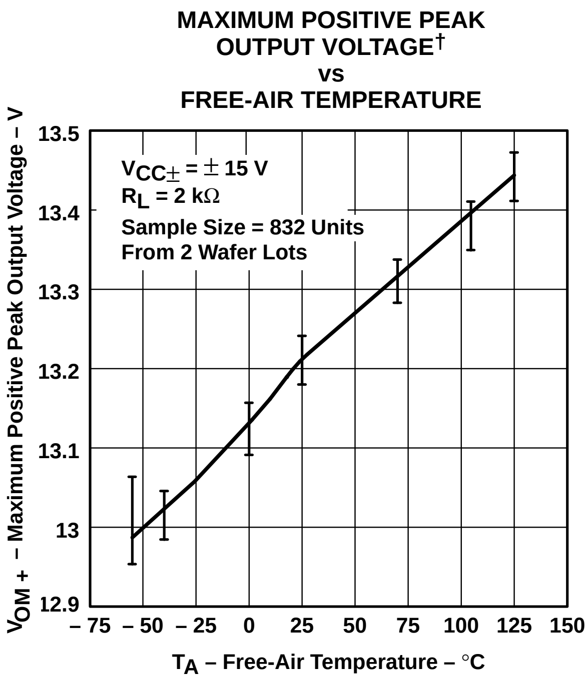


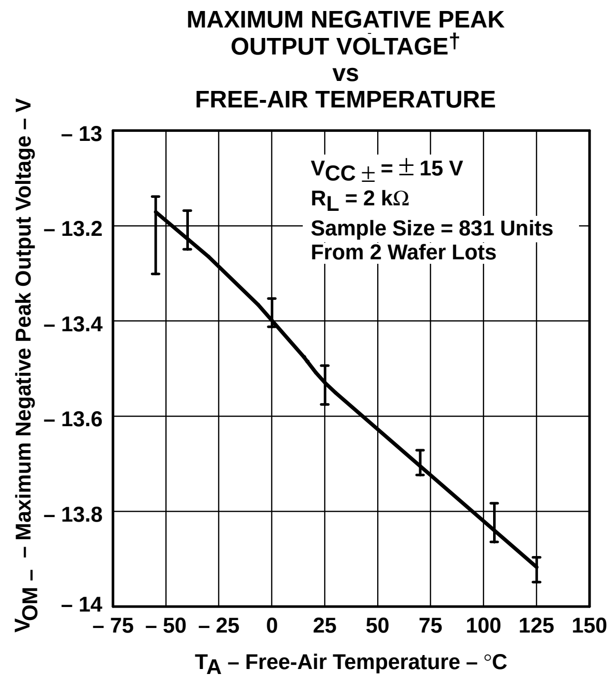
Figure 13

TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 14



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 15

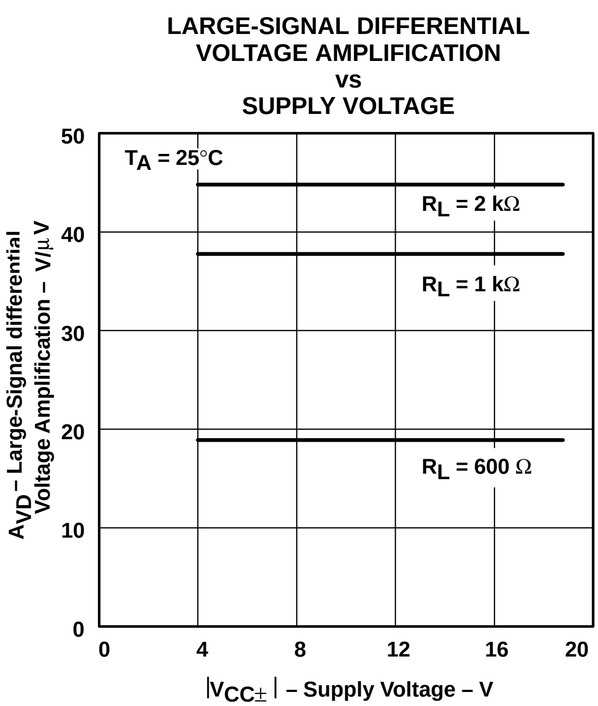


Figure 16

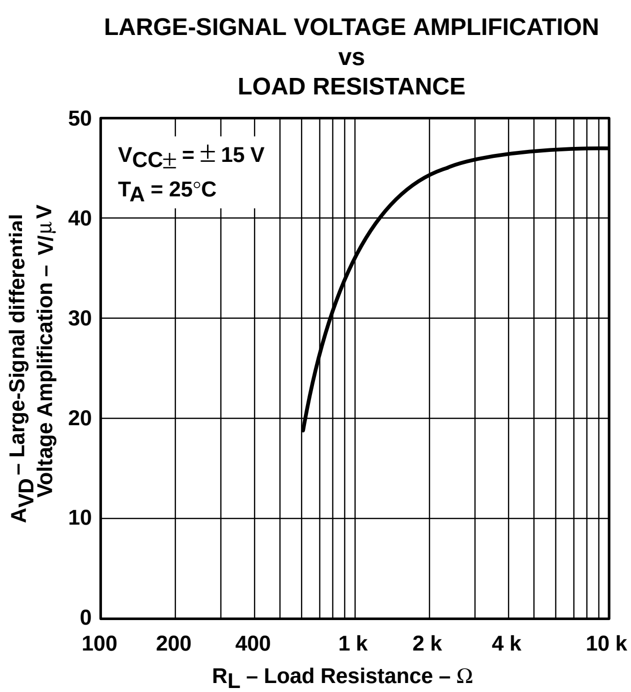


Figure 17

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

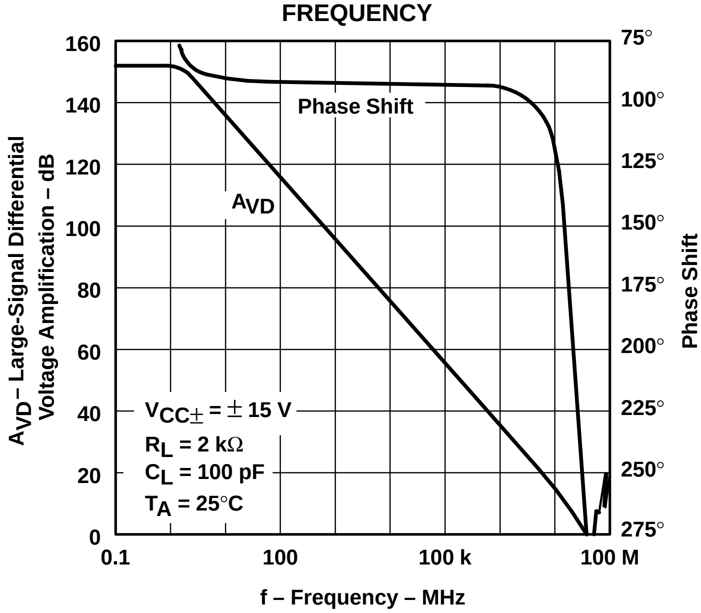


Figure 18

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

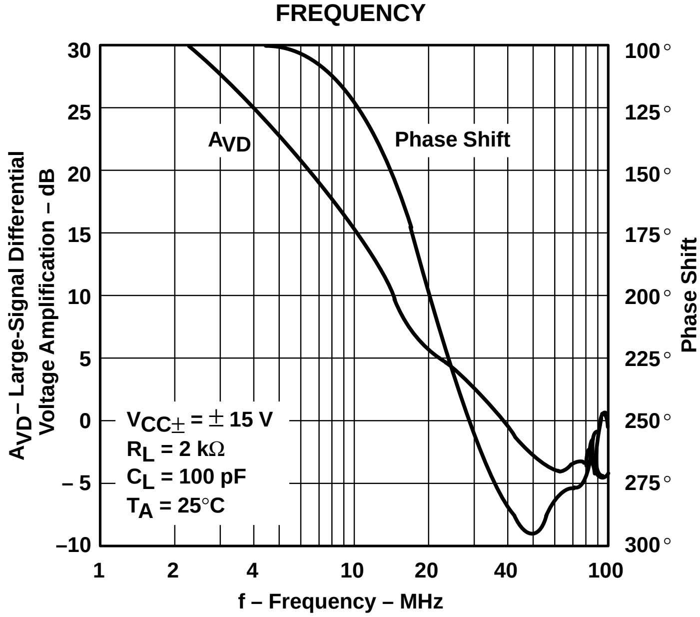
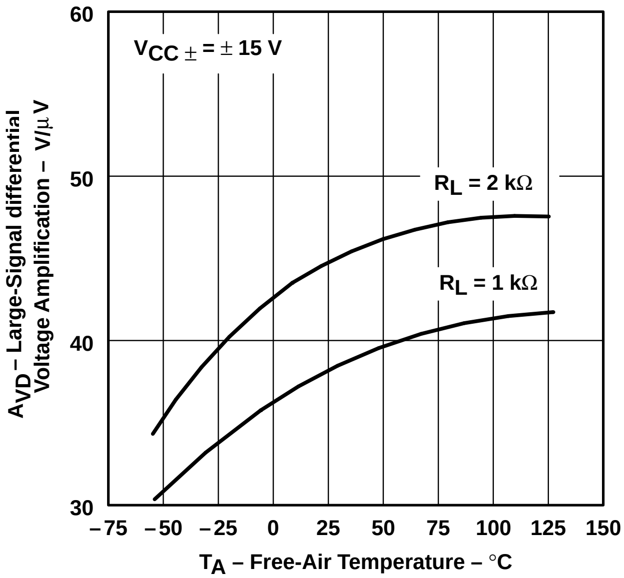


Figure 19

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION† vs FREE-AIR TEMPERATURE



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 20

OUTPUT IMPEDANCE vs FREQUENCY

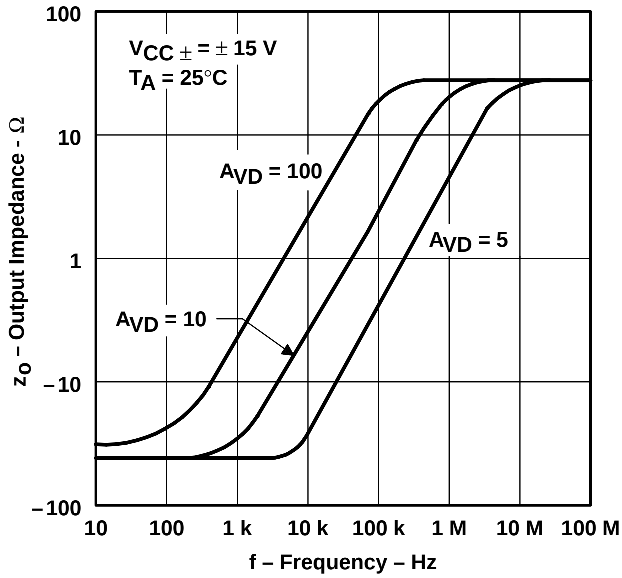


Figure 21

TYPICAL CHARACTERISTICS

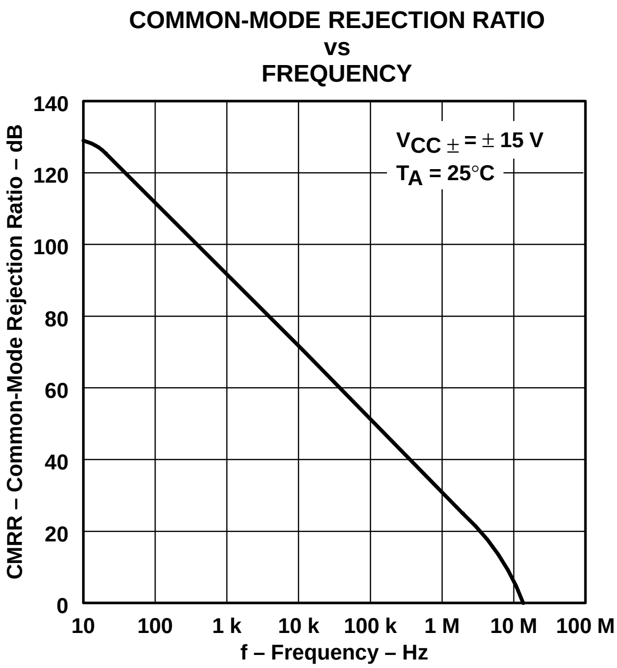


Figure 22

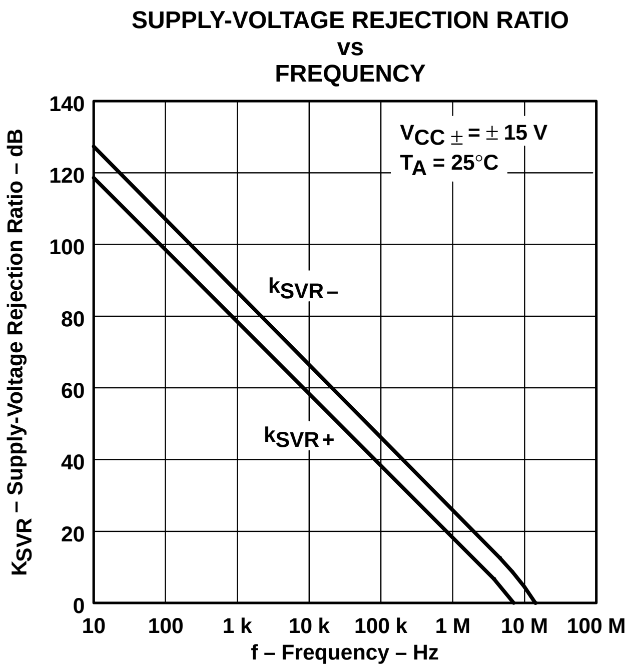


Figure 23

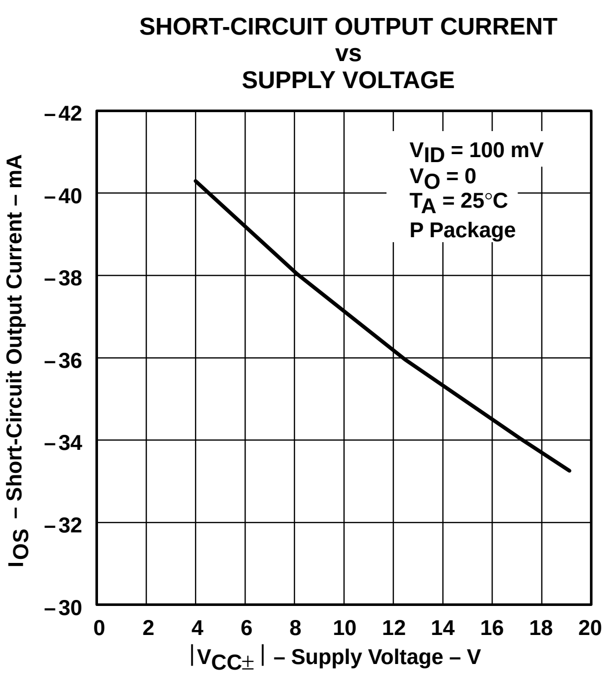


Figure 24

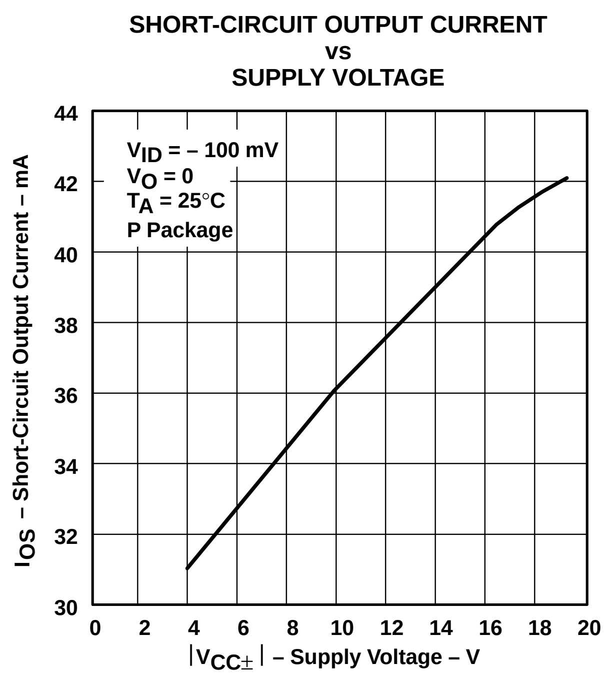


Figure 25

TYPICAL CHARACTERISTICS

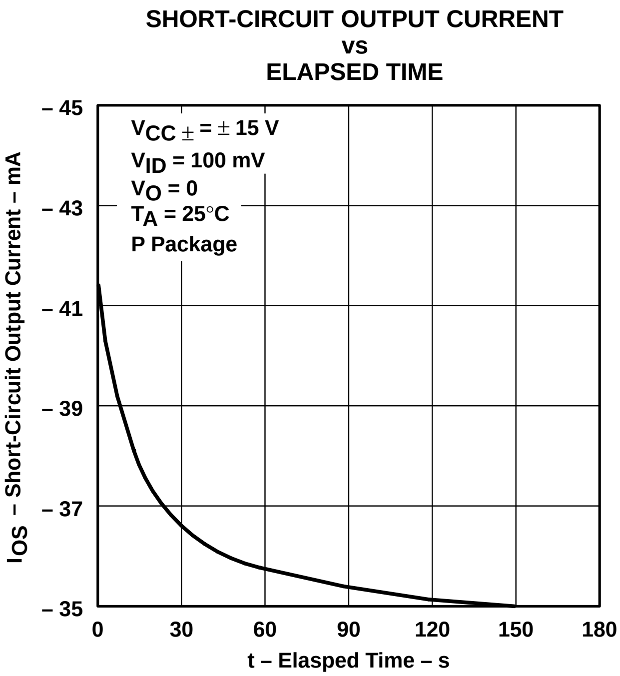


Figure 26

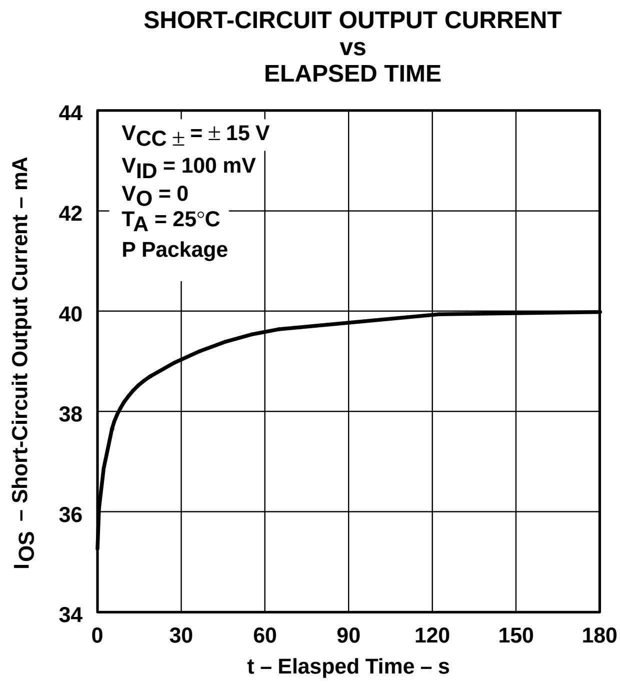
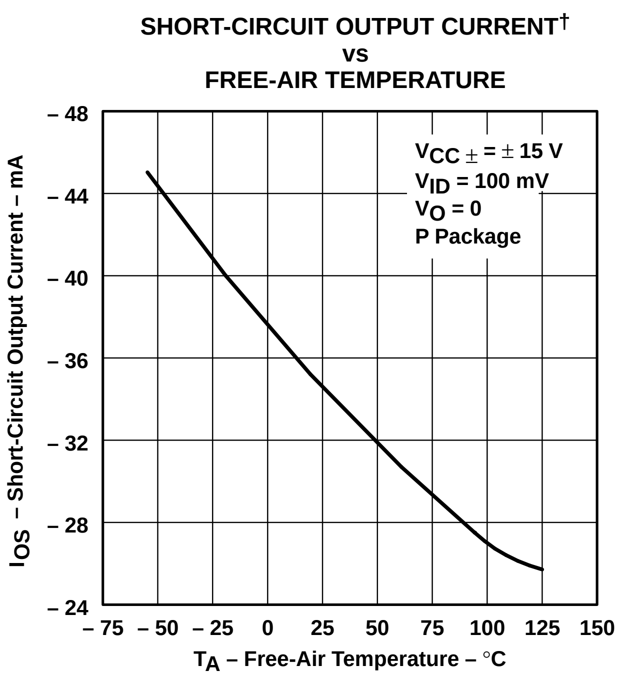
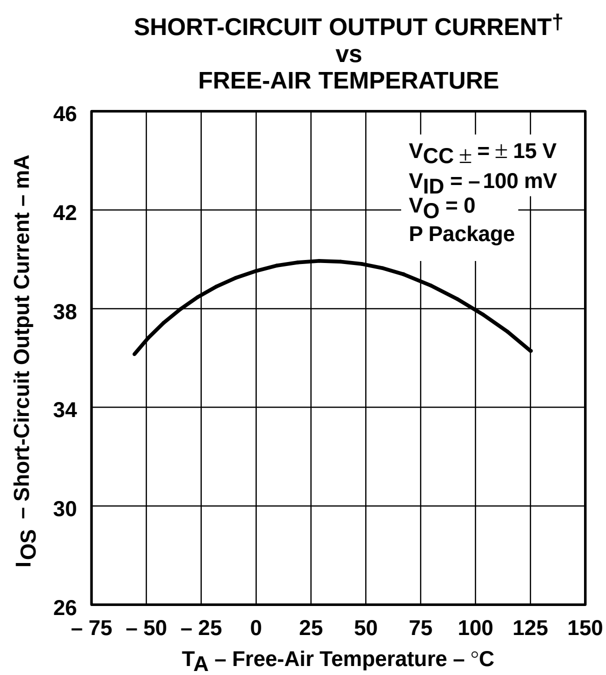


Figure 27



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

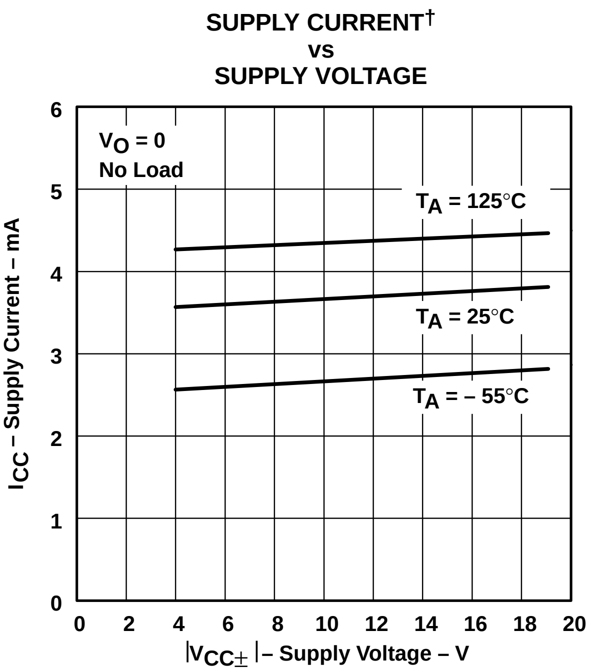
Figure 28



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

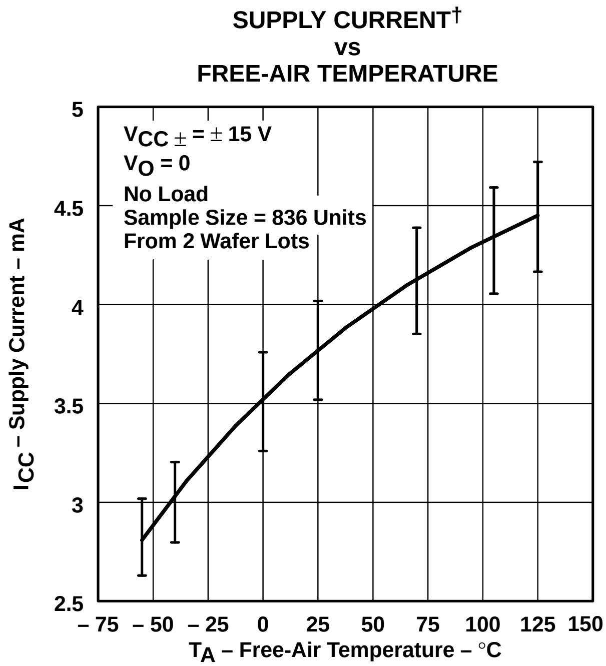
Figure 29

TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 30



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 31

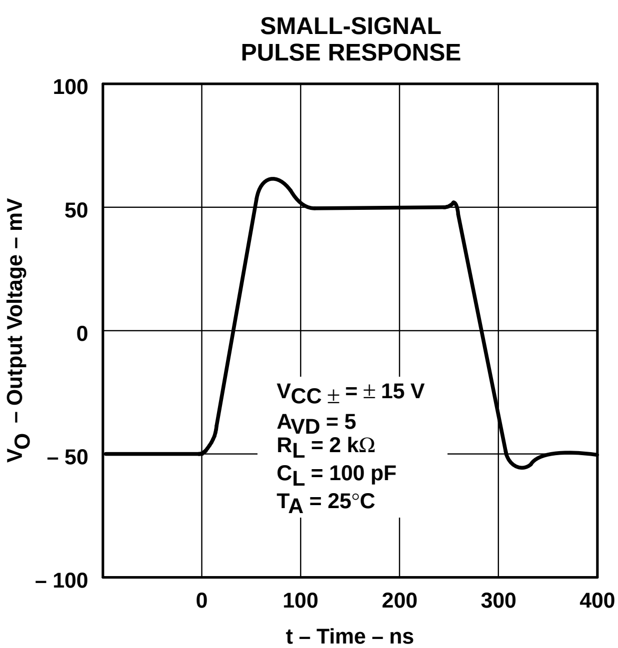


Figure 32

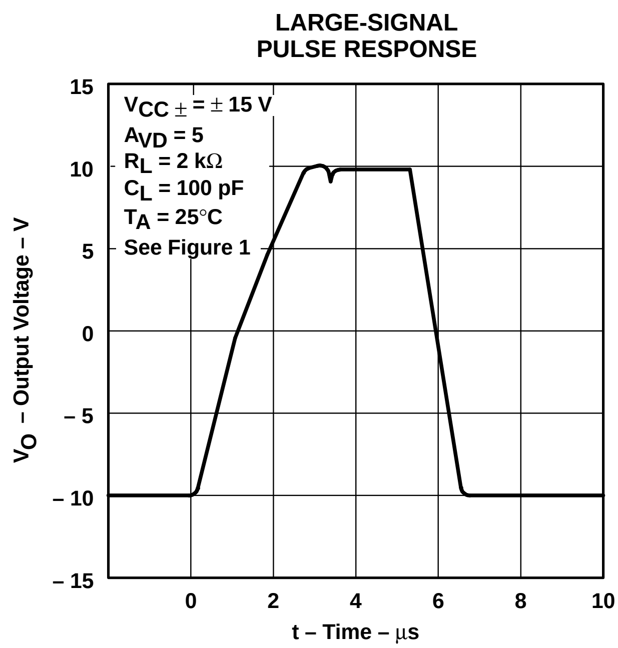


Figure 33

TYPICAL CHARACTERISTICS

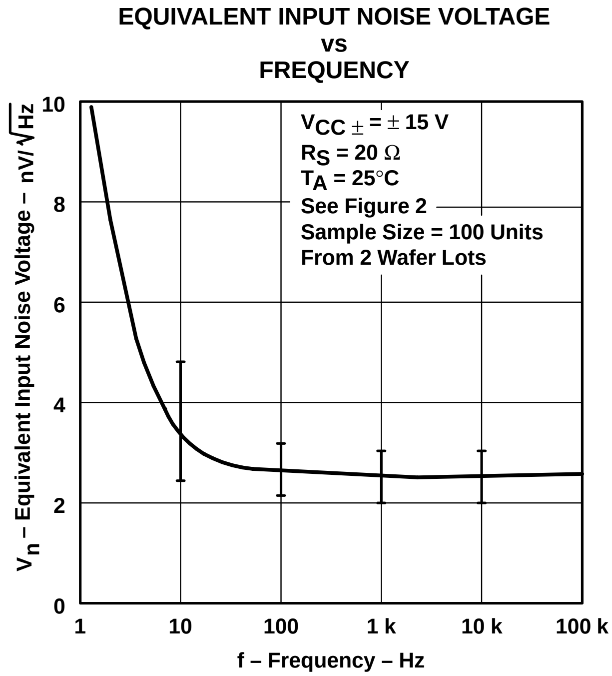


Figure 34

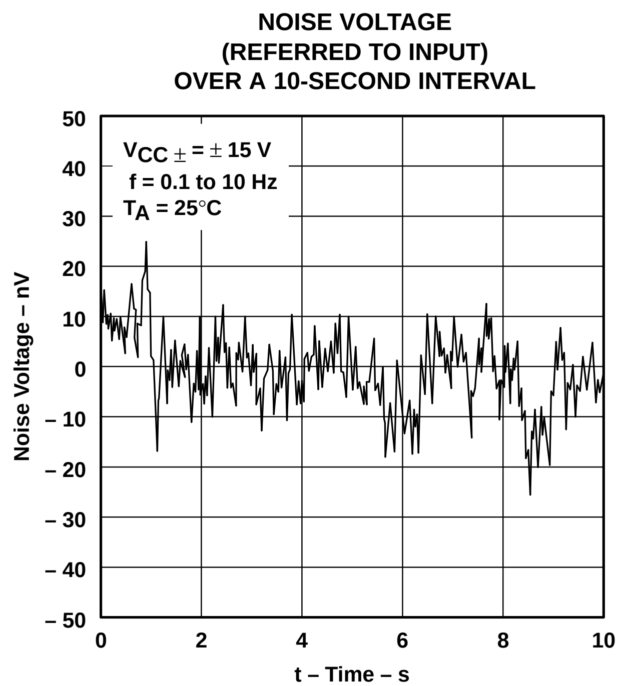


Figure 35

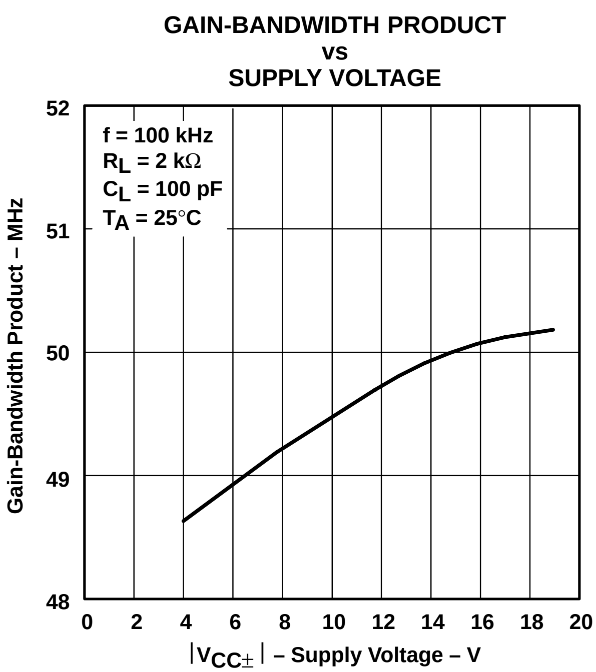


Figure 36

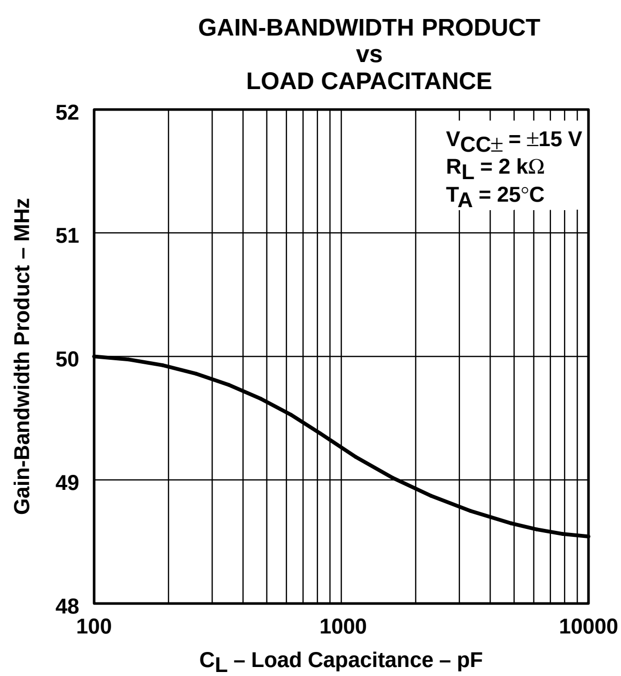
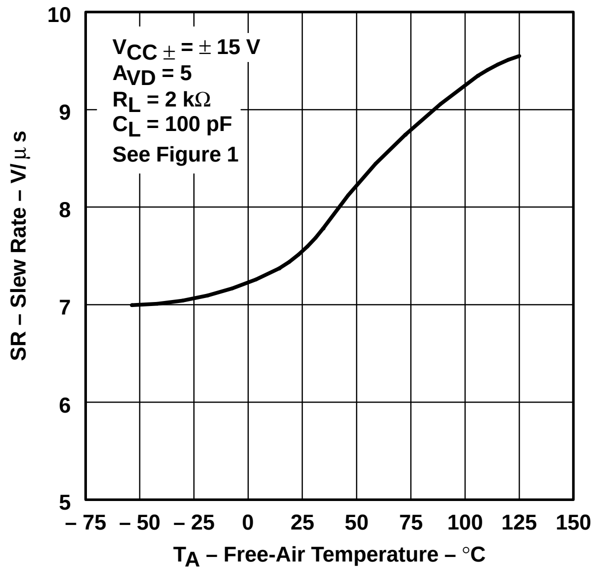


Figure 37

TYPICAL CHARACTERISTICS

SLEW RATE†
vs
FREE-AIR TEMPERATURE



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 38

PHASE MARGIN
vs
SUPPLY VOLTAGE

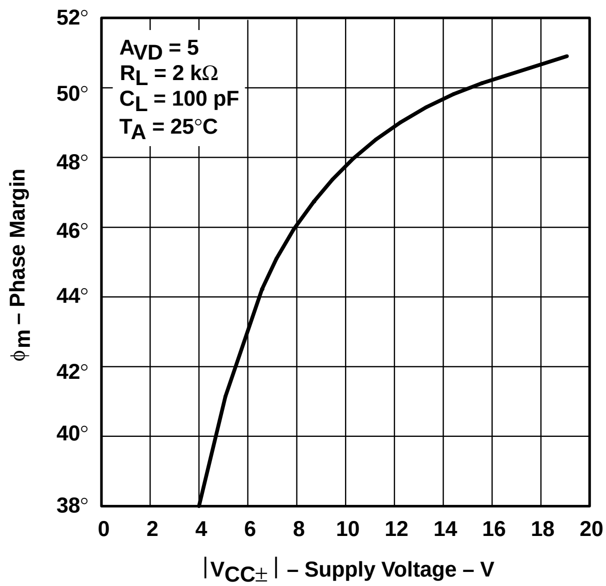


Figure 39

TYPICAL CHARACTERISTICS

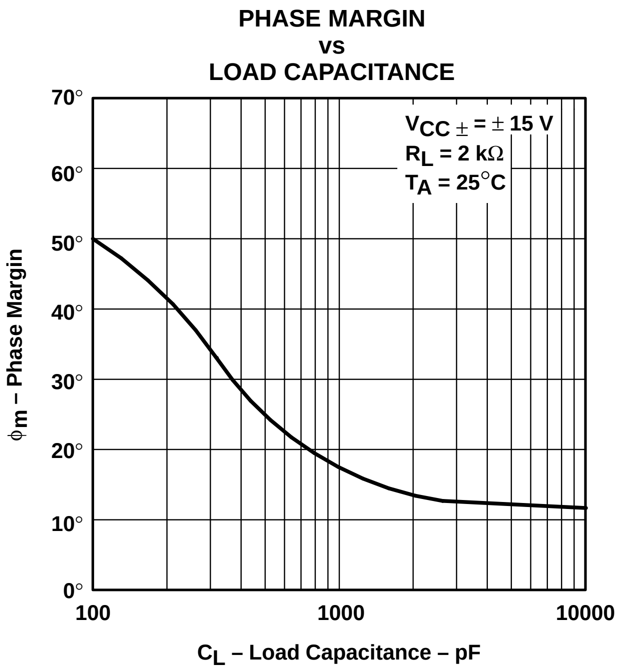
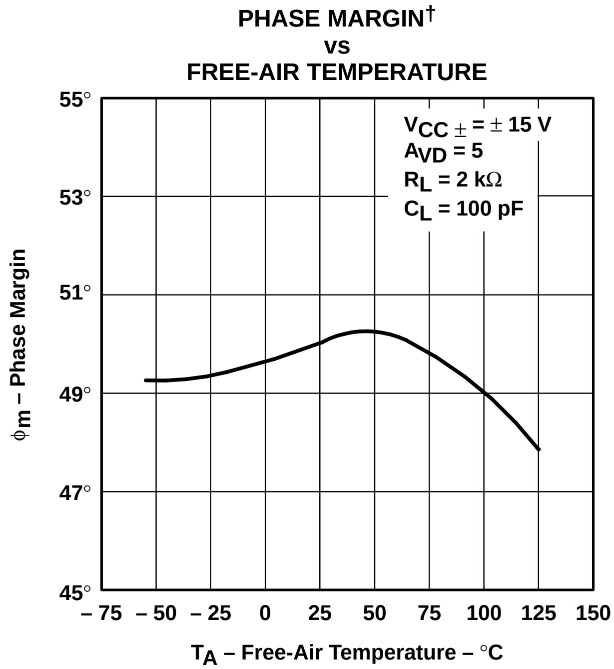


Figure 40



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 41

APPLICATION INFORMATION

input offset voltage nulling

The TLE2037 series offers external null pins that can be used to further reduce the input offset voltage. The circuits of Figure 42 can be connected as shown if the feature is desired. If external nulling is not needed, the null pins may be left disconnected.

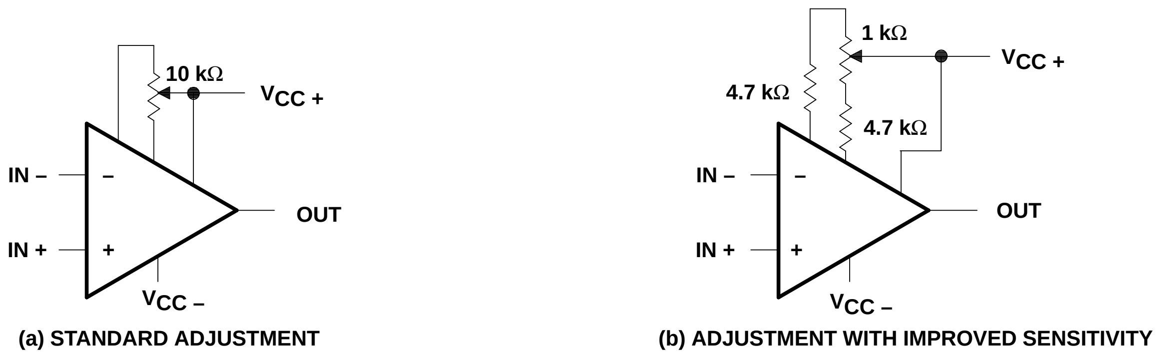


Figure 42. Input Offset Voltage Nulling Circuits

macromodel information

Macromodel information provided was derived using *PSpice*™ *Parts*™ model generation software. The Boyle macromodel (see Note 6) and subcircuit in Figures 42 and 43 were generated using the TLE2037 typical electrical and operating characteristics at 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Gain-bandwidth product
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 6: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, “Macromodeling of Integrated Circuit Operational Amplifiers”, IEEE Journal of Solid-State Circuits, SC-9, 353 (1974).

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APPLICATION INFORMATION

macromodel information (continued)

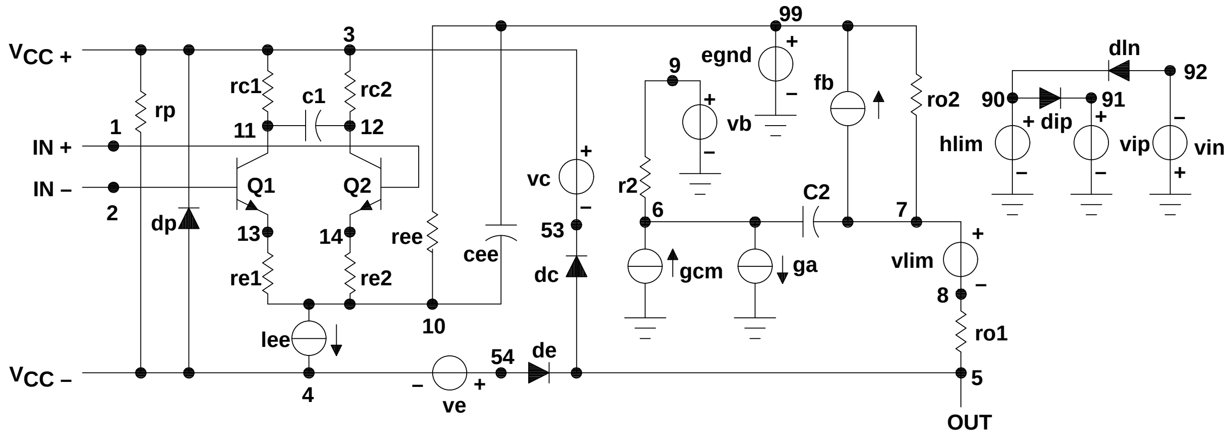


Figure 43. Boyle Macromodel

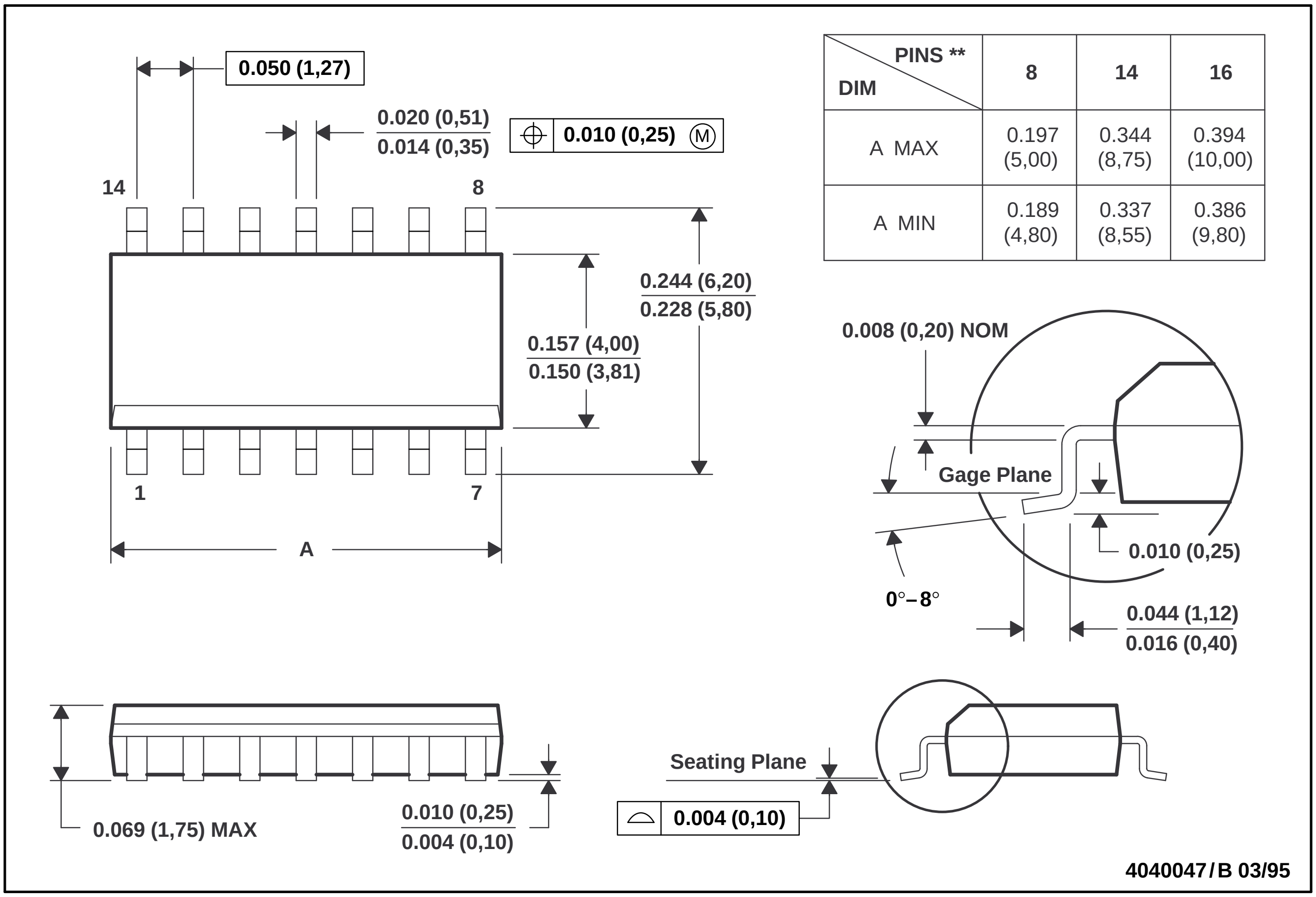
```
.subckt TLE2037 1 2 3 4 5
*
  c1          11   12 4.003E–12
  c2           6    7 7.500E–12
  dc           5   53 dz
  de          54    5 dz
  dlp         90   91 dz
  dln         92   90 dx
  dp           4    3 dz
  egnd        99    0 poly(2)  (3,0)   (4,0)   0  .5   .5
  fb           7   99 poly(5) vb vc ve vip vln 0 923.4E6 A800E6 800E6 800E6 A800E6
  ga           6    0 11 12 2.121E–3
  gcm          0    6 10 99 597.7E–12
  iee         10    4 dc 56.26E–6
  hlim        90    0 vlim 1K
  q1          11    2 13 qx
  q2          12    1 14 qz
  r2           6    9 100.0E3
  rc1          3   11 471.5
  rc2          3   12 471.5
  re1         13   10 A448
  re2         14   10 A448
  ree         10   99 3.555E6
  ro1          8    5 25
  ro2          7   99 25
  rp           3    4 8.013E3
  vb           9    0 dc 0
  vc           3   53 dc  2.400
  ve          54    4 dc  2.100
  vlim         7    8 dc  0
  vlp         91    0 dc  40
  vln          0   92 dc  40
.model        dx D(Is=800.0E–18)
.model        qx NPN(Is=800.0E–18 Bf=7.031E3)
.ends
```

Figure 44. Macromodel Subcircuit

MECHANICAL INFORMATION

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



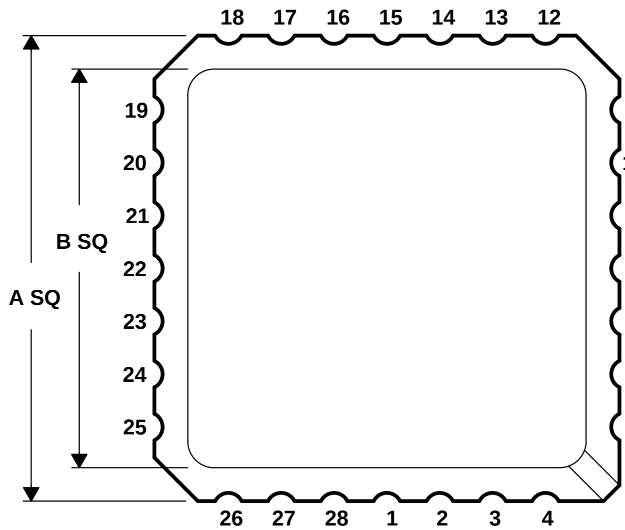
DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Four center pins are connected to die mount pad.
E. Falls within JEDEC MS-012

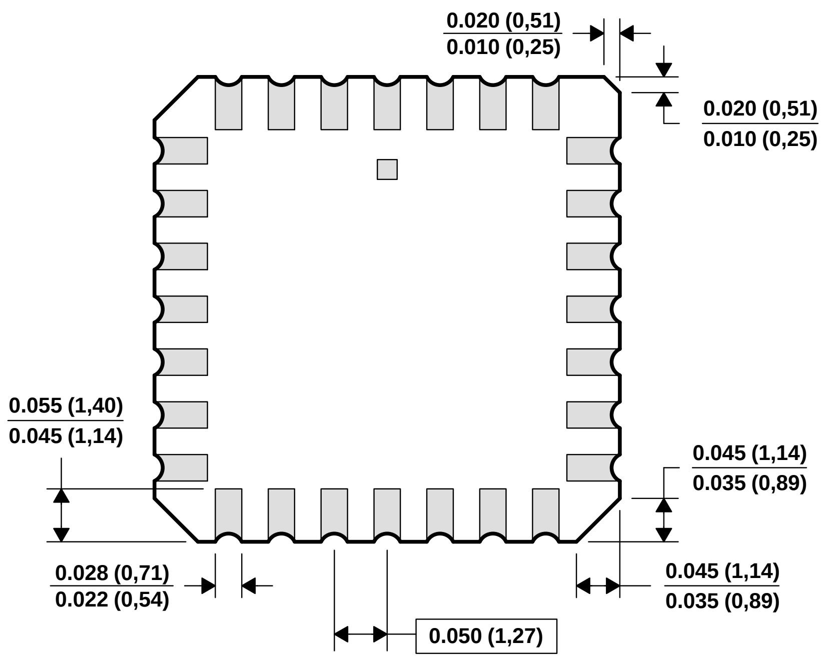
MECHANICAL INFORMATION

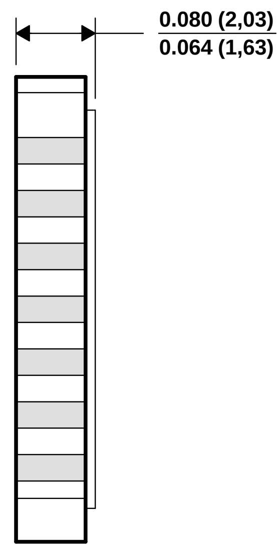
FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



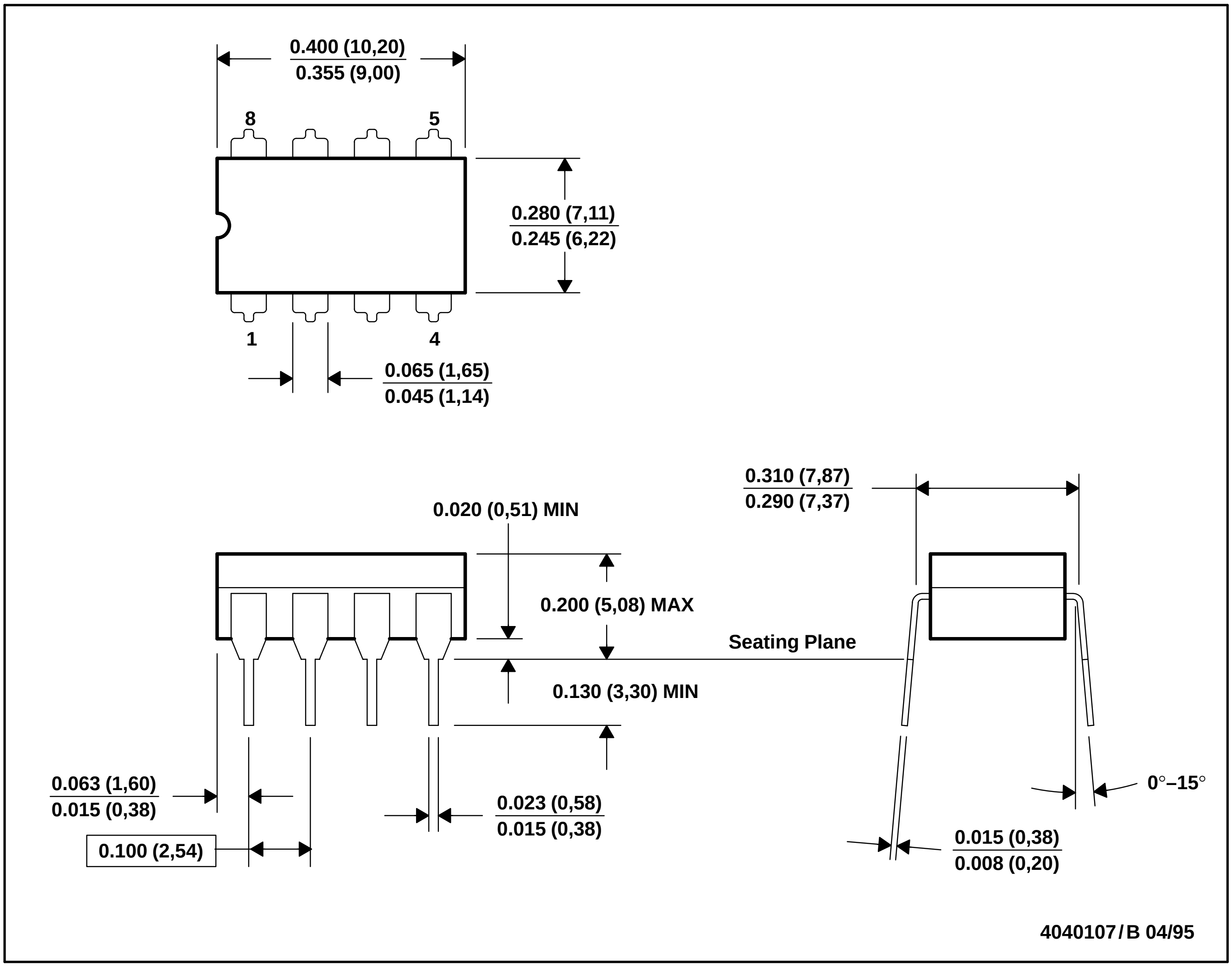


4040140/C 11/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

MECHANICAL INFORMATION

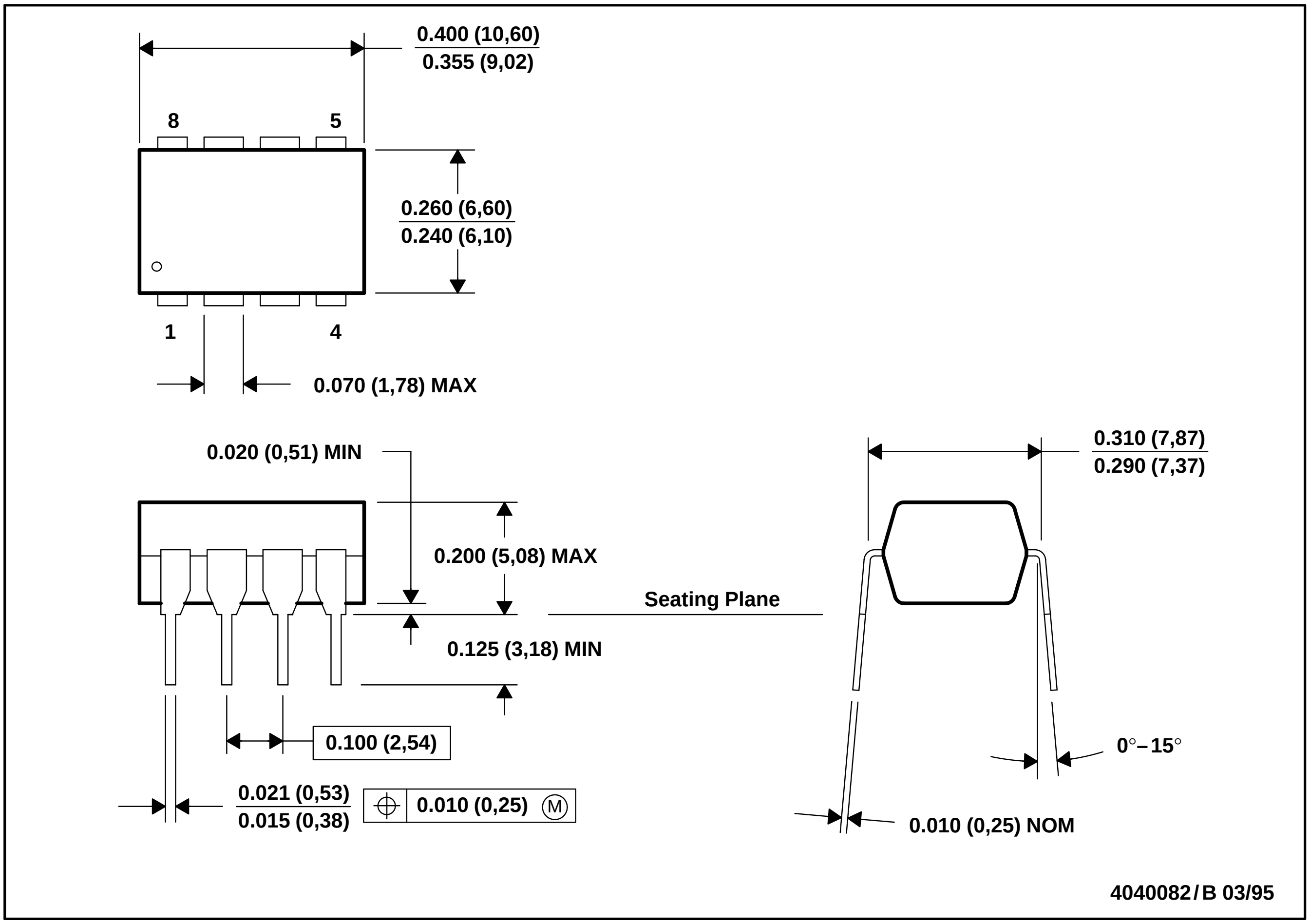
JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only
E. Falls within MIL-STD-1835 GDIP1-T8

MECHANICAL INFORMATION

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

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