Excalibur™ LOW-NOISE HIGH-SPEED PRECISION OPERATIONAL AMPLIFIERS

Check for Samples: TLE2141-Q1

FEATURES

- **Qualified for Automotive Applications**
- **Low Noise**
  - **10 Hz … 15 nV/√Hz**
  - **1 kHz … 10.5 nV/√Hz**
- **10000-pF Load Capability**
- **20-mA Min Short-Circuit Output Current**
- **27-V/μs Slew Rate (Min)**
- **High Gain-Bandwidth Product … 5.9 MHz**
- **Low V_{IO} … 500 μV (Max) at 25°C**
- **Single or Split Supply … 4 V to 44 V**
- **Fast Settling Time**
  - **340 ns to 0.1%**
  - **400 ns to 0.01%**
- **Saturation Recovery … 150 ns**
- **Large Output Swing … V_{CC-} + 0.1 V to V_{CC+} – 1 V**

DESCRIPTION

The TLE2141-Q1 device is a high-performance, internally compensated operational amplifier built using the Texas Instruments complementary bipolar Excalibur™ process. It is a pin-compatible upgrade to standard industry products.

The design incorporates an input stage that simultaneously achieves low audio-band noise of 10.5 nV/√Hz with a 10-Hz 1/f corner and symmetrical 40-V/μs slew rate typically with loads up to 800 pF. The resulting low distortion and high power bandwidth are important in high-fidelity audio applications. A fast settling time of 340 ns to 0.1% of a 10-V step with a 2-kΩ/100-pF load is useful in fast actuator/positioning drivers. Under similar test conditions, settling time to 0.01% is 400 ns.

The device is stable with capacitive loads up to 10 nF, although the 6-MHz bandwidth decreases to 1.8 MHz at this high loading level. As such, the TLE2141-Q1 is useful for low-droop sample-and-holds and direct buffering of long cables, including 4-mA to 20-mA current loops.

The special design also exhibits an improved insensitivity to inherent integrated circuit component mismatches as is evidenced by a 500-μV maximum offset voltage and 1.7-μV/°C typical drift. Minimum common-mode rejection ratio and supply-voltage rejection ratio are 85 dB and 90 dB, respectively.

Device performance is relatively independent of supply voltage over the ±2-V to ±22-V range. Inputs can operate between V_{CC-} – 0.3 V to V_{CC+} – 1.8 V without inducing phase reversal, although excessive input current may flow out of each input exceeding the lower common-mode input range. The all-npn output stage provides a nearly rail-to-rail output swing of V_{CC-} – 0.1 V to V_{CC+} – 1 V under light current-loading conditions. The device can sustain shorts to either supply since output current is internally limited, but care must be taken to ensure that maximum package power dissipation is not exceeded.

The TLE2141-Q1 device can also be used as a comparator. Differential inputs of $V_{CC\pm}$ can be maintained without damage to the device. Open-loop propagation delay with TTL supply levels is typically 200 ns. This gives a good indication as to output stage saturation recovery when the device is driven beyond the limits of recommended output swing.

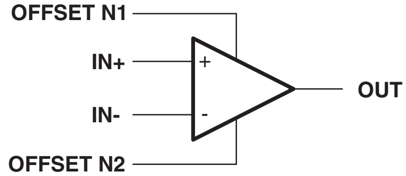
The TLE2141-Q1 device is available in industry-standard 8-pin package. The device is characterized for operation from –40°C to 125°C.

ORDERING INFORMATION(1)

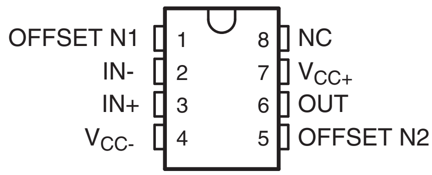
T_A	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – D (8 pin)	Reel of 2500	TLE2141QDRQ1	2141Q

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

SYMBOL

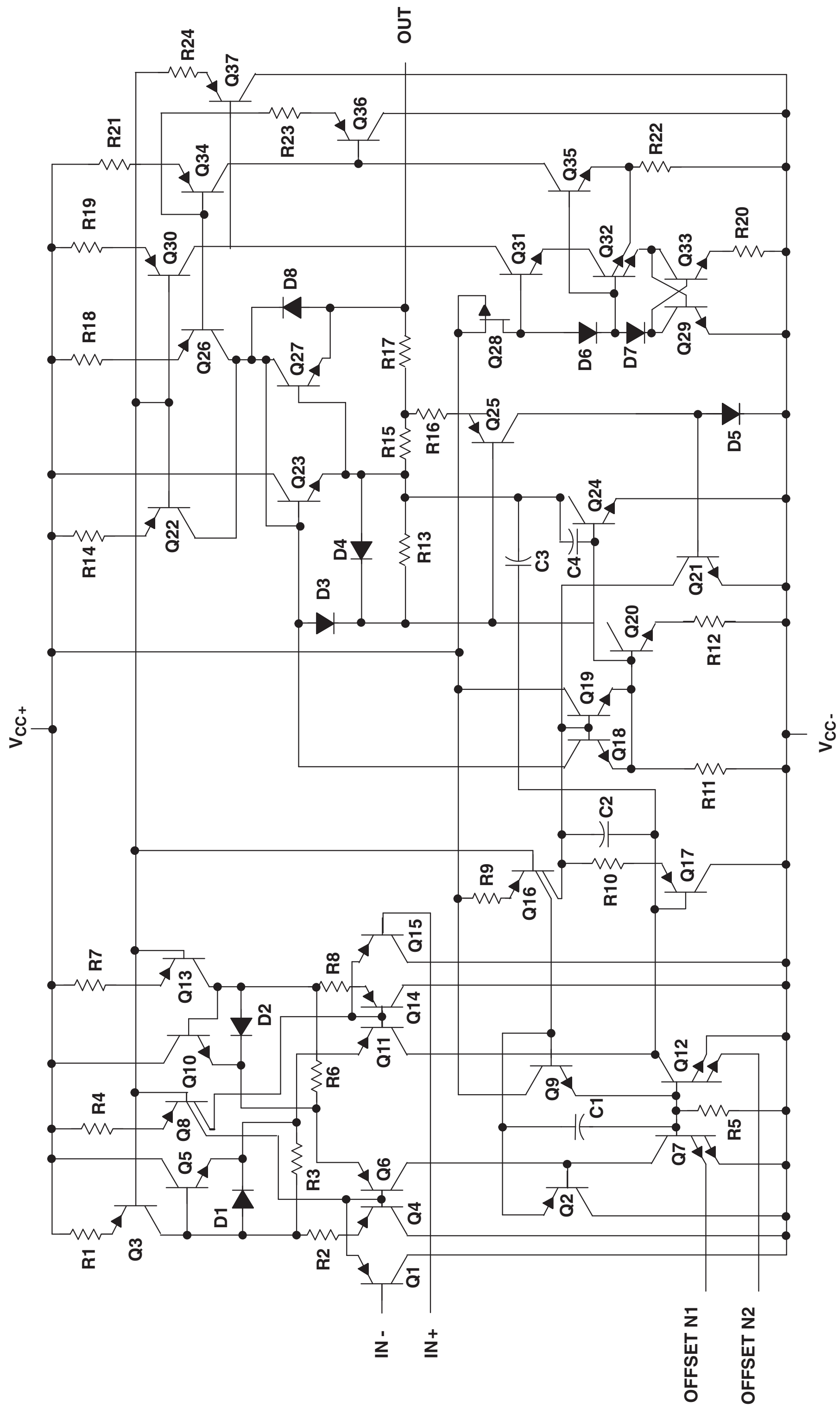


D PACKAGE
(TOP VIEW)



NC – No internal connection

Figure 1. EQUIVALENT SCHEMATIC



DEVICE COMPONENT COUNT

COMPONENT	TLE2141-Q1
Transistors	46
Resistors	24
Diodes	8
Capacitors	4
Epi-FET	1

ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
V_{CC+}	Supply voltage[2]		22	V
V_{CC-}	Supply voltage		–22	V
V_{ID}	Differential input voltage[3]		±44	V
V_I	Input voltage range (any input)		V_{CC+} to (V_{CC-} – 0.3)	V
I_I	Input current (each input)		±1	mA
I_O	Output current		±80	mA
	Total current into V_{CC+}		80	mA
	Total current out of V_{CC-}		80	mA
	Duration of short-circuit current at (or below) 25°C[4]		Unlimited	
θ_{JA}	Package thermal impedance[5] [6]	D package (8 pin)	97.1	°C/W
T_A	Operating free-air temperature range		–40 to 125	°C
T_{stg}	Storage temperature range		–65 to 150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
(3) Differential voltages are at IN+ with respect to IN–. Excessive current flows, if input, are brought below V_{CC-} – 0.3 V.
(4) The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
(5) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
$V_{CC\pm}$	Supply voltage		±2	±22	V
V_{IC}	Common-mode input voltage	V_{CC} = 5 V	0	2.7	V
		$V_{CC\pm}$ = ±15 V	–15	12.7	
T_A	Operating free-air temperature		–40	125	°C

ELECTRICAL CHARACTERISTICS

V_{CC} = 5 V, at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A (1)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 2.5 V, R_S = 50 Ω, V_{IC} = 2.5 V	25°C		225	1400	µV
			Full range			2100	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 2.5 V, R_S = 50 Ω, V_{IC} = 2.5 V	Full range		1.7		µV/°C
I_{IO}	Input offset current	V_O = 2.5 V, R_S = 50 Ω, V_{IC} = 2.5 V	25°C		8	100	nA
			Full range			250	
I_{IB}	Input bias current	V_O = 2.5 V, R_S = 50 Ω, V_{IC} = 2.5 V	25°C		–0.8	–2	µA
			Full range			–2.3	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3	–0.3 to 3.2		V
			Full range	0 to 2.7	–0.3 to 2.9		
V_{OH}	High-level output voltage	I_{OH} = –150 µA	25°C	3.9	4.1		V
		I_{OH} = –1.5 mA		3.8	4		
		I_{OH} = –15 mA		3.2	3.7		
		I_{OH} = –100 µA	Full range	3.75			
		I_{OH} = –1 mA		3.65			
		I_{OH} = –10 mA		3.25			
V_{OL}	Low-level output voltage	I_{OL} = 150 µA	25°C		75	125	mV
		I_{OL} = 1.5 mA			150	225	
		I_{OL} = 15 mA			1.2	1.4	V
		I_{OL} = 100 µA	Full range			200	mV
		I_{OL} = 1 mA				250	
		I_{OL} = 10 mA				1.25	V
A_{VD}	Large-signal differential voltage amplification	V_{IC} = ±2.5 V, R_L = 2 kΩ, V_O = 1 V to 1.5 V	25°C	50	220		V/mV
			Full range	5			
r_i	Input resistance		25°C		70		MΩ
c_i	Input capacitance		25°C		2.5		pF
z_o	Open-loop output impedance	f = 1 MHz	25°C		30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}(min), R_S = 50 Ω	25°C	85	118		dB
			Full range	80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω	25°C	90	106		dB
			Full range	85			
I_{CC}	Supply current	V_O = 2.5 V, No load, V_{IC} = 2.5 V	25°C		3.4	4.4	mA
			Full range			4.6	

(1) Full range is –40°C to 125°C.

OPERATING CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR+	Positive slew rate	A_{VD} = –1, R_L = 2 kΩ[(1)], C_L = 500 pF			45		V/µs
SR–	Negative slew rate	A_{VD} = –1, R_L = 2 kΩ[(1)], C_L = 500 pF			42		V/µs
t_s	Settling time	A_{VD} = –1, 2.5-V step	To 0.1%		0.16		µs
			To 0.01%		0.22		
V_n	Equivalent input noise voltage	R_S = 20 Ω	f = 10 Hz		15		nV/√Hz
			f = 1 kHz		10.5		
$V_{n(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48		µV
		f = 0.1 Hz to 10 Hz			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.92		pA/√Hz
		f = 1 kHz			0.5		
THD+N	Total harmonic distortion plus noise	V_O = 1 V to 3 V, R_L = 2 kΩ[(1)], A_{VD} = 2, f = 10 kHz			0.0052		%
B_1	Unity-gain bandwidth	R_L = 2 kΩ[(1)], C_L = 100 pF[(1)]			5.9		MHz
	Gain-bandwidth product	R_L = 2 kΩ[(1)], C_L = 100 pF[(1)], f = 100 kHz			5.8		MHz
BOM	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 2 kΩ[(1)], A_{VD} = 1			660		kHz
φ_m	Phase margin at unity gain	R_L = 2 kΩ[(1)], C_L = 100 pF[(1)]			57		°

(1) R_L and C_L terminated to 2.5 V.

ELECTRICAL CHARACTERISTICS

V_{CC} = ±15 V, at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω		25°C		200	900	μV
				Full range			1700	
α_{VIO}	Temperature coefficient of input offset voltage	V_{IC} = 0, R_S = 50 Ω		Full range		1.7		μV/°C
I_{IO}	Input offset current	V_{IC} = 0, R_S = 50 Ω		25°C		7	100	nA
				Full range			250	
I_{IB}	Input bias current	V_{IC} = 0, R_S = 50 Ω		25°C		–0.7	–1.5	μA
				Full range			–1.8	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	–15 to 13	–15.3 to 13.2		V
				Full range	–15 to 12.7	–15.3 to 12.9		
V_{OM+}	Maximum positive peak output voltage swing	I_O = –150 μA		25°C	13.8	14.1		V
		I_O = –1.5 mA			13.7	14		
		I_O = –15 mA			13.1	13.7		
		I_O = –100 μA		Full range	13.7			
		I_O = –1 mA			13.6			
		I_O = –10 mA			13.1			
$V_{OM–}$	Maximum negative peak output voltage swing	I_O = 150 μA		25°C	–14.7	–14.9		V
		I_O = 1.5 mA			–14.5	–14.8		
		I_O = 15 mA			–13.4	–13.8		
		I_O = 100 μA		Full range	–14.6			
		I_O = 1 mA			–14.5			
		I_O = 10 mA			–13.4			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = 2 kΩ		25°C	100	450		V/mV
				Full range	20			
r_i	Input resistance			25°C		65		MΩ
c_i	Input capacitance			25°C		2.5		pF
z_o	Open-loop output impedance	f = 1 MHz		25°C		30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}(min), R_S = 50 Ω		25°C	85	108		dB
				Full range	80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω		25°C	90	106		dB
				Full range	85			
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	–25	–50		mA
			V_{ID} = –1 V		20	31		
I_{CC}	Supply current	V_O = 0, No load, V_{IC} = 2.5 V		25°C		3.5	4.5	mA
				Full range			4.7	

(1) Full range is –40°C to 125°C.

OPERATING CHARACTERISTICS

V_{CC} = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR+	Positive slew rate	A_{VD} = –1, R_L = 2 kΩ, C_L = 100 pF		27	45		V/μs
SR–	Negative slew rate	A_{VD} = –1, R_L = 2 kΩ, C_L = 100 pF		27	42		V/μs
t_s	Settling time	A_{VD} = –1, 10-V step	To 0.1%		0.34		μs
			To 0.01%		0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω	f = 10 Hz		15		$nV/\sqrt{Hz}$
			f = 1 kHz		10.5		
$V_{n(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.89		$pA/\sqrt{Hz}$
		f = 1 kHz			0.47		
THD+N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, R_L = 2 kΩ, A_{VD} = 10, f = 10 kHz			0.01		%
B_1	Unity-gain bandwidth	R_L = 2 kΩ, C_L = 100 pF			6		MHz
	Gain-bandwidth product	R_L = 2 kΩ, C_L = 100 pF, f = 100 kHz			5.9		MHz
BOM	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, A_{VD} = 1, R_L = 2 kΩ, C_L = 100 pF			668		kHz
φ_m	Phase margin at unity gain	R_L = 2 kΩ, C_L = 100 pF			58		°

TYPICAL CHARACTERISTICS

Table 1. Table of Graphs

V_{IO}	Input offset voltage		Distribution	Figure 2
I_{IO}	Input offset current		vs Free-air temperature	Figure 3
I_{IB}	Input bias current		vs Common-mode input voltage	Figure 4
			vs Free-air temperature	Figure 5
V_{OM+}	Maximum positive peak output voltage		vs Supply voltage	Figure 6
			vs Free-air temperature	Figure 7
			vs Output current	Figure 8
			vs Settling time	Figure 10
$V_{OM–}$	Maximum negative peak output voltage		vs Supply voltage	Figure 6
			vs Free-air temperature	Figure 7
			vs Output current	Figure 9
			vs Settling time	Figure 10
$V_{O(PP)}$	Maximum peak-to-peak output voltage		vs Frequency	Figure 11
V_{OH}	High-level output voltage		vs Output current	Figure 12
V_{OL}	Low-level output voltage		vs Output current	Figure 13
	Phase shift		vs Frequency	Figure 14
A_{VD}	Large-signal differential voltage amplification		vs Frequency	Figure 14
			vs Free-air temperature	Figure 15
z_o	Closed-loop output impedance		vs Frequency	Figure 16
I_{OS}	Short-circuit output current		vs Free-air temperature	Figure 17
CMRR	Common-mode rejection ratio		vs Frequency	Figure 18
			vs Free-air temperature	Figure 19
k_{SVR}	Supply-voltage rejection ratio		vs Frequency	Figure 20
			vs Free-air temperature	Figure 21
I_{CC}	Supply current		vs Supply voltage	Figure 22
			vs Free-air temperature	Figure 23
V_n	Equivalent input noise voltage		vs Frequency	Figure 24
V_n	Input noise voltage		Over a 10-second period	Figure 25
I_n	Noise current		vs Frequency	Figure 26
THD+N	Total harmonic distortion plus noise		vs Frequency	Figure 27
SR	Slew rate		vs Free-air temperature	Figure 28
			vs Load capacitance	Figure 29
	Pulse response	Noninverting large signal	vs Time	Figure 30
		Inverting large signal	vs Time	Figure 31
		Small signal	vs Time	Figure 32
B_1	Unity-gain bandwidth		vs Load capacitance	Figure 33
	Gain margin		vs Load capacitance	Figure 34
φ_m	Phase margin		vs Load capacitance	Figure 35

TLE2141
DISTRIBUTION OF
INPUT OFFSET VOLTAGE

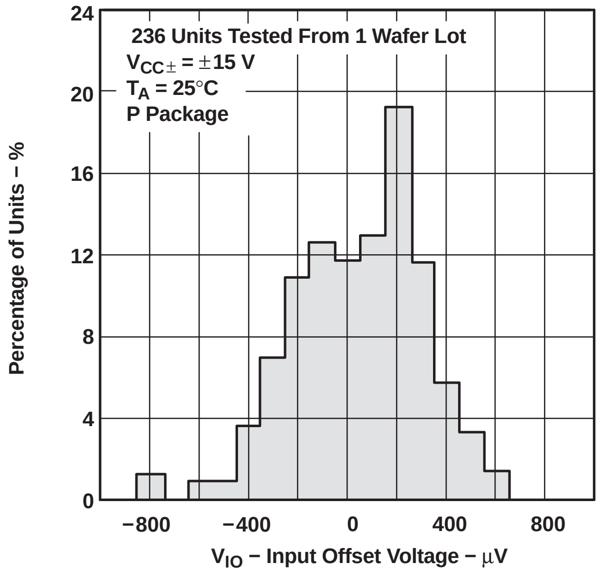


Figure 2.

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

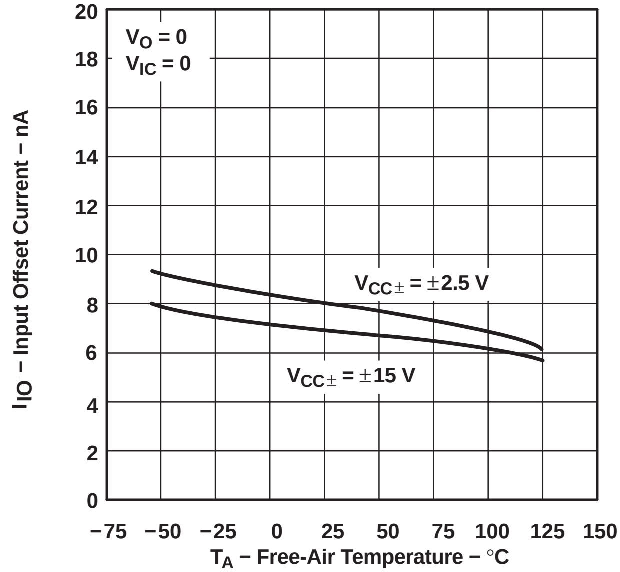


Figure 3.

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

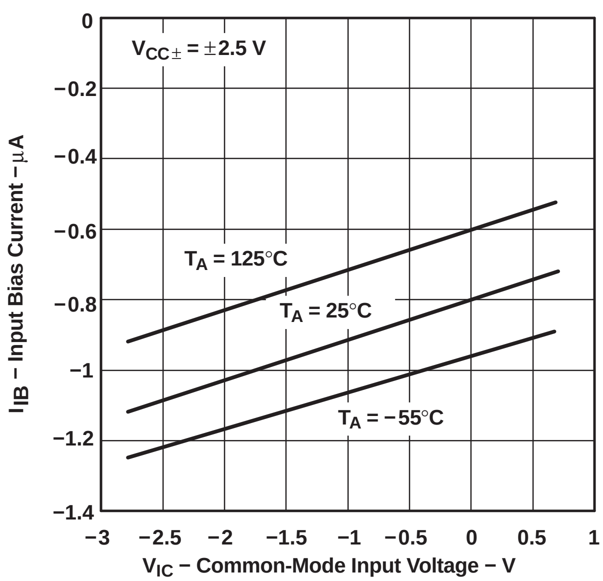


Figure 4.

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

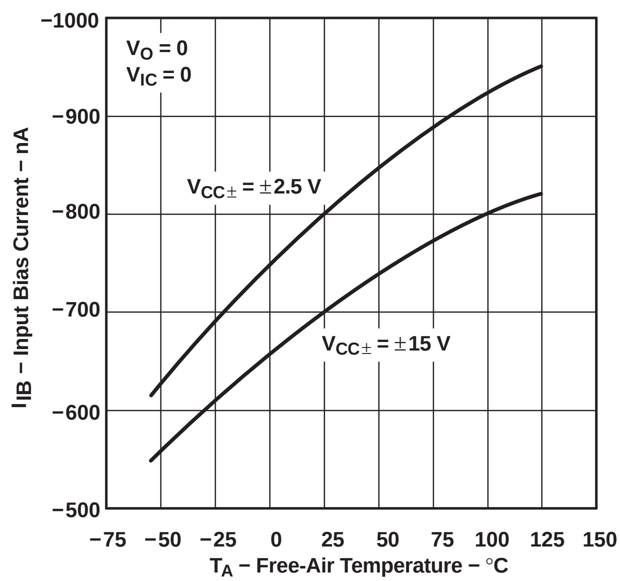


Figure 5.

**MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE**

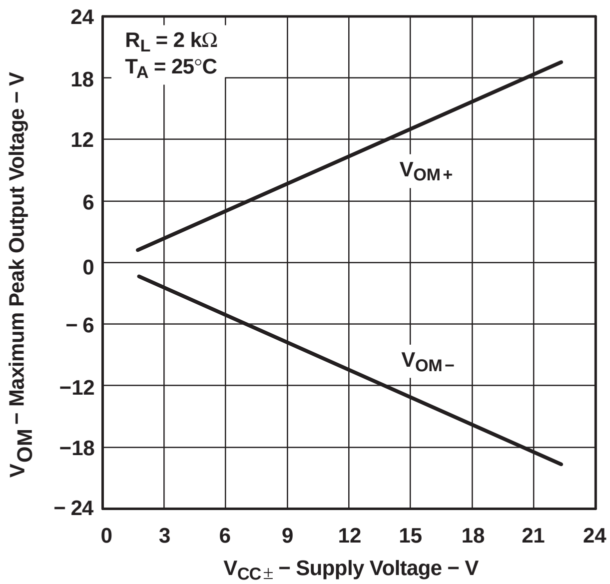


Figure 6.

**MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE**

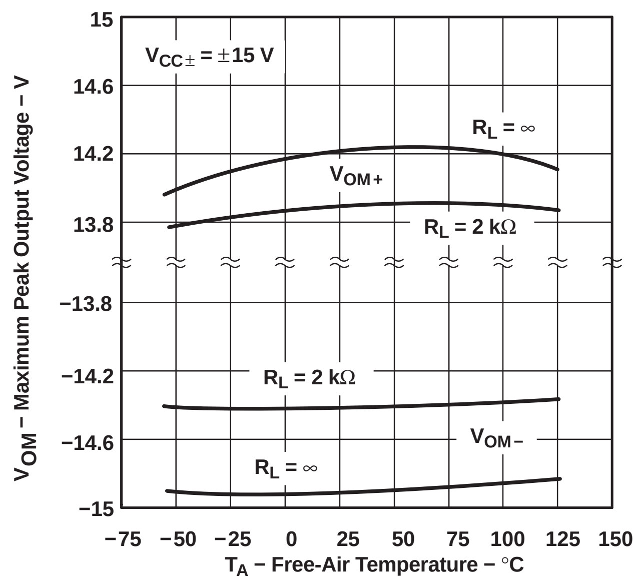


Figure 7.

**MAXIMUM POSITIVE PEAK
OUTPUT VOLTAGE
vs
OUTPUT CURRENT**

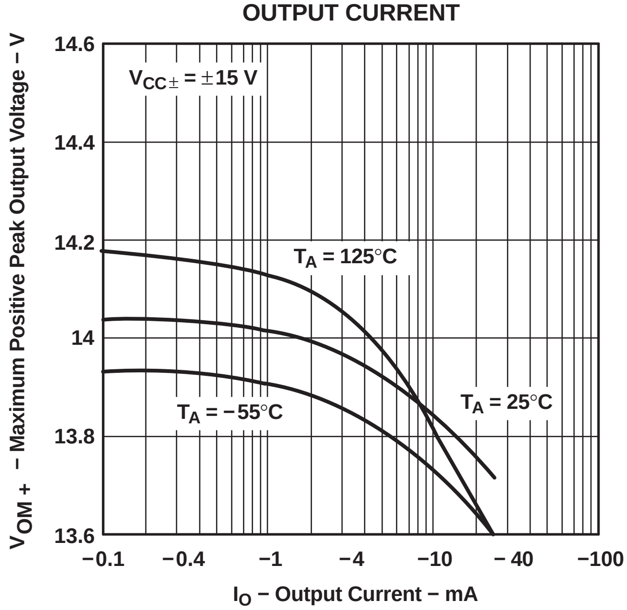


Figure 8.

**MAXIMUM NEGATIVE PEAK
OUTPUT VOLTAGE
vs
OUTPUT CURRENT**

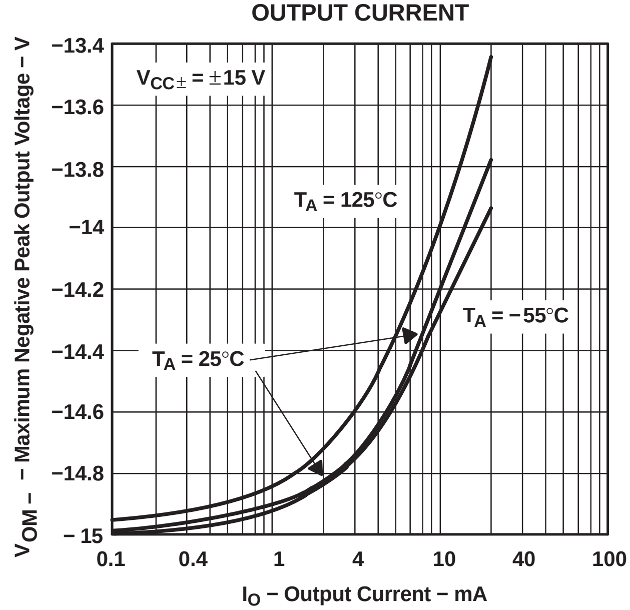


Figure 9.

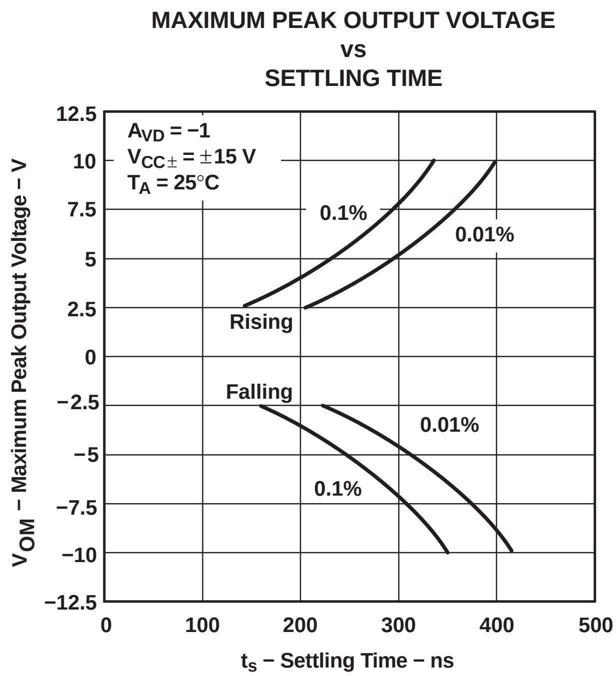


Figure 10.

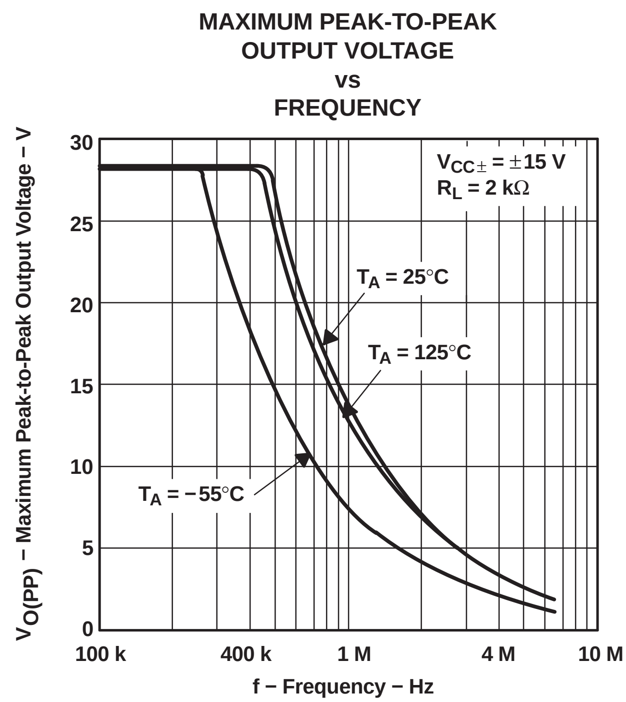


Figure 11.

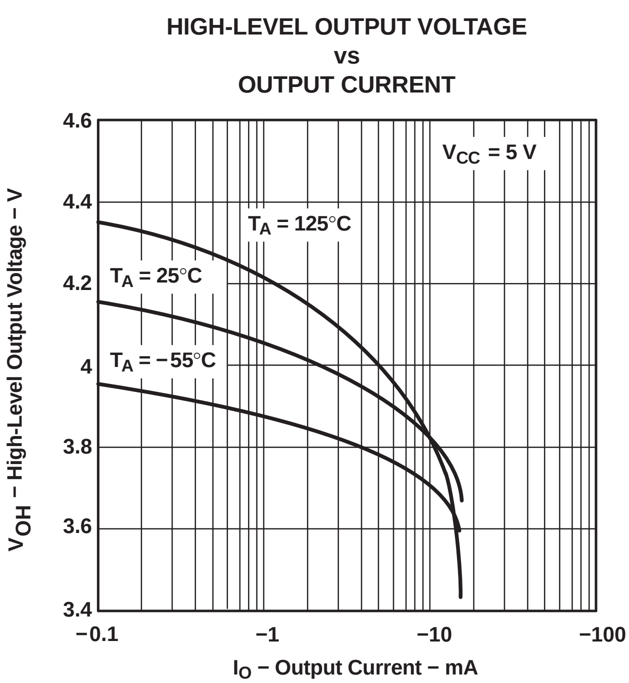


Figure 12.

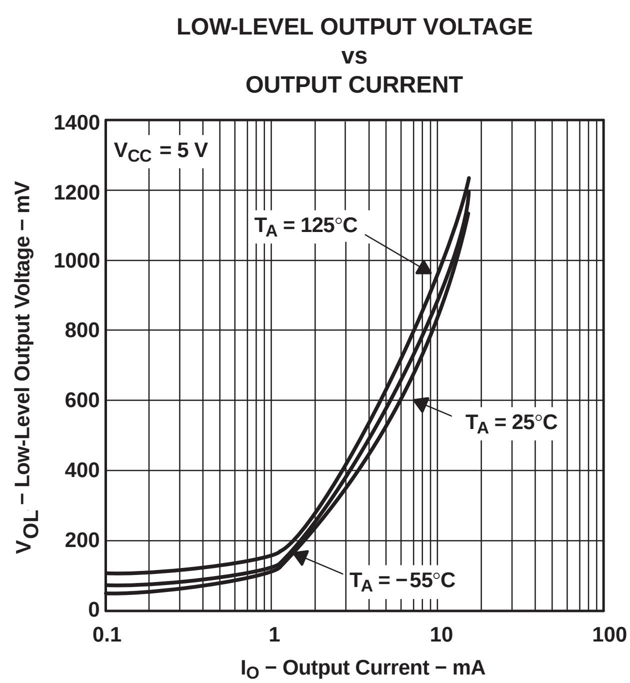


Figure 13.

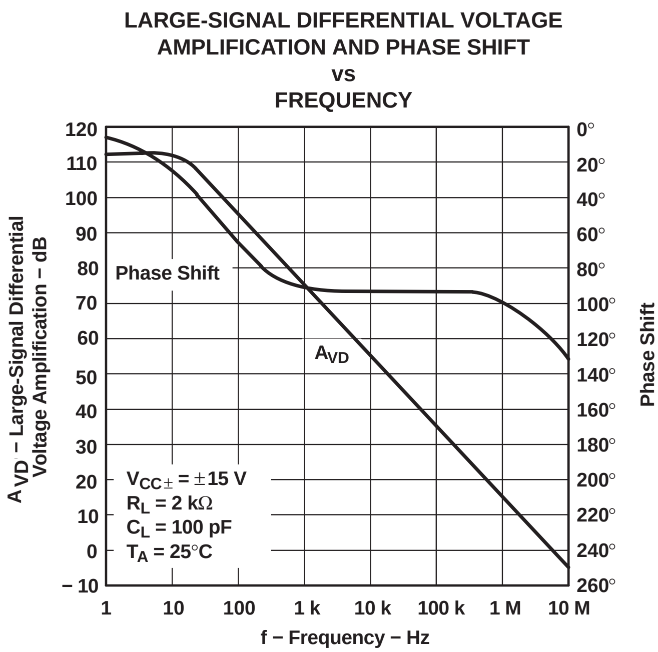


Figure 14.

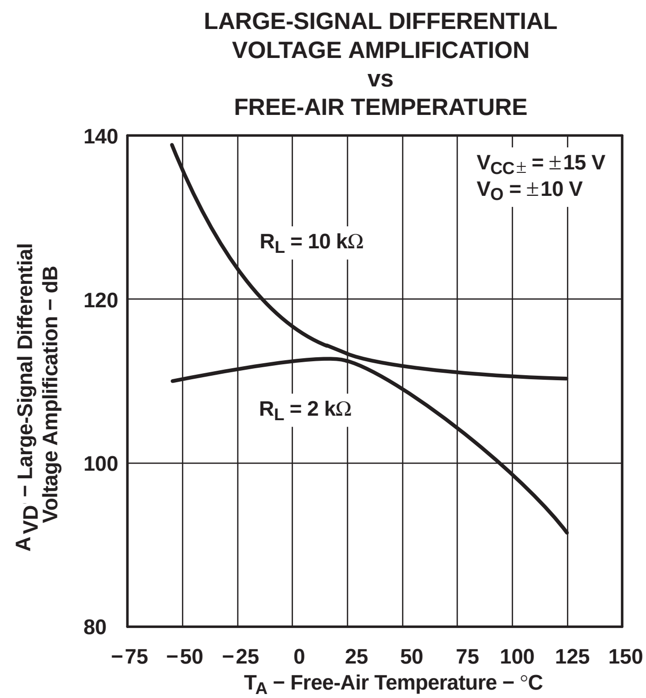


Figure 15.

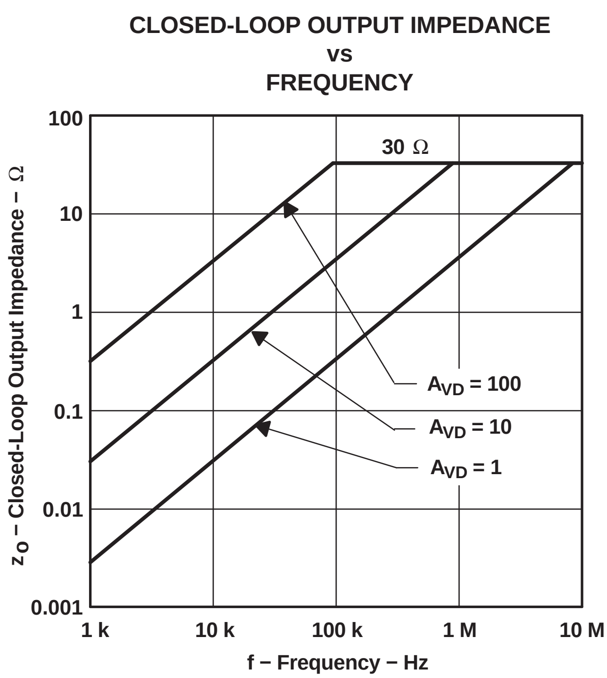


Figure 16.

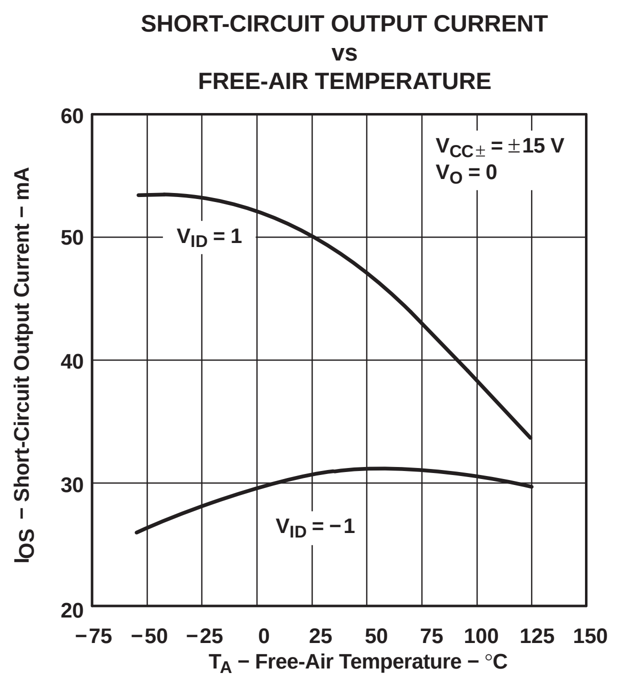


Figure 17.

COMMON-MODE REJECTION RATIO vs FREQUENCY

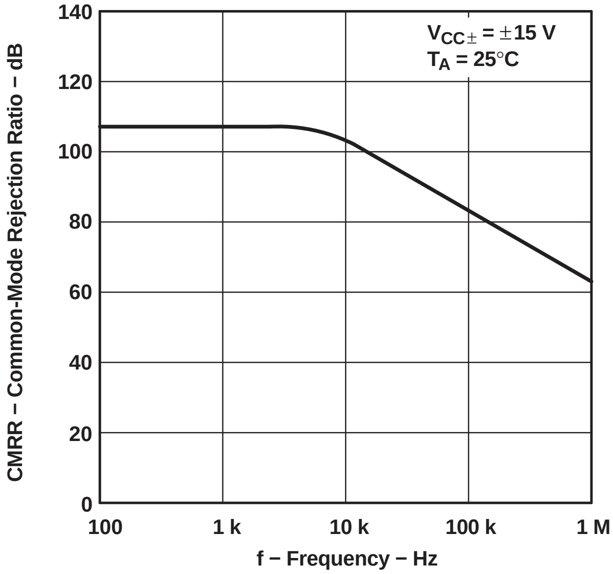


Figure 18.

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

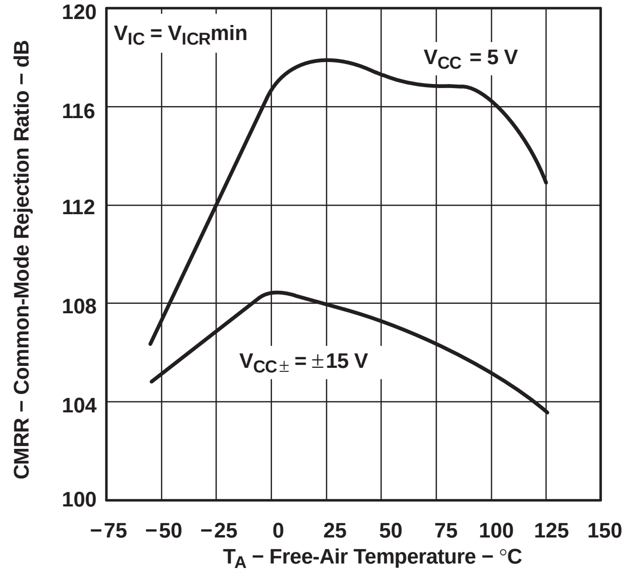


Figure 19.

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

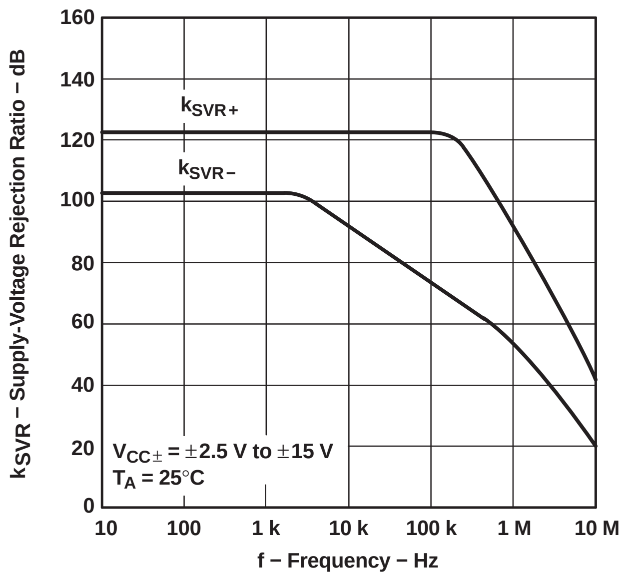


Figure 20.

SUPPLY-VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

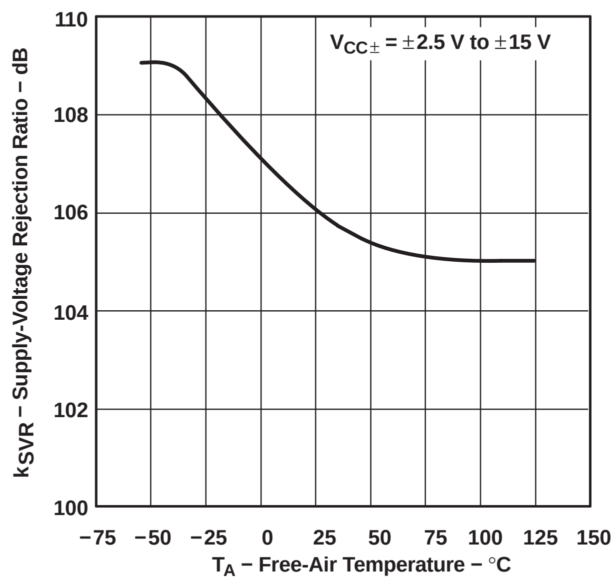


Figure 21.

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

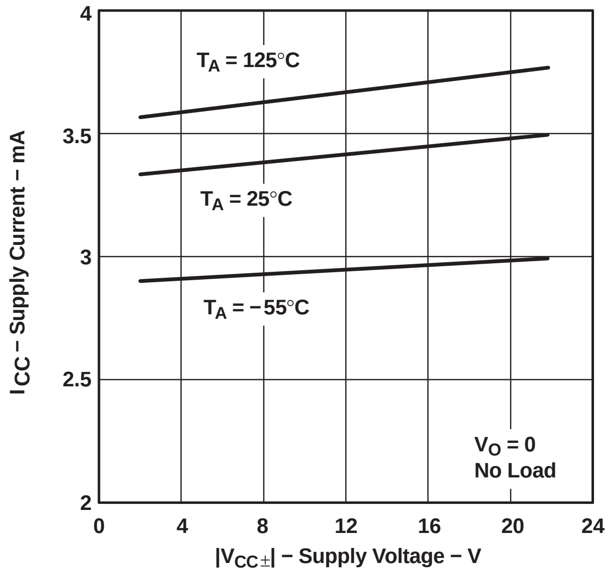


Figure 22.

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

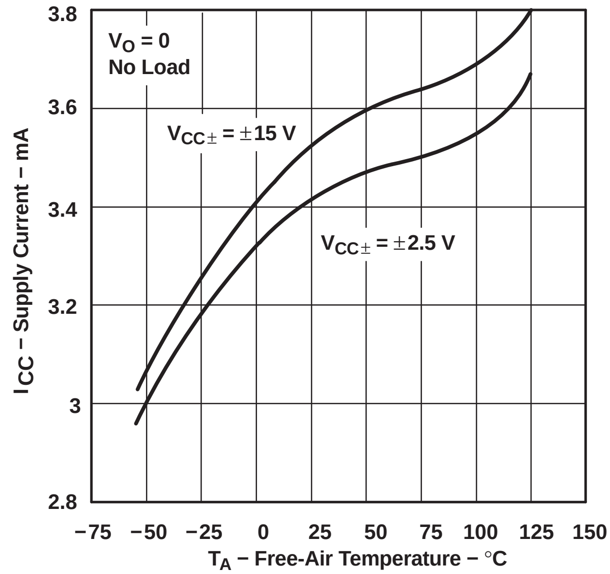


Figure 23.

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

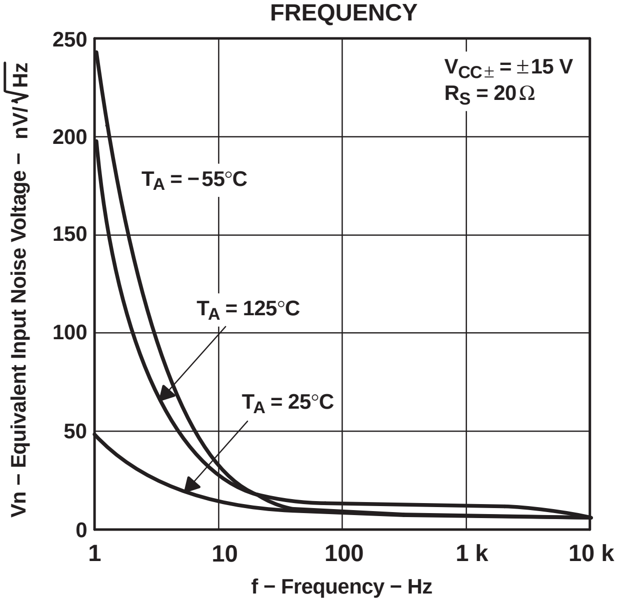


Figure 24.

INPUT NOISE VOLTAGE
OVER A 10-SECOND PERIOD

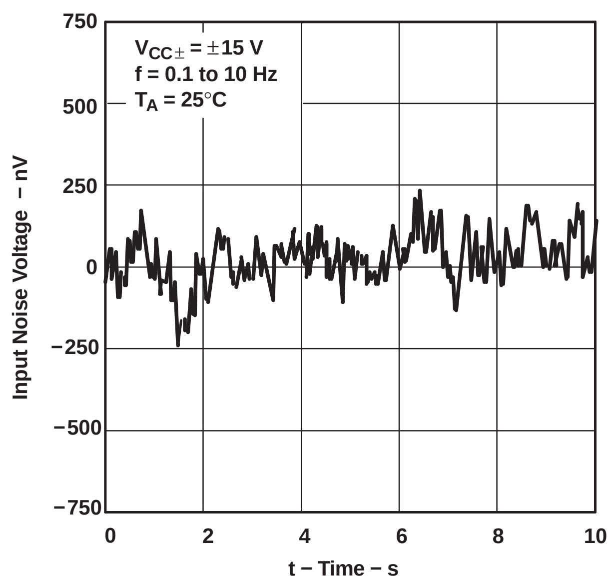


Figure 25.

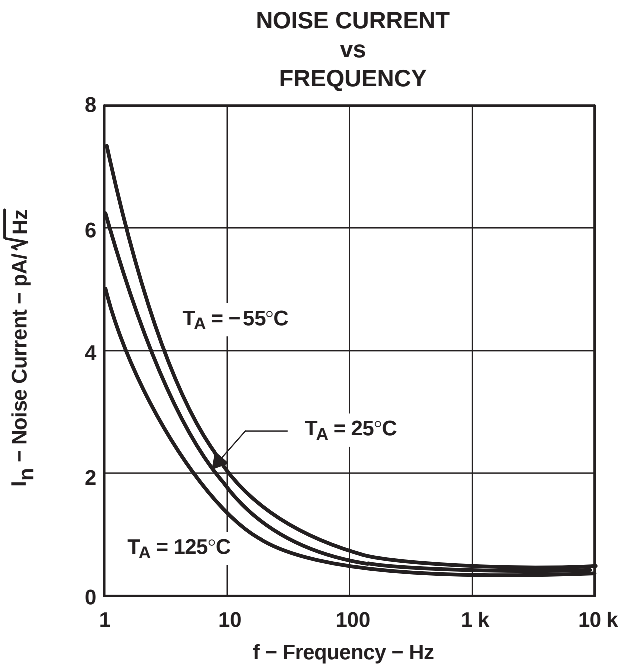


Figure 26.

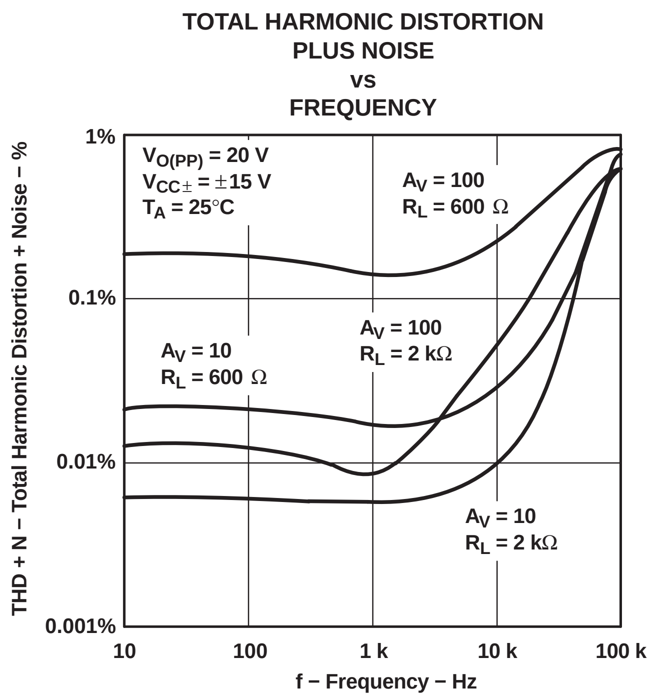


Figure 27.

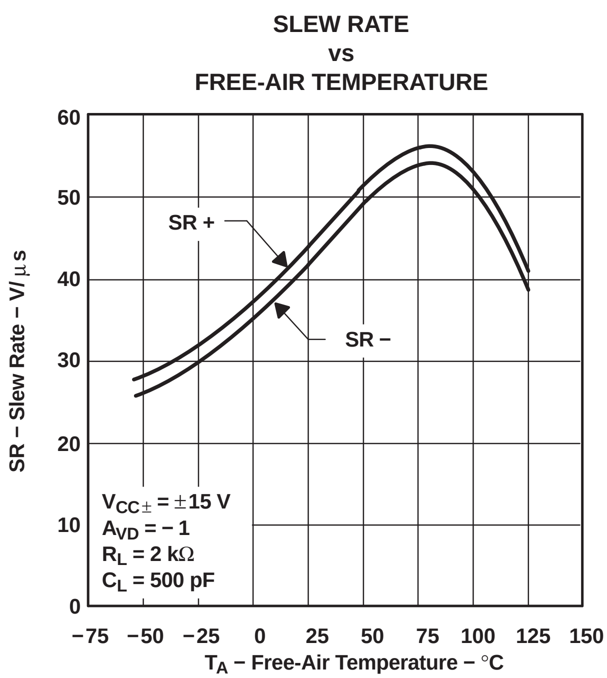


Figure 28.

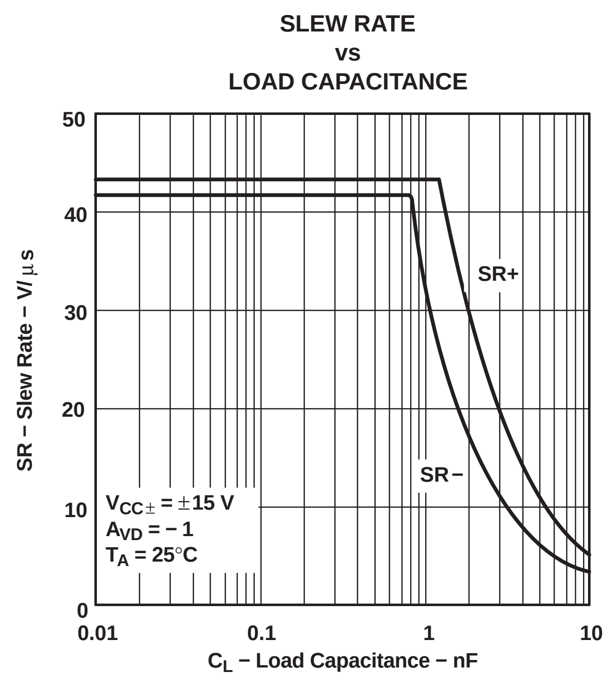


Figure 29.

NONINVERTING LARGE-SIGNAL PULSE RESPONSE

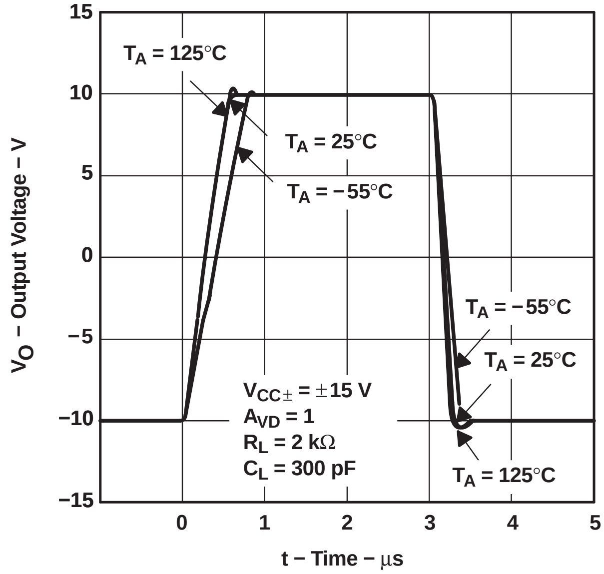


Figure 30.

INVERTING LARGE-SIGNAL PULSE RESPONSE

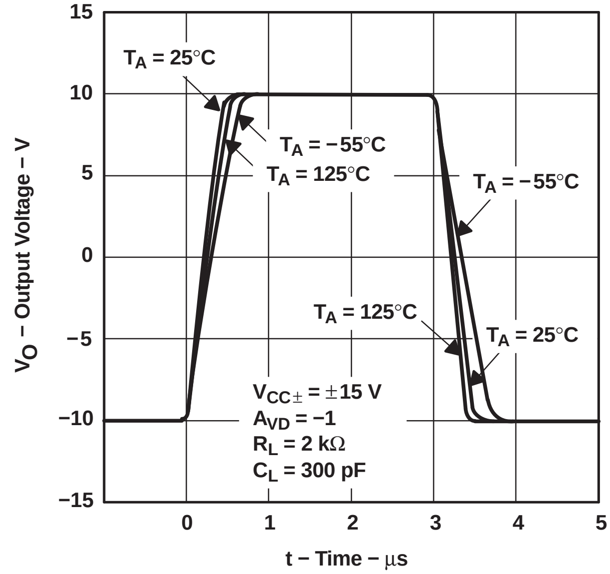


Figure 31.

SMALL-SIGNAL PULSE RESPONSE

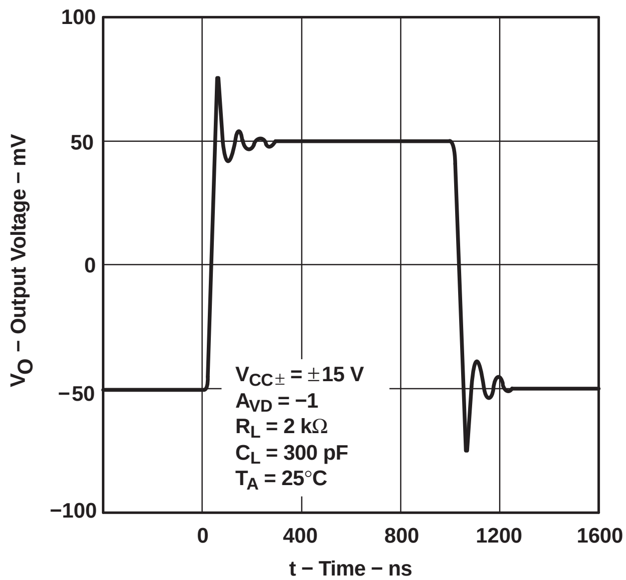


Figure 32.

UNITY-GAIN BANDWIDTH vs LOAD CAPACITANCE

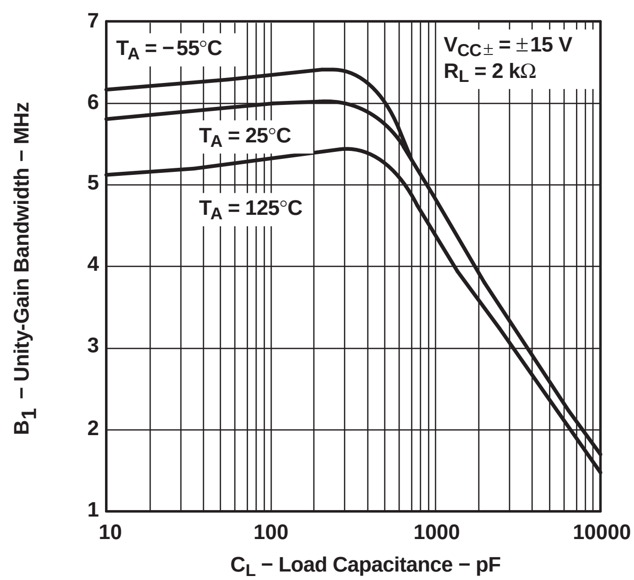


Figure 33.

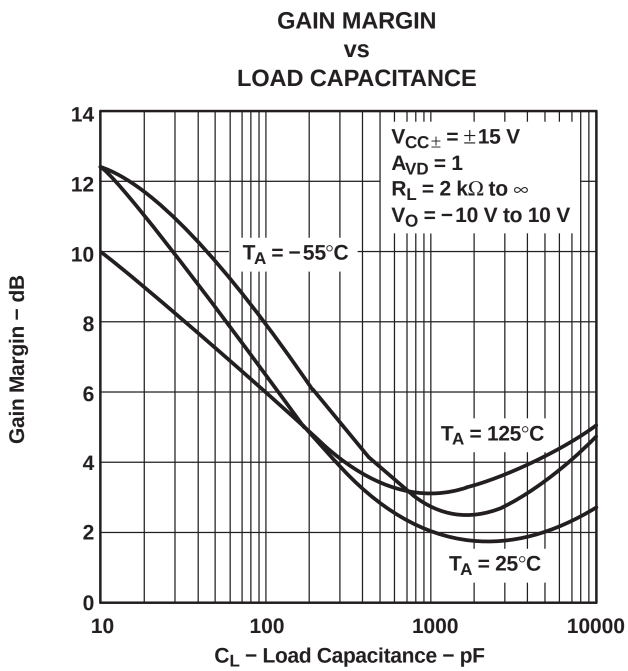


Figure 34.

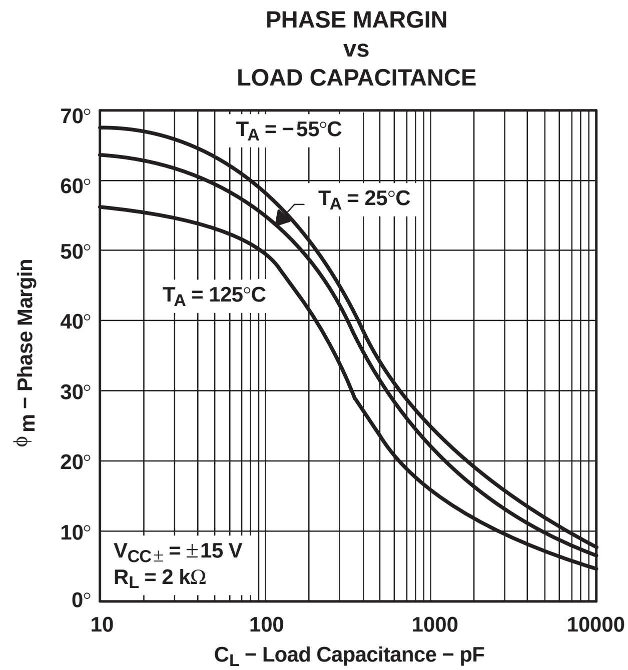


Figure 35.

APPLICATION INFORMATION

Input Offset Voltage Nulling

The TLE2141-Q1 offers external null pins that can be used to further reduce the input offset voltage. If this feature is desired, connect the circuit of Figure 36 as shown. If external nulling is not needed, the null pins may be left unconnected.

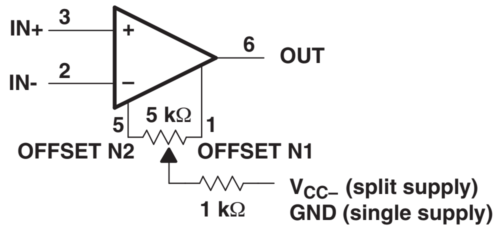


Figure 36. Input Offset Voltage Null Circuit

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TLE2141QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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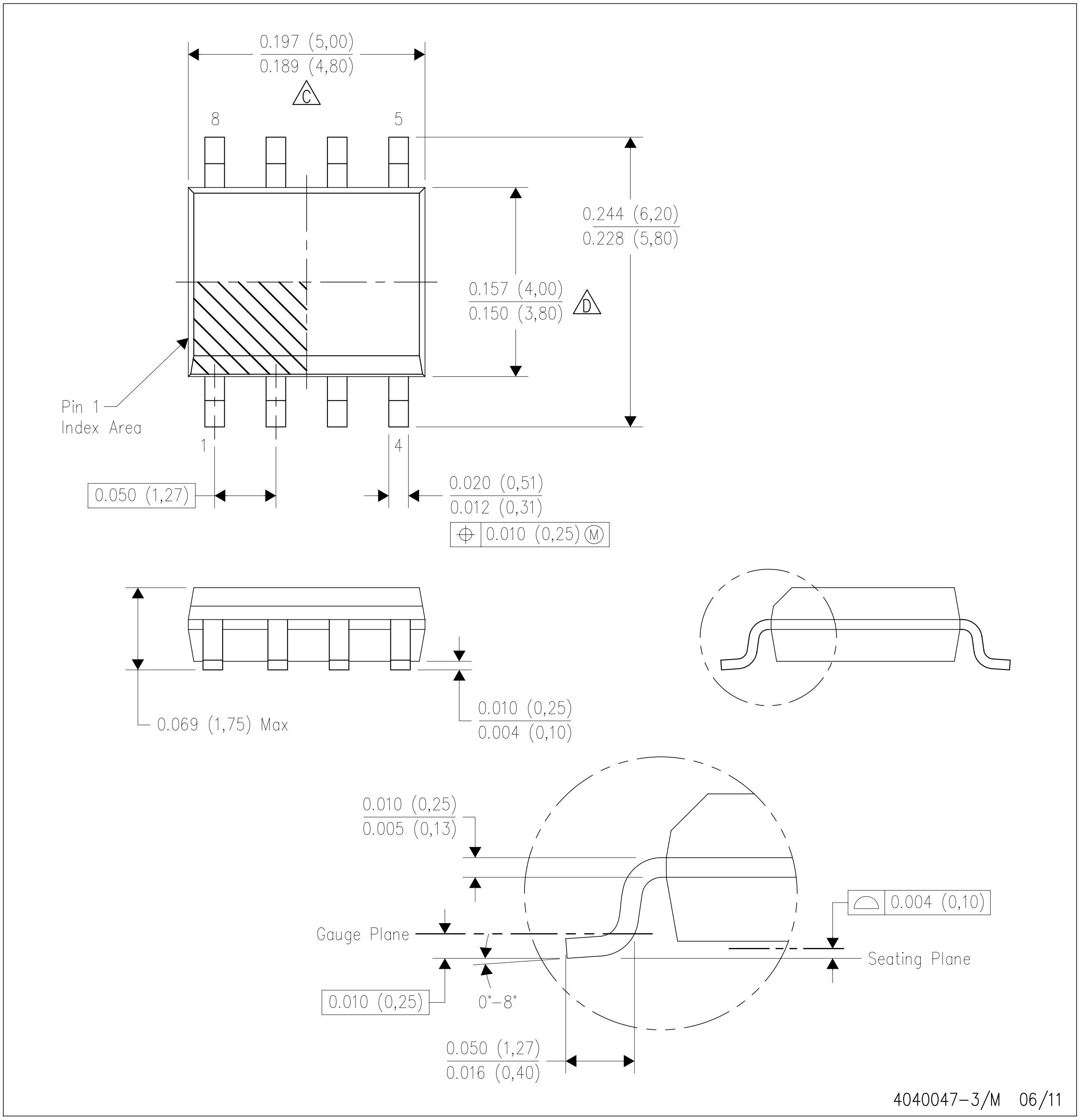
OTHER QUALIFIED VERSIONS OF TLE2141-Q1 :

- Catalog: TLE2141
- Enhanced Product: TLE2141-EP
- Military: TLE2141M

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

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