SIEMENS

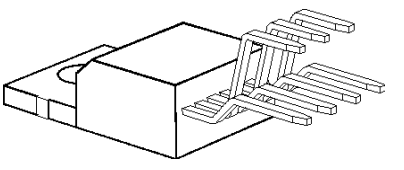
Intelligent Double Low-Side Switch 2 x 2 A

TLE 4211

Bipolar IC

Features

- Double low-side switch, 2 x 2 A
- Power limitation
- Overtemperature shutdown
- Status monitoring
- Shorted-load protection
- Reverse polarity protection
- Integrated clamp Z-Diodes
- Voltage proof up to 70 V
- Temperature range – 40 to 125 °C



P-TO220-7-1

Type	Ordering Code	Package
TLE 4211	Q67000-A8118	P-TO220-7-1

Application

Applications in automotive electronics require intelligent power switches activated by logic signals, which are also shorted-load protected and provide error feedback.

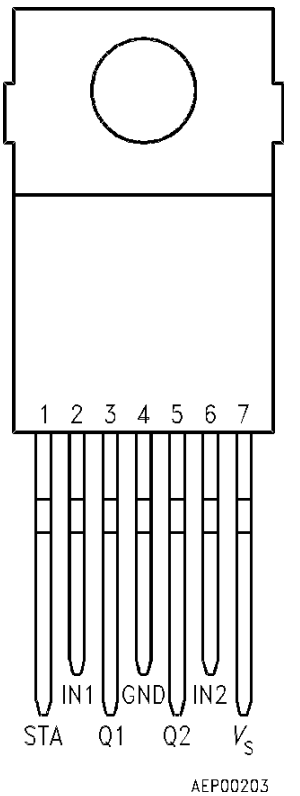
The IC contains two of these power switches (low-side switch). In case of inductive loads the integrated power Z-diodes clamp the discharging voltage.

Through TTL signals at the control inputs (active low) both switches can be activated independently of one another. If one of the inputs is not in use, it must be applied to high potential.

The status output (open collector) signals the following malfunctions through low potential:

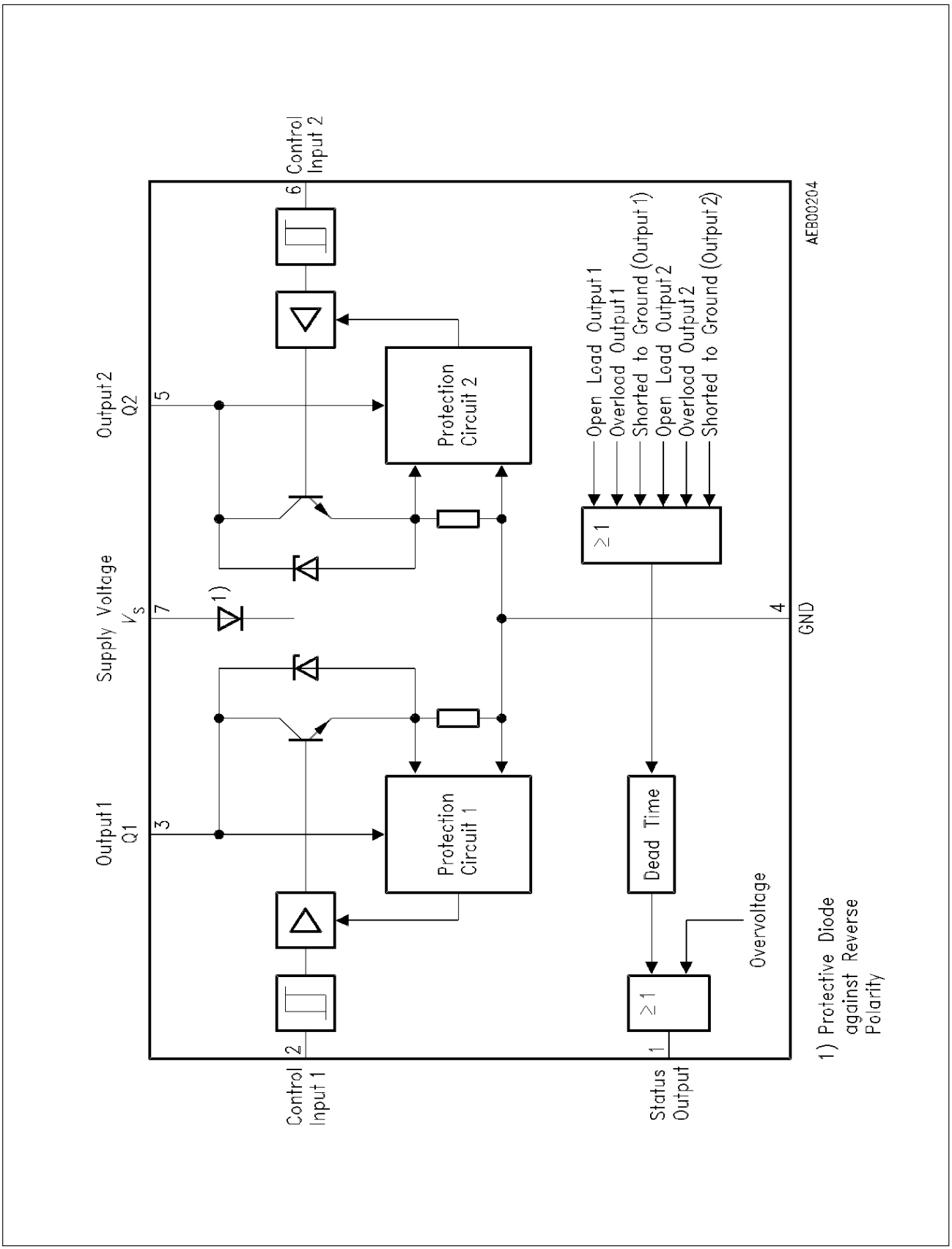
- Overload,
- Open load,
- Shorted load to ground,
- Overvoltage.

Pin Configuration
(top view)



Pin Definitions and Functions

Pin No.	Symbol	Function
1	STA	**Status output (open collector)** for both outputs; indicates overload, open load and shorted load to ground as well as overvoltage at pin 7. In case of malfunction the status output is switched to low after a delay time (except overvoltage).
2	IN1	**Control input 1 (TTL-compatible)** activates output transistor 1 in case of low-potential.
3	Q1	**Output 1** Shorted-load protected, open collector output with 36 V clamp Z-diode to ground.
4	GND	**Ground** Wiring must be designed for a max. short-circuit current (2 x 3.5 A).
5	Q2	**Output 2** Shorted-load protected, open collector output with 36 V clamp Z-diode to ground.
6	IN2	**Control input 2 (TTL-compatible)** activates output transistor 2 in case of low-potential.
7	V_S	**Supply voltage** In case of overvoltage at this pin large sections of the circuit are deactivated. The status output indicates the malfunction without delay time.



Block Diagram

Circuit Description

Input Circuits

The control inputs comprise TTL-compatible Schmitt triggers with hysteresis. Driven by these stages the inverting buffer amplifiers convert the logic signal for driving the NPN power transistors.

Switching Stages

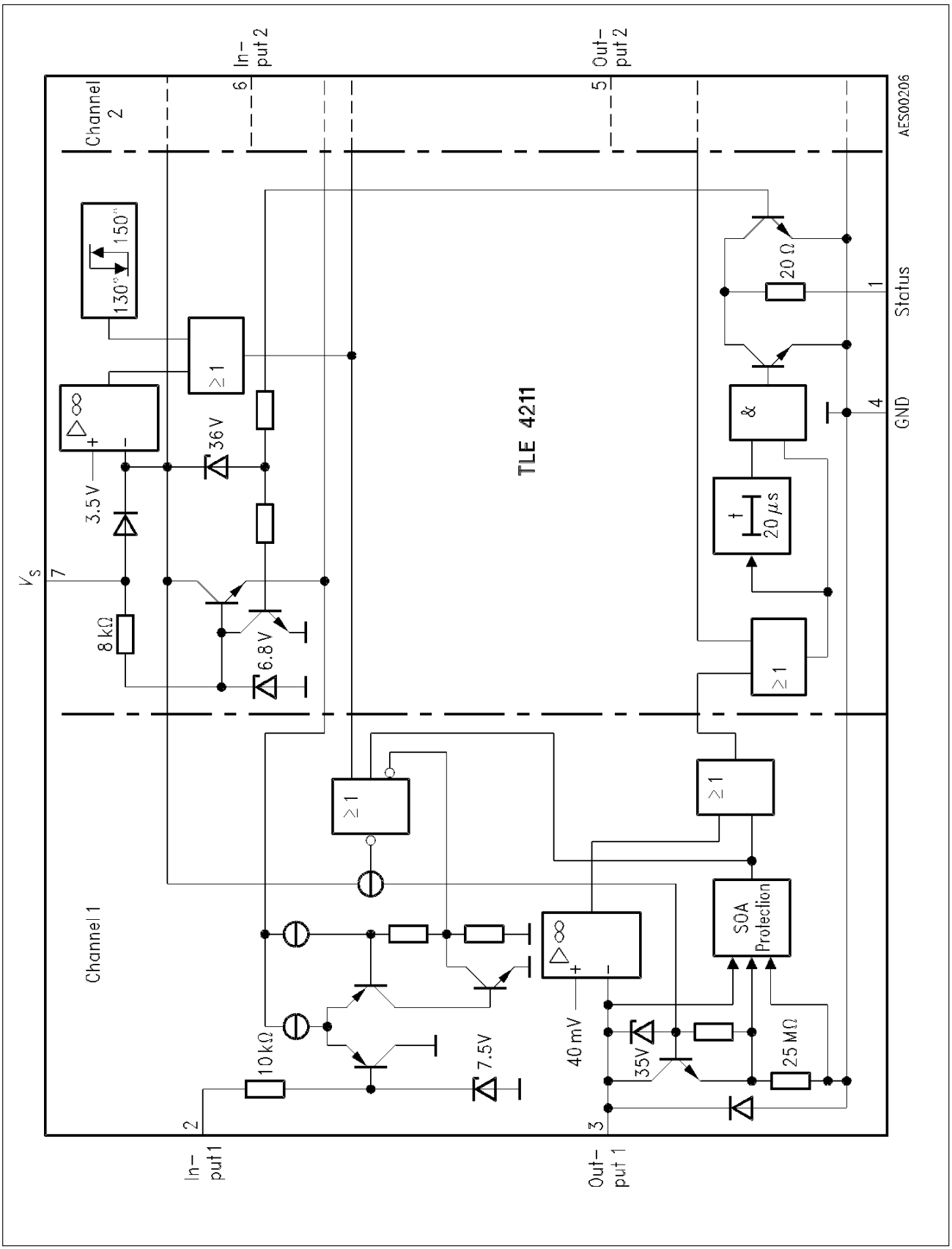
The output stages comprise NPN power transistors with open collectors. Since the protective circuit allocated to each stage limits the power dissipation, the outputs are shorted-load protected to the supply voltage throughout the entire operating range. Positive voltage peaks, which occur during the switching of inductive loads, are limited by the integrated clamp Z-diodes.

Monitoring and Protective Functions

The outputs are monitored for open load, overload, and shorted load to ground (**see table below**). In addition, large sections of the circuit are de-activated in case of excessive supply voltages V_S. Linked via OR gate the information regarding these malfunctions effects the status output (open collector, active low). An internally determined delay time applied to all malfunctions but overvoltage prevents the output of messages in case of short-term malfunctions. Furthermore, a temperature protection circuit prevents thermal overload. An integrated reverse diode protects the supply voltage V_S against reverse polarities. Similarly the load circuit is protected against reverse polarities within the limits established by the maximum ratings (no shorted load at the same time!). At supply voltages below the operating range an undervoltage detector ensures that neither the status nor the outputs are activated.

Status Output (L = Error)

	Undervoltage	**Operating Range**		**Overvoltage**
		V_I = L (active)	V_I = H (passive)	
Normal function	H	H	H	L
Overload	H	L	H	L
Open load	H	L	H	L
Shorted load to ground	H	L	L	L



Circuit Diagram

Absolute Maximum Ratings

T_A = – 40 to 125 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Voltages				
Supply voltage (pin 7) [1]	V_S	– 45	45	V
Supply voltage (pin 7) $t \leq 500$ ms	V_S	–	70	V
Input voltage (pin 2; pin 6)	V_I	– 5	45	V
Output voltage (pin 1)	V_O	– 0.3	45	V
Currents				
Switching current (pin 3; pin 5)	I_Q	limited internally		
Current with reverse polarity (pin 3; pin 5) $T_C \leq 85$ °C	I_Q	– 2.2	–	A
Output current (pin 1)	I_Q	–	10	mA
Max. current at inductive load	I_Q	–	**see Diagram**	
Junction temperature	T_j	–	150	°C
Storage temperature	T_{stg}	– 50	150	°C
Operating Range				
Supply voltage	V_S	5.6 [2]	20	V
Supply voltage slew rate	dV_S/dV	– 1	1	V/µs
Ambient temperature	T_A	– 40	125	°C
Thermal resistance				
junction to case	$R_{th\ JC}$	–	4	K/W
junction to ambient	$R_{th\ JA}$	–	65	K/W

1) Refer to monitoring and protective functions
2) Lower limit = 4.6 V, if previously V_S greater than 5.6 V (turn-on hysteresis)

Characteristics

V_S = 6 to 18 V and T_A = – 40 to 125 °C

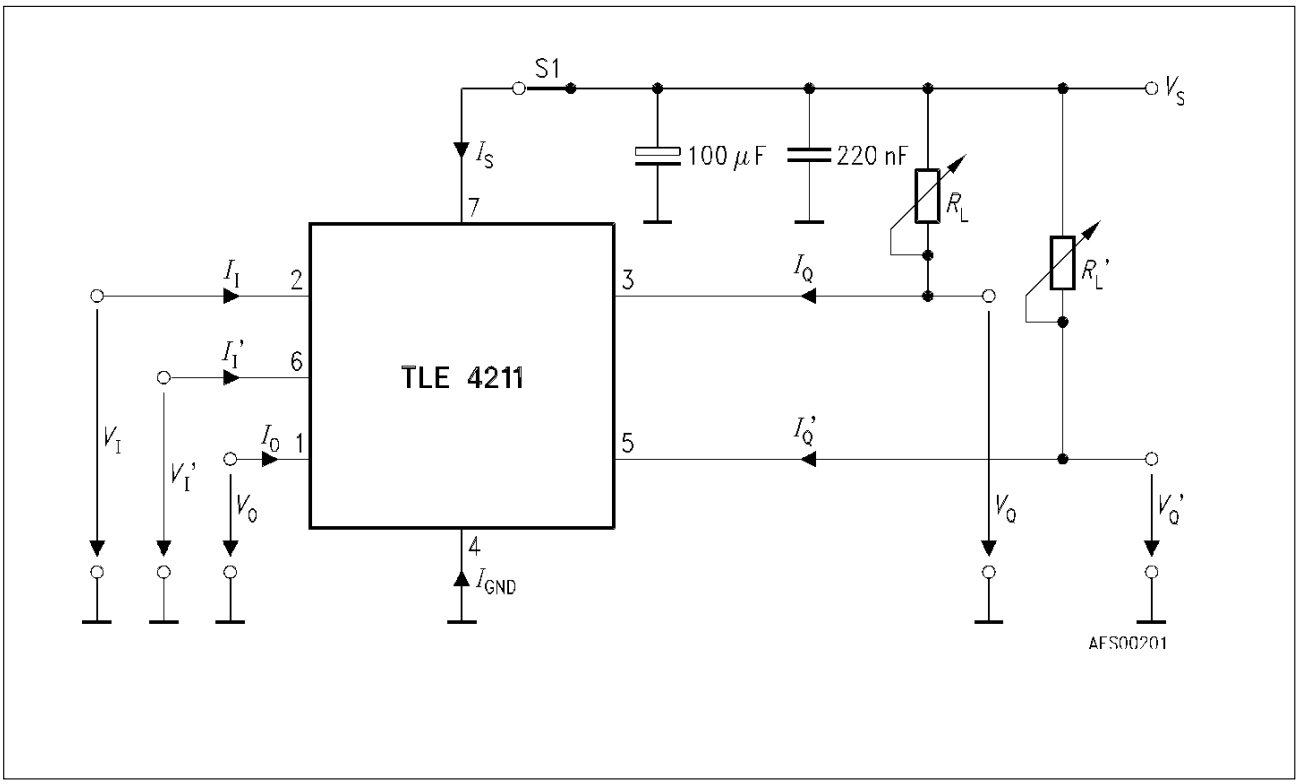
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
General Characteristics						
Quiescent current	I_S	–	3.5	10	mA	$V_I = V_I > V_{IH}$
Supply voltage	I_S	–	100	180	mA	$V_I = V_I < V_{IL}$
Supply overvoltage shutdown threshold	V_{SO}	34	36	42	V	$I_O = 5$ mA; $V_O < 0.4$ V
Open load error threshold voltage	V_{QU}	–	40	–	mV	$I_O = 5$ mA; $V_O < 0.4$ V
Open load error threshold current	I_{QU}	–	50	120	mA	$V_Q = V_{QU}$
Open load error threshold current for both channels active	I_{QU}	–	–	250	mA	$V_{Q1} = V_{Q2} = V_{QU}$
Logic						
Control input H-input voltage L-input voltage	 V_{IH} V_{IL}	 – 0.7	 1.7 1.1	 2.4 –	 V V	 – –
Hysteresis of input voltage	ΔV_I	–	0.6	–	V	–
H-input current L-input current	I_{IH} $-I_{IL}$	– –	– –	10 10	µA µA	$V_I = 5$ V $V_I = 0.5$ V
Status output (open coll.) L-saturation voltage	V_{OSat}	–	–	0.4	V	$I_O = 5$ mA
Status delay time	t_{dS}	12	20	30	µs	[1]

[1] Period from the beginning of the disturbance at one channel (exception: overvoltage) until the 50 % value of the status switching edge is reached.

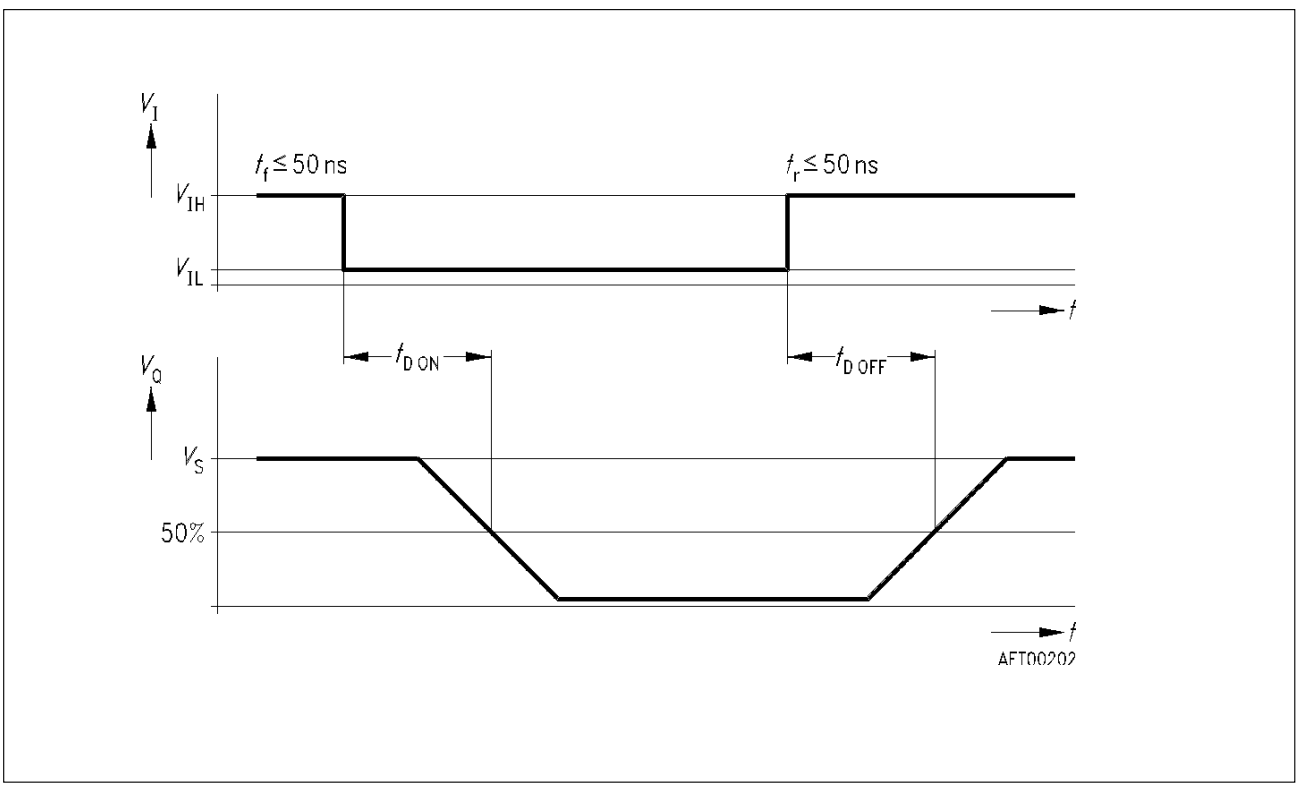
Characteristics (cont'd)

V_S = 6 to 18 V and T_A = – 40 to 125 °C

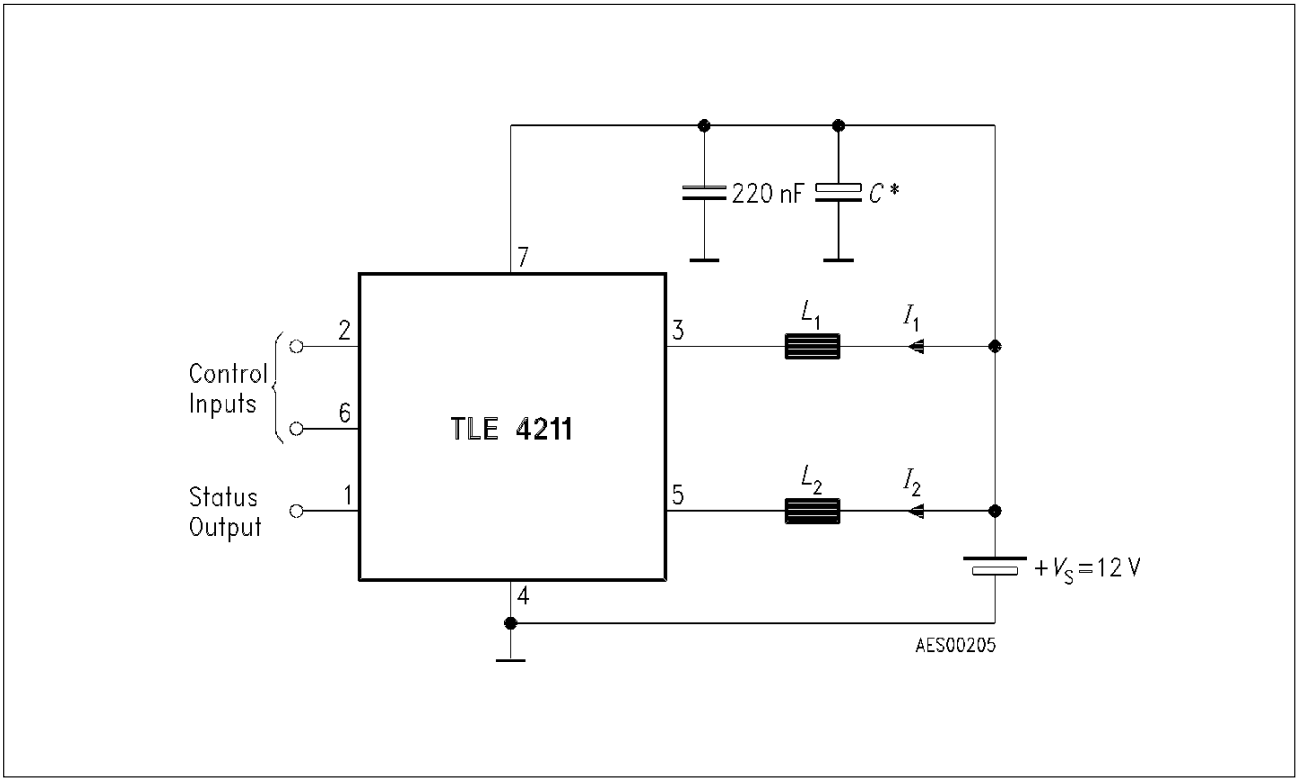
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Power Output						
Saturation voltage	V_{QSat}	–	0.6	0.8	V	I_Q = 1.6 A; $V_I < V_{IL}$; T_j = 25 °C
Leakage current	I_Q	–	–	300	µA	V_Q = 6 V; $V_I > V_{IH}$
Switch-ON time Switch-OFF time	$t_{D\ ON}$ $t_{D\ OFF}$	– –	0.5 2.5	5 10	µs µs	**see Timing Diagram**; I_Q = 1 A
Output voltage Negative clamp	$-V_{QF}$	–	1.4	1.8	V	I_Q = – 2.0 A
Power Clamp Diode (V_S = 42 V; S_1 open)						
Output voltage positive clamp	V_{QZ}	34	36	40	V	I_Q = 0.1 A
Serial resistance	r_z	–	2	–	Ω	0 A < I_Q < 2 A



Test Circuit



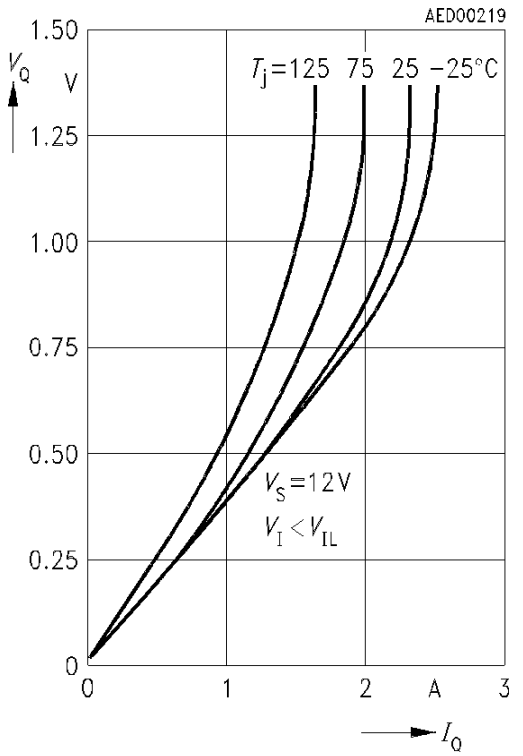
Timing Diagram



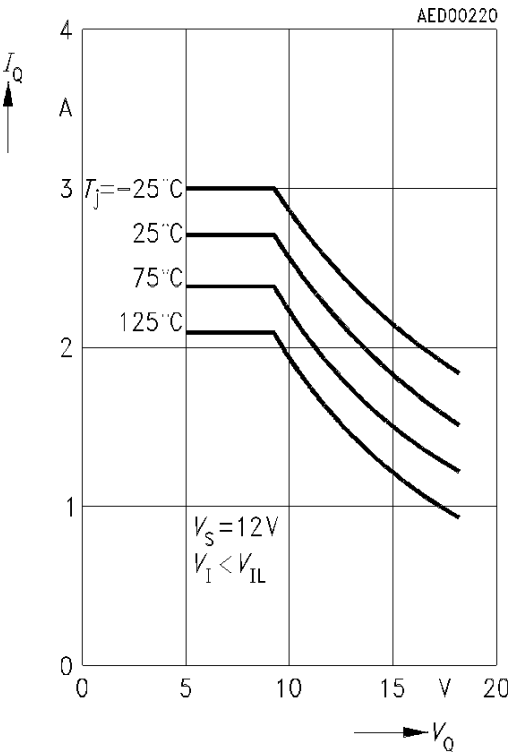
Application Circuit

C* is to be dimensioned such that e.g. in case of a battery voltage failure the maximum ratings of the IC are not exceeded by the recirculation energy L_1, L_2.

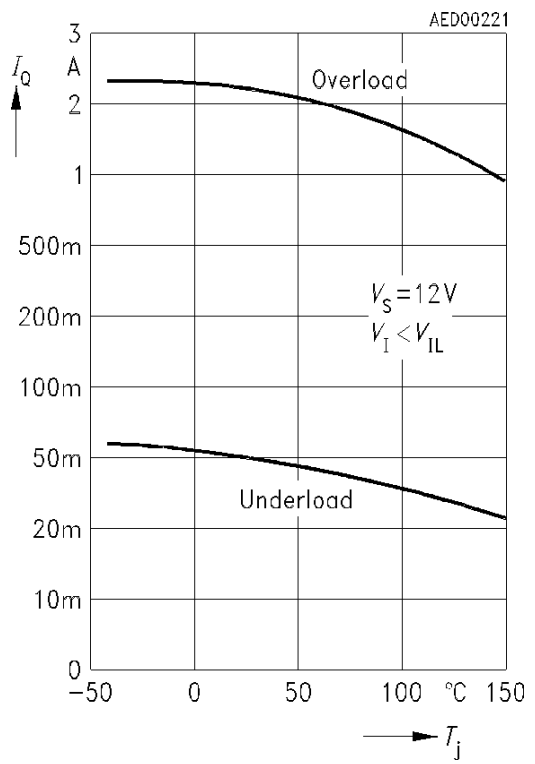
Output Voltage V_Q versus Output Current I_Q



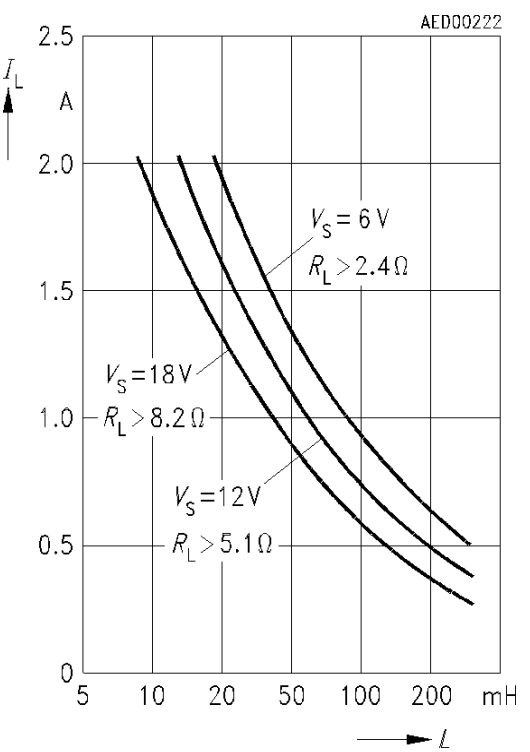
Shorted Load Current I_{Q0} versus Output Voltage V_Q



Status Signal Threshold versus Chip Temperature T_j



Maximum Load Current I_L versus Load Inductance L



SIEMENS

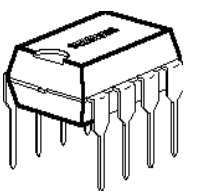
Intelligent Double Low-Side Switch 2 x 0.5 A

TLE 4214

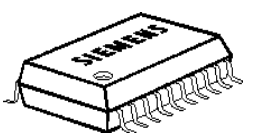
Bipolar IC

Features

- Double low-side switch, 2 x 0.5 A
- Power limitation
- Overtemperature shutdown
- Overvoltage shutdown
- Status monitoring
- Shorted-load protection
- Integrated clamp diodes
- Temperature range – 40 to 125 °C



P-DIP-8-1



P-DSO-20-7

Type	Ordering Code	Package
TLE 4214	Q67000-A8183	P-DIP-8-1
TLE 4214 G	Q67000-A9094	P-DSO-20-7 (SMD)

Application

Applications in automotive electronics require intelligent power switches activated by logic signals, which are also shorted-load protected and provide error feedback.

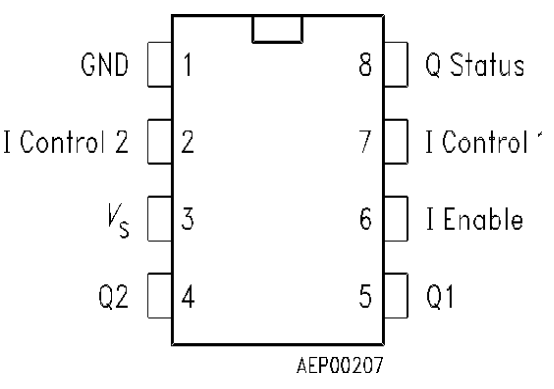
The IC contains two of these power switches (low-side switches). In case of inductive loads the integrated clamp diodes clamp the discharging voltage. If a “high” signal is applied to the enable input both switches can be activated independently of one another through TTL signals at the control inputs (active high). The high impedance inputs and must therefore not be left unconnected, but should always be connected to a fixed potential (noise immunity).

The status output (open collector) signals the following malfunctions through high potential:

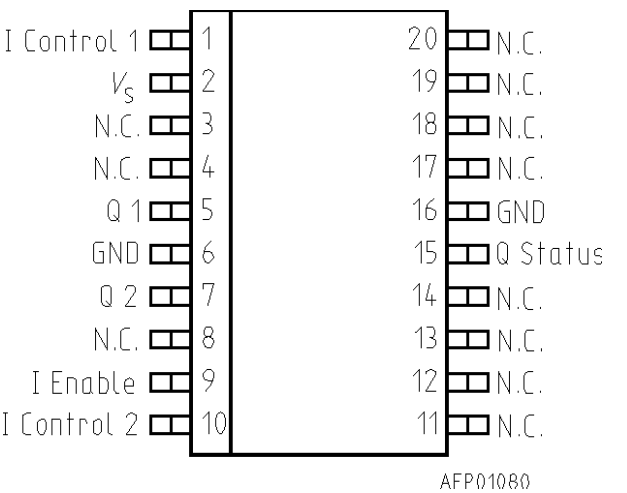
- Overload,
- Open load,
- Shorted load to ground,
- Overvoltage,
- Overtemperature.

Pin Configuration
(top view)

TLE 4214

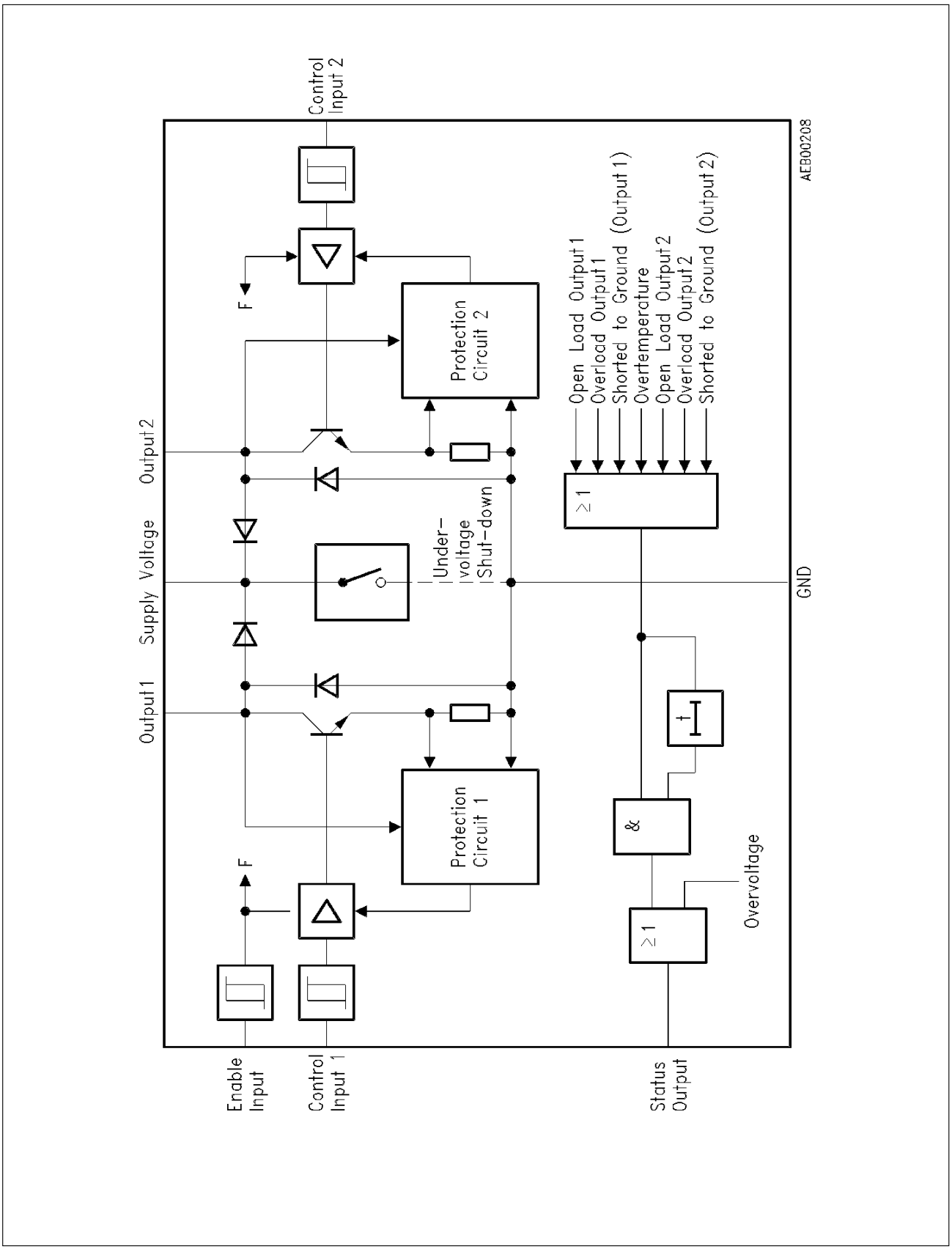


TLE 4214 G



Pin Definitions and Functions

TLE 4214 G	TLE 4214	Symbol	Function
Pin No.	**Pin No.**		
6, 16	1	GND	**Ground** Design wiring for the max. short-circuit current (2 x 1 A)
10	2	IN2	**Control input 2** (TTL compatible) activates the output transistor 2 in case of high potential
2	3	V_S	**Supply voltage** In case of overvoltage at this pin large sections of the circuit are deactivated. The status output indicates this malfunction without delay time.
7	4	Q2	**Output 2** Shorted load protected, open collector output for currents up to 0.5 A, with clamping diodes to supply voltage.
5	5	Q1	**Output 1** Shorted load protected, open collector output for currents up to 0.5 A, with clamping diodes to supply voltage.
9	6	ENA	**Enable input**, active high
1	7	IN1	**Control input 1** (TTL-compatible) activates output transistor 1 in case of high potential
15	8	STA	**Status output** (open collector) for both outputs; indicates overtemperature, overload, open load and shorted load to ground as well as overvoltage at pin 3. Is switched to high after a defined delay time in case of malfunction (except: overvoltage)
3, 4, 8, 11 … 14, 17 … 20		N. C.	Not connected



Block Diagram

Circuit Description

Input Circuits

The control inputs and the enable input consist of TTL-compatible Schmitt triggers with hysteresis. Driven by these stages the buffer amplifiers convert the logic signal necessary for driving the NPN power transistors.

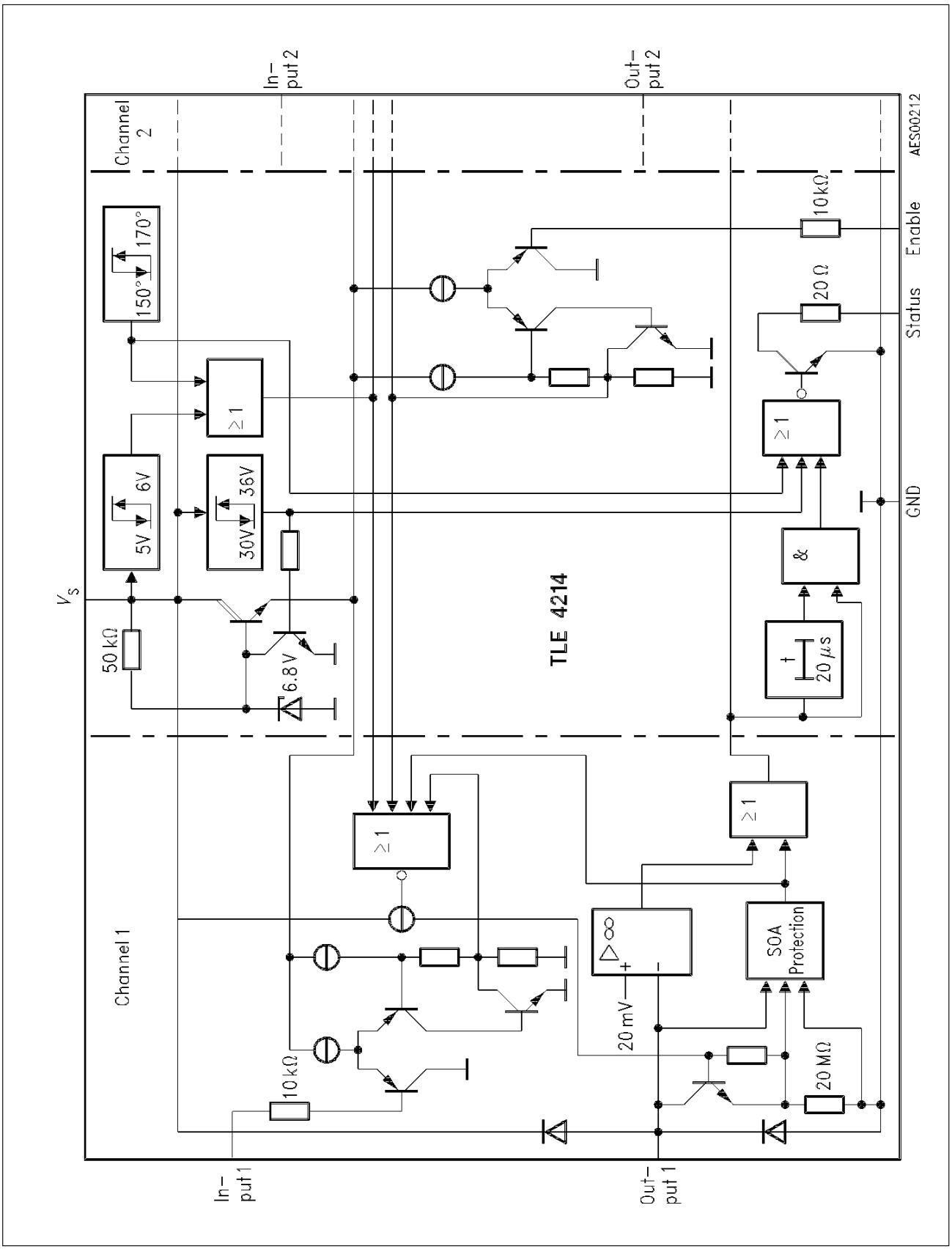
Switching Stages

The output stages consist of NPN power transistors with open collectors. Since the protective circuit allocated to each stage limits the power dissipation, the outputs are shorted-load protected to the supply voltage throughout the entire operating range. Positive voltage peaks, which occur during the switching of inductive loads, are limited by the integrated clamp diodes.

Monitoring and Protective Functions

During the activated status the outputs are monitored for open load, overload, and shorted load to ground (see table below). In addition, large sections of the circuit are shut down in case of excessive supply voltages V_S. Linked via OR gate the information regarding these malfunctions effects the status output (open collector, active high). An internally determined delay time applied to all malfunctions but overvoltage prevents the output of messages in case of short-term malfunctions. Furthermore, a temperature protection circuit prevents thermal overload. If overload occurs, the outputs are protected according to the safe operating area (SOA) mode (**see diagram**). If voltage and current are outside the SOA, the outputs oscillate to reduce the power dissipation. The switching frequency depends on the internal delay time and the external load (inductances and capacitances). If the frequency is low, the status output may follow the oscillation. An integrated reverse diode protects the supply voltage V_S against reverse polarities. Similarly the load circuit is protected against reverse polarities within the limits established by the maximum ratings (no shorted load at the same time!). At supply voltages below the operating range an undervoltage detector ensures that neither the status nor the outputs are activated. At supply voltages below the operating range the output stages are de-activated.

Status Output (H = Error)				
	Undervoltage > 3.5 V	**Operating Range**		**Overvoltage**
		V_I = L (passive)	V_I = H (active)	
Normal function	L	L	L	H
Overload	L	L	H	H
Open load	L	L	H	H
Shorted load to ground	L	H	H	H
Overtemperature	L	H	H	H



Circuit Diagram

Absolute Maximum Ratings

T_j = – 40 to 150 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Voltages				
Supply voltage, $t < 0.2$ s	V_S	–	70	V
Supply voltage	V_S	– 1.3	40	V
Input voltage	V_I	– 13	40	V
Output voltage (status output)	V_O	– 0.3	40	V
Output voltage (switching stages)	V_Q	– 0.3	+ V_S	V
Currents				
Output current (switching stages)	I_Q	internally limited	–	–
Current with reverse polarity, $t < 0.1$ s	I_Q	– 0.7	–	A
Output current positive clamp	I_Q	–	0.7	A
Ground current	I_{GND}	– 1.4	2.0	A
Output current (status output)	I_O	–	10	mA
Junction temperature	T_j	–	150	°C
Storage temperature	T_{stg}	– 50	150	°C
Operating Range				
Supply voltage	V_S	6 [1)]	25	V
Supply voltage slew rate	dV_S/dt	– 1	1	V/µs
Output current (switching stages)	I_Q	– 0.5	0.5	A
Input voltage	V_I, V_F	– 5	32	V
Output current (status output)	I_O	0	5	mA
Ambient temperature	T_A	– 40	125	°C

1) Lower limit = 5 V, if previously V_S greater than 6 V (turn-on hysteresis)

Absolute Maximum Ratings (cont'd)

T_j = – 40 to 150 °C

Parameter		Symbol	Limit Values		Unit
			min.	max.	
Supply voltage while shorted load	TLE 4214 TLE 4214 G	V_S V_S	– –	16 15	V V
Thermal resistance junction to ambient	TLE 4214 TLE 4214 G	$R_{th\ JA}$ $R_{th\ JA}$	– –	91 77	K/W K/W

Characteristics

V_S = 6 to 16 V (typ. V_S = 12 V); T_j = – 40 to 150 °C (typ. T_j = 25 °C)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
General Characteristics						
Quiescent current Supply voltage	I_S I_S	– –	2 35	4 50	mA mA	$V_F < V_{FL}$ $V_I = V_I > V_{IH}$, $V_F > V_{FH}$
Supply overvoltage shutdown threshold	V_{SO}	30	37	42	V	V_L = 5 V; V_O > 4.5 V
Hysteresis of supply overvoltage shutdown threshold	ΔV_{SO}	4	6	9	V	V_L = 5 V; V_O > 4.5 V
Open load error threshold voltage	V_Q	5	20	50	mV	V_L = 5 V; V_O > 4.5 V
Open load error threshold current	I_{QU}	1	–	40	mA	$V_Q = V_{QU}$
Open load error threshold current for both channels active	I_{QU}	–	–	80	mA	$V_{Q1} = V_{Q2} = V_{QU}$

Characteristics (cont'd)

V_S = 6 to 16 V (typ. V_S = 12 V); T_j = – 40 to 150 °C (typ. T_j = 25 °C)

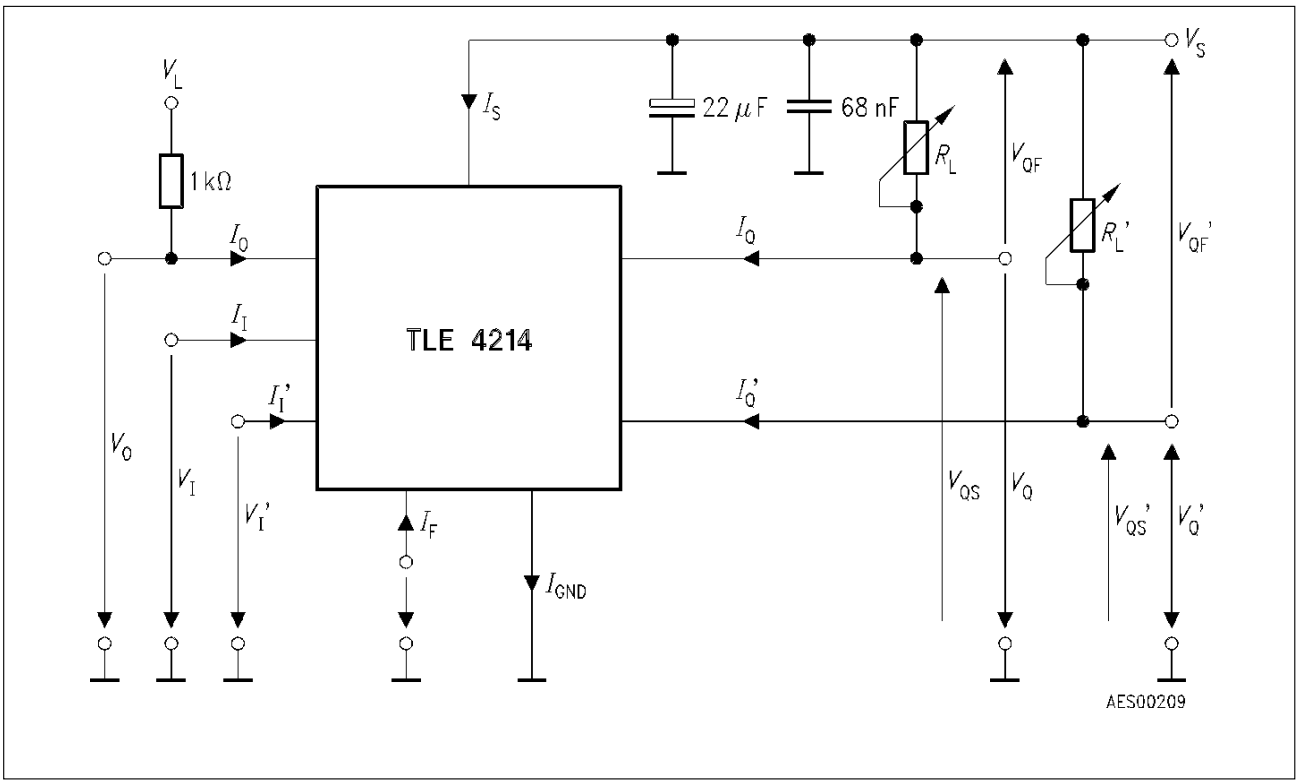
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Logic						
Control inputs						
H-input voltage threshold	V_{IH}	1.3	1.8	2.1	V	–
L-input voltage threshold	V_{IL}	0.9	1.2	1.5	V	–
Hysteresis of input voltage	ΔV_I	0.2	0.6	1.0	V	–
H-input voltage threshold	V_{FH}	1.6	2.1	2.7	V	–
L-input voltage threshold	V_{FL}	1.4	1.8	2.3	V	–
Hysteresis of input voltage	ΔV_F	0.1	0.3	0.7	V	–
H-input current	I_{IH}	0	–	10	µA	V_I = 5 V
L-input current	$-I_{IL}$	0	–	10	µA	V_I = 0.5 V
Status Output (open collector)						
L-saturation voltage	V_{QSat}	0.1	0.2	0.4	V	I_O = 5 mA
Status delay time	t_{dS}	8	20	32	µs	[1]

[1] Period from the beginning of the disturbance at one channel (exception: overvoltage) until the 50 % value of the status switching edge is reached.

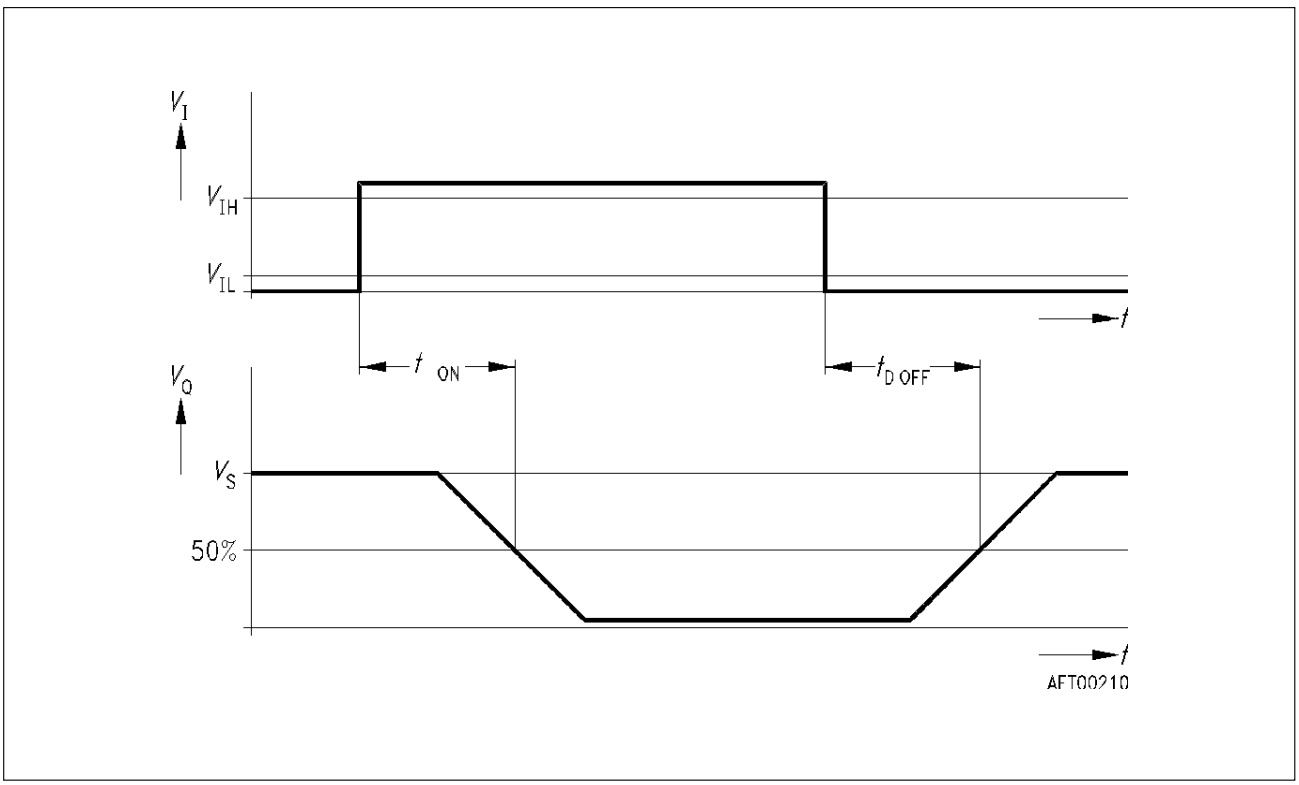
Characteristics (cont'd)

V_S = 6 to 16 V (typ. V_S = 12 V); T_j = – 40 to 150 °C (typ. T_j = 25 °C)

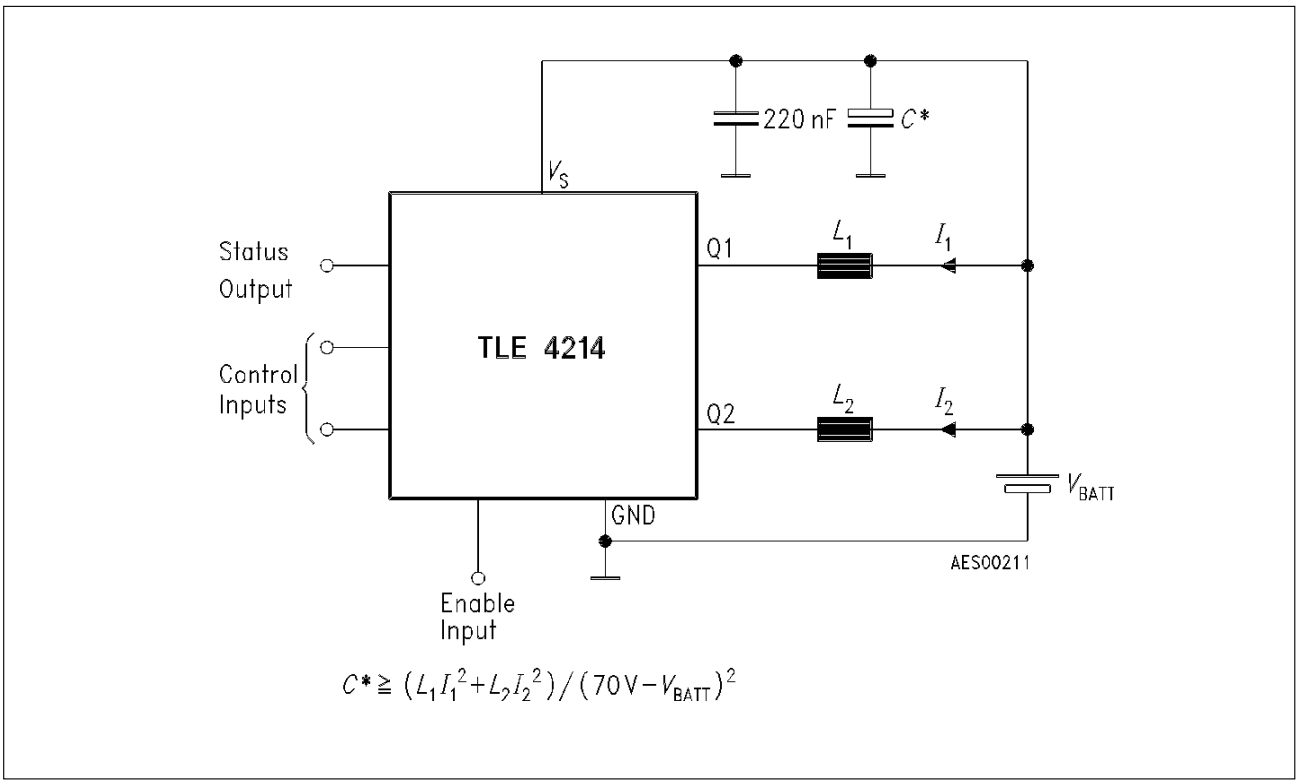
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Switching Stages						
Saturation voltage	V_{QSat}	–	0.6	0.8	V	I_Q = 0.5 A; $V_I > V_{IH}$; $V_F > V_{FH}$
Saturation voltage	V_{QSat}	–	45	100	mV	I_Q = 50 mA; $V_I > V_{IH}$; $V_F > V_{FH}$
Output current	I_Q	0.5	–		A	V_{QSat} = 0.8 V; $V_I > V_{IH}$
Leakage current	I_Q	– 5	–	50	µA	V_Q = 6 V; $V_I < V_{IL}$
Switch-ON time	$t_{D\ ON}$	0.2	0.5	5	µs	I_Q = 0.5 A **see Timing**
Switch-OFF time	$t_{D\ OFF}$	0.2	2	5	µs	I_Q = 0.5 A **Diagram**
Forward voltage of substrate diode	V_{QS}	–	1.3	1.7	V	I_Q = – 0.5 A t < 0.1 s
Forward voltage of clamp diode	V_{QF}	–	1.3	1.7	V	I_Q = 0.5 A t < 0.1 s
Leakage current of clamp diode	$-I_{QF}$	–	–	5	µA	V_Q = 0 V; $V_I < V_{IL}$



Test Circuit

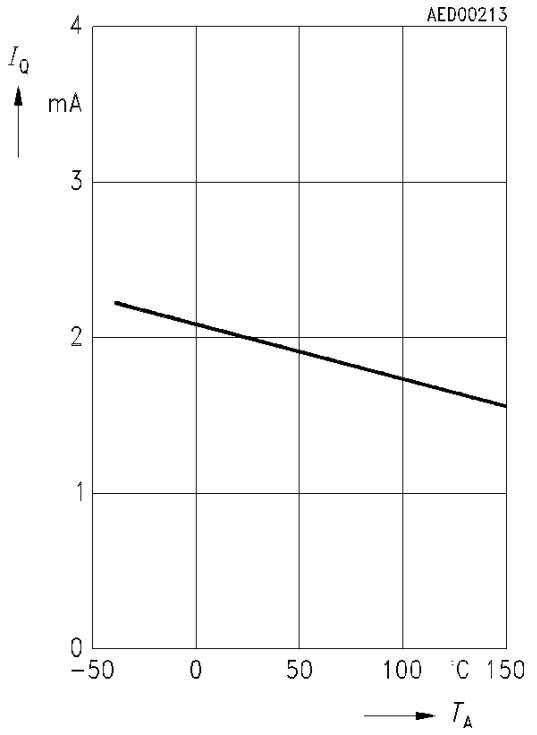


Timing Diagram

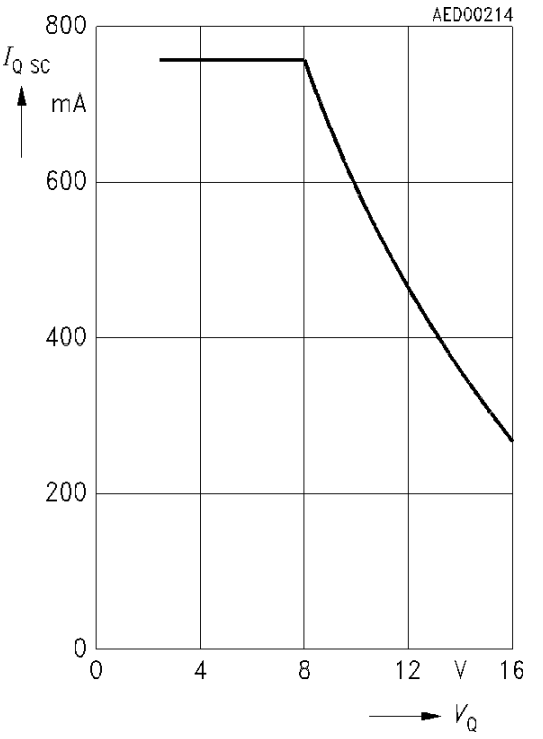


Application Circuit

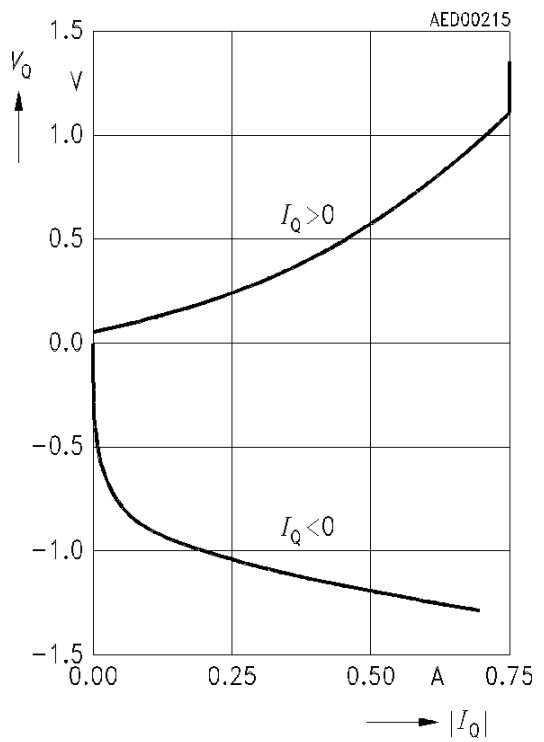
Quiescent Current I_S versus Ambient Temperature T_A in the OFF-Status
V_S = 12 V; $V_F < V_{FL}$



Shorted Load Current I_{Q0} versus Output Voltage V_Q



Output Voltage V_Q versus Output Current V_S = 12 V; $V_I > V_{IH}$



Maximum permissible output currents, being the result of the typical thermal power dissipation in a **P-DIP-8-1** package, for three operating modes.

ΔT: Difference between junction and ambient temperature ($T_j - T_A$) [K].

I_S: Max. output current (steady current) per channel.

SIEMENS

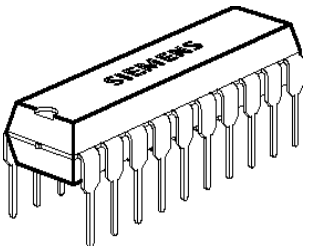
Intelligent Sixfold Low-Side Switch

TLE 4216

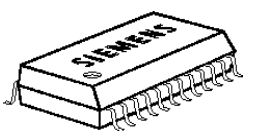
Bipolar IC

Features

- Double low-side switch, 2 x 0.5 A
- Quad low-side switch, 4 x 50 mA
- Power limitation
- Open-collector outputs
- Overtemperature shutdown
- Status monitoring
- Shorted-load protection
- Integrated clamp Z-Diodes
- Temperature range – 40 to 110 °C



P-DIP-20-3



P-DSO-24-3

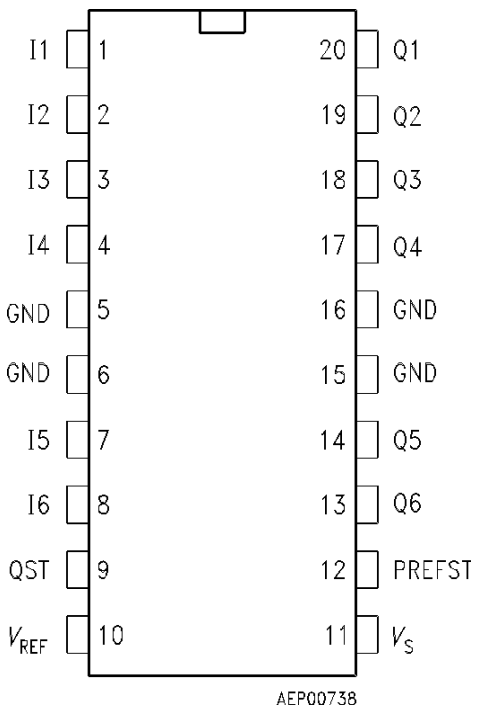
Type	Ordering Code	Package
TLE 4216	Q67000-A8237	P-DIP-20-3
▼ TLE 4216 G	Q67000-A9108	P-DSO-24-3 (SMD)

▼ New type

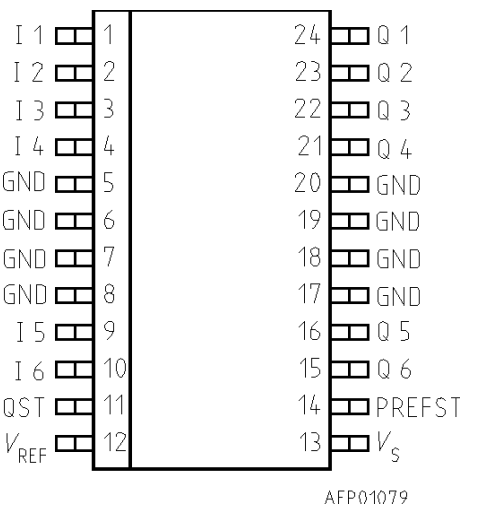
TLE 4216 is an integrated, sixfold low-side power switch with power limiting of the 0.5 A outputs, shorted load protection of the 50 mA switches and Z-diodes on all switches from output to ground. TLE 4216 is particularly suitable for automotive and industrial applications.

Pin Configuration
(top view)

TLE 4216

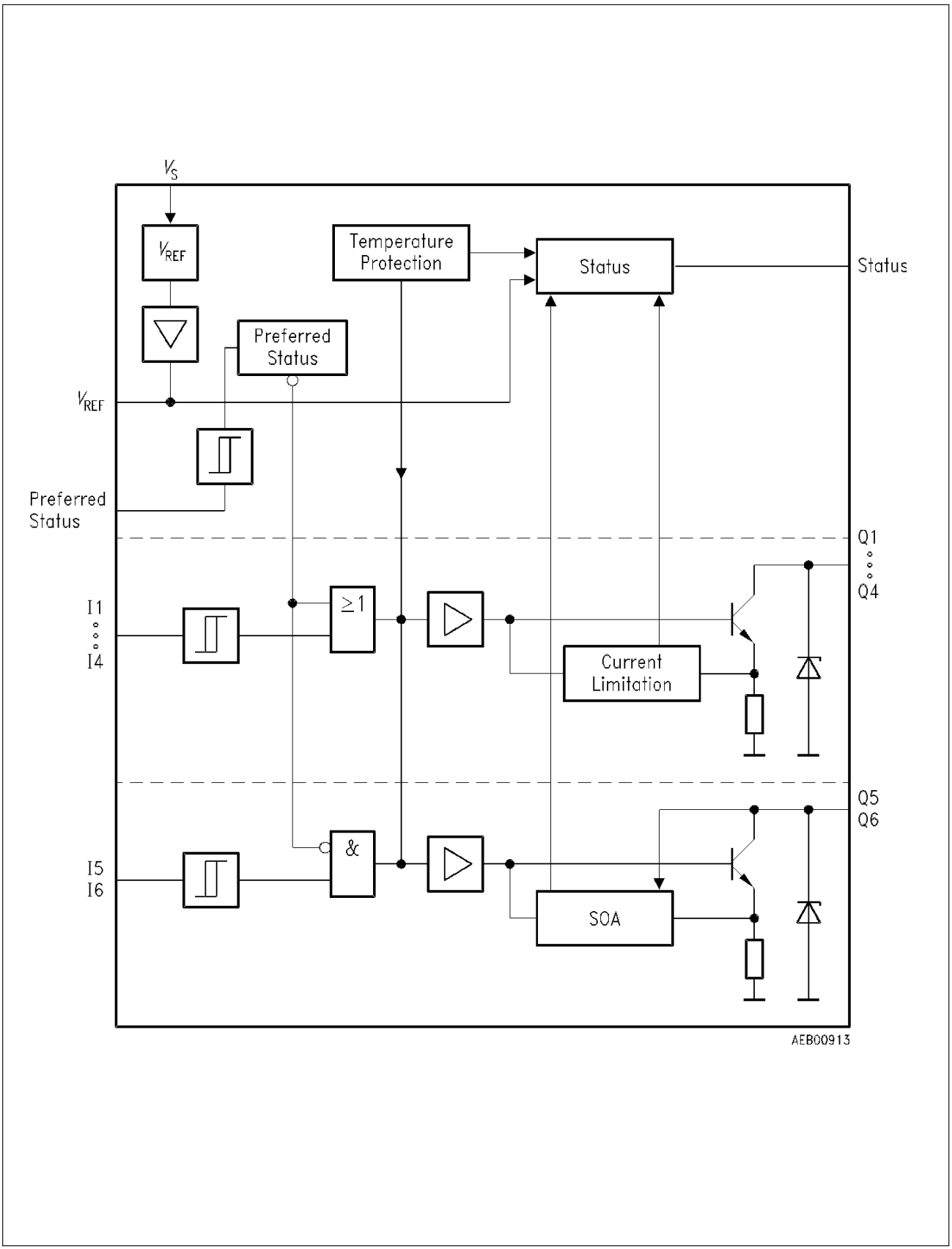


TLE 4216 G



Pin Definitions and Functions

TLE 4216 G	TLE 4216	Symbol	Function
Pin No.	**Pin No.**		
1, 2, 3, 4	1, 2, 3, 4	I1, I2, I3, I4	Inputs of 50-mA switches 1, 2, 3, 4
5, 6, 7, 8	5, 6	GND	Ground, cooling
9, 10	7, 8	I5, I6	Inputs of 0.5 A switches 5, 6
11	9	Q_{ST}	Status analog output
12	10	V_{REF}	Reference voltage; a higher reference voltage than the internal one can be applied from the exterior as a voltage reference for the status output (A/D converter).
13	11	V_S	Supply voltage
14	12	PREFST	Preferred state (low = preferred state of all outputs regardless of inputs)
15, 16	13,14	Q6, Q5	Outputs 6, 5 (0.5 A), open collector
17, 18, 19, 20	15, 16	GND	Ground, cooling
21, 22, 23, 24	17, 18, 19, 20	Q4, Q3, Q2, Q1	Outputs 4, 3, 2, 1 (50 mA), open collector



Block Diagram

Circuit Description

Input Circuits

The control inputs and the preferred-state input consist of TTL-compatible Schmitt triggers with hysteresis. Driven by these stages the buffer amplifiers convert the logic signal necessary for driving the NPN power transistors.

Switching Stages

The output stages consist of NPN power transistors with open collectors. Each stage has its own protective circuit for limiting power dissipation and shorted-load current, which makes the outputs shorted-load protected to the supply voltage throughout the operating range. Integrated Z-diodes limit positive voltage spikes that occur when inductive loads are discharged.

Monitoring and Protective Functions

Each output is monitored in its activated status for overload. Furthermore, large parts of the circuitry are shutdown (control, output stages). The information from these malfunctions is ORed and applied to the status output. If several malfunctions appear simultaneously, the highest voltage level will dominate. The IC is also protected against thermal overload. If a chip temperature of typically 160 °C is reached, overtemperature is signalled on the status output. If the temperature continues to increase, all outputs are turned off at 170 °C.

If the minimum supply voltage for functioning is not maintained, the output stages become inactive. At a supply voltage of 2 to 4 V, the outputs are switched to a preferred state regardless of the level on pin PREFST. If the preferred state is to be maintained beyond this range, pin PREFST must be switched to low potential. Above a supply voltage of typical 3 V (max. 4 V) the preferred state is controlled by pin PREFST. From 4 to 5.2 V the logic operation of the outputs is guaranteed, but the status output cannot be evaluated. At a supply voltage of 5.2 to 30 V the full function is guaranteed.

Application Description

Applications in automotive electronics require intelligent power switches activated by logic signals, which are shorted-load protected and provide error feedback.

The IC contains six power switches connected to ground (low-side switch). On inductive loads the integrated Z-diodes clamp the discharging voltage.

By means of TTL signals on the control inputs (active high) all six switches can be activated independently of another when a high level appears on the preferred-state input. When there is a low level on the preferred-state input, switches 1 to 4 are switched on, switches 5 and 6 are switched off regardless of the input level. The inputs are highly resistive and therefore must not be left unconnected, but should always be on fixed potential (noise immunity).

The status output signals the following malfunctions by analog voltage levels:

- Overload
- Overtemperature

Possible Input and Output Levels

Supply Voltage V_S	PREFST	I1 … I6	Q1 … Q4	Q5, Q6
2 to 4 V	L	X	L	H
4 to 30 V	H	L	H	H
4 to 30 V	H	H	L	L

Absolute Maximum Ratings

T_j = – 40 to 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Voltages					
Supply voltage	V_S	– 1	40	V	
Supply voltage, load circuit	V_{Q1-6}	– 0.7	25	V	
Input voltage	V_{I1-6}, V_{PREFST}	0	V_S	V	
Input voltage	$V_{REF\ ext}$	– 0.7	7	V	
Currents					
Switching current	I_{Q1}-I_{Q6}				limited internally
Current on reverse poling in load circuit	$I_{Q5, Q6}$	– 0.5		A	
Current on reverse poling in load circuit	I_{Q1-Q4}	– 50		mA	
Output current positive clamp	I_{Z5-Z6}		0.7	A	
Output current positive clamp	I_{Z1-Z4}		70	mA	
Junction temperature	T_j	– 40	150	°C	Thermal overload shutdown at 170 °C
Storage temperature	T_{stg}	– 50	150	°C	

Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	5.2	30	V	$V_{REF} \leq V_S$, functioning is guaranteed at V_S = 4 – 5.2 V but status output cannot be evaluated.
Supply voltage in load circuit	$V_{Q1\text{-}6}$	– 0.3	24	V	
Ambient temperature	T_A	– 40	110	°C	
Supply voltage for load short-circuit	V_S		16	V	
Input current (high)	I_{IH}		100	µA	
Thermal resistance Junction-ambient	$R_{th\ JA}$		65	K/W	P-DSO-24-3
Junction-ambient	$R_{th\ JA}$		55	K/W	P-DIP-20-3

Characteristics

V_S = 5 to 12 V; T_j = – 25 to 140 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
General						
Supply current	I_S		50	70	mA	$V_I > V_{IH}$; $V_{IP} > V_{IH}$
Supply current	I_S		36	50	mA	$V_I > V_{IH}$; $V_{IP} > V_{IH}$; V_S = 5 V
Quiescent current	I_S		8	11	mA	$V_I < V_{IL}$; $V_{IP} > V_{IH}$
Logic (Control inputs + preferred state)						
H-switching threshold	V_{IH}	1.3	1.8	2.1	V	
L-switching threshold	V_{IL}	0.9	1.2	1.5	V	
Hysteresis	ΔV_I	0.3	0.6	1.0	V	
Input current						
Input current	I_I	–2		2	µA	0.9 V < V_I < 6 V
L-input current	$-I_{IL}$	0		20	µA	0.5 V < V_I < 0.9 V
Switching Stages						
Load current	$I_{Q1\text{-}Q4}$	50			mA	V_S = 2 V (preferred state)
Saturation voltage	$V_{QSat\ 5,\ 6}$		0.5	0.8	V	I_Q = 0.4 A; $V_I > V_{IH}$
Saturation voltage	$V_{QSat\ 1\text{-}4}$		0.4	0.6	V	I_Q = 50 mA; $V_I > V_{IH}$
Saturation voltage	$V_{QSat\ 1\text{-}4}$			0.22	V	I_Q = 20 mA; $V_I > V_{IH}$
Turn-ON time	$t_{D\text{-}ON}$	0.2	1	1.5	µs	**see Diagrams**
Turn-OFF time	$t_{D\text{-}OFF}$	0.2	1	1.5	µs	**see Diagrams;** $I_L = I_{max}$

Characteristics (cont'd)

V_S = 5 to 12 V; T_j = – 25 to 140 °C

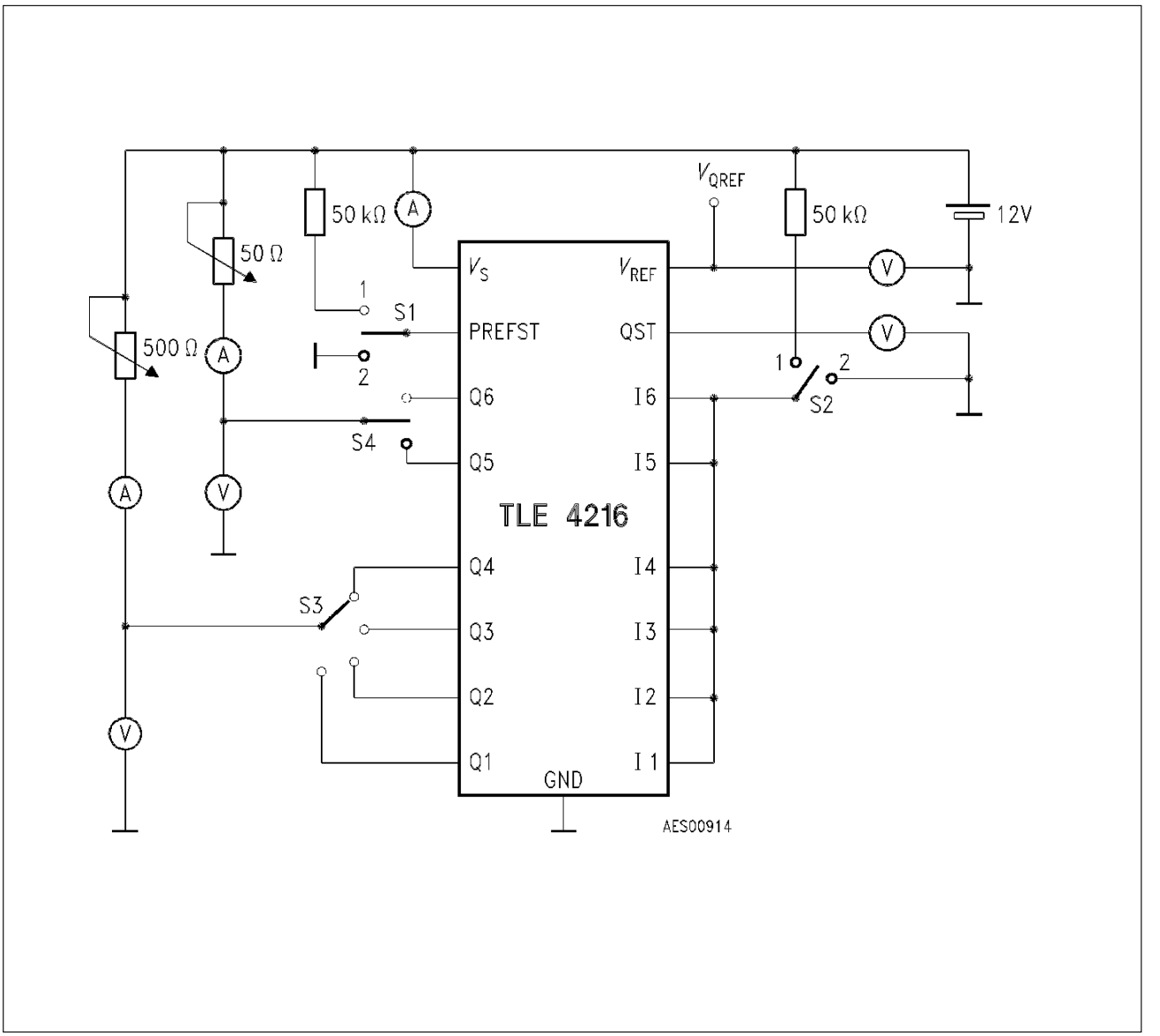
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Temperature Protection						
Overtemperature (signaled on status output)			160		°C	
Overtemperature (outputs shut down)			170		°C	
Outputs						
Output voltage pos. clamp	V_{Q1-4}	25.5		33	V	$I = 50$ mA
Output voltage pos. clamp	V_{Q5-6}	25.5		35	V	$I = 0.5$ A
Shorted-load current	$I_{Q1max-Q4max}$	50		120	mA	V_Q < 16 V
Leakage current	I_{Q1-4}			200	nA	V_Q = 24 V; T_j = 125 °C
Leakage current	$I_{Q5;6}$			300	µA	V_Q = 24 V
Shorted-load current	$I_{Q5max-Q6max}$					**see Diagrams**
Status output						
No error	V_{st}			0.5	V	V_{REF} = 5 V [1]
Overload output 6	V_{st}	1.0		1.3	V	V_{REF} = 5 V [1]
Overload output 5	V_{st}	1.4		1.7	V	V_{REF} = 5 V [1]
Overload output 4	V_{st}	1.8		2.1	V	V_{REF} = 5 V [1]
Overload output 3	V_{st}	2.2		2.5	V	V_{REF} = 5 V [1]
Overload output 2	V_{st}	2.6		2.9	V	V_{REF} = 5 V [1]
Overload output 1	V_{st}	3.0		3.3	V	V_{REF} = 5 V [1]
Overtemperature	V_{st}	3.5			V	V_{REF} = 5 V [1]

[1] The limits shift proportionally for a higher value of reference voltage.

Characteristics (cont'd)

V_S = 5 to 12 V; T_j = – 25 to 140 °C

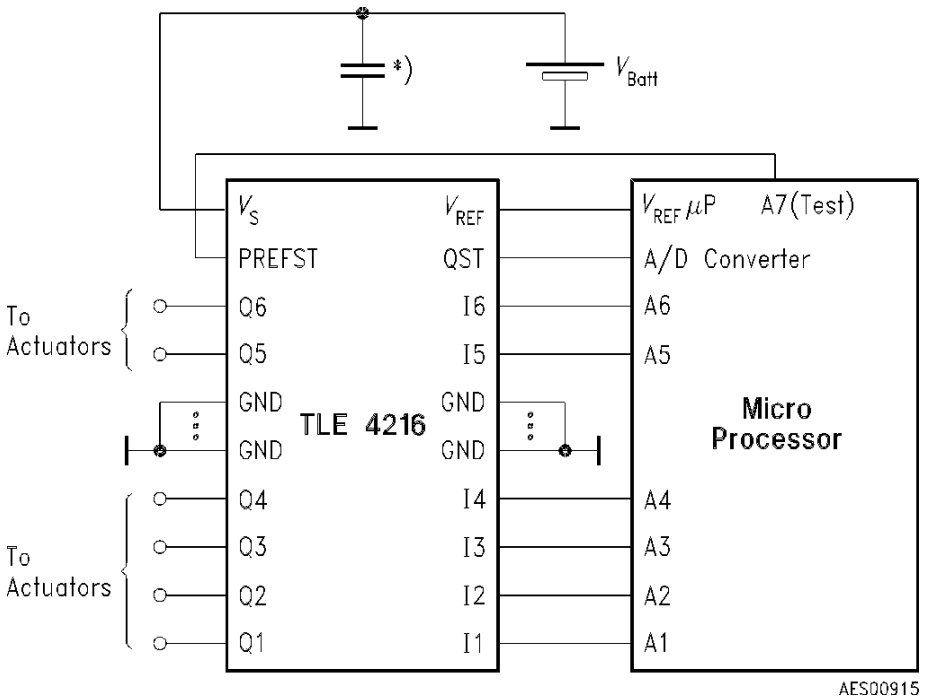
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Source resistance of status output	R_{QSt}	100		550	Ω	
Delay time of status	t_{dst}			10	µs	Shorted load
Reference voltage (internal)	V_{REF}		2.5		V	
Input resistance of reference pin	$R_{REF\ in}$	7	10	14.5	kΩ	V_{REF} = 2.8 V … 6.5 V



Test Circuit

S1 in position 1: all switches can be activated by S2 (position 1) or deactivated (position 2)

S1 in position 2: preferred state

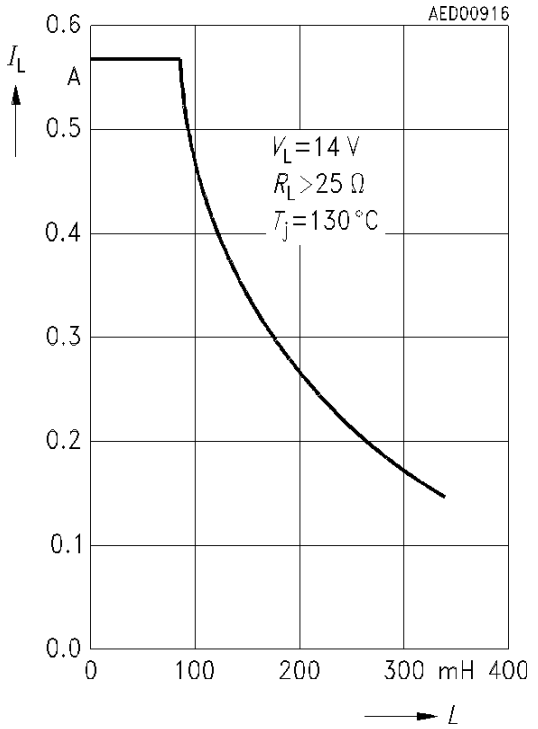


Application Circuit

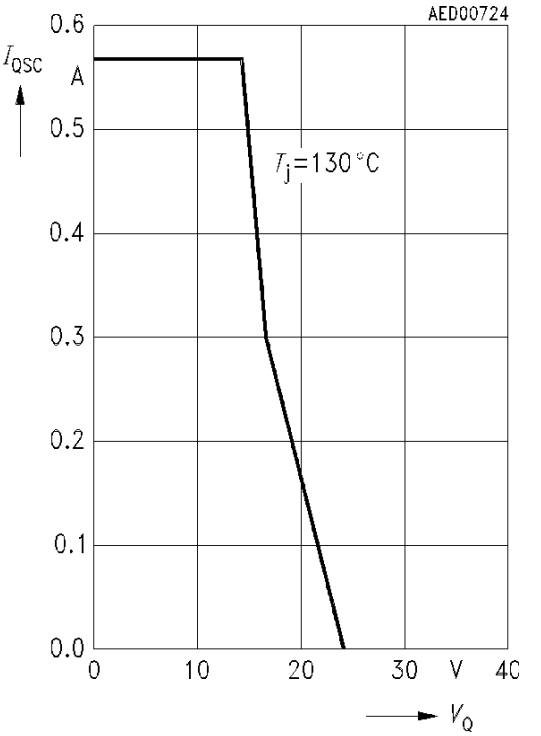
*) The capacitance depends on the inductance and current load of the supply.

Diagrams

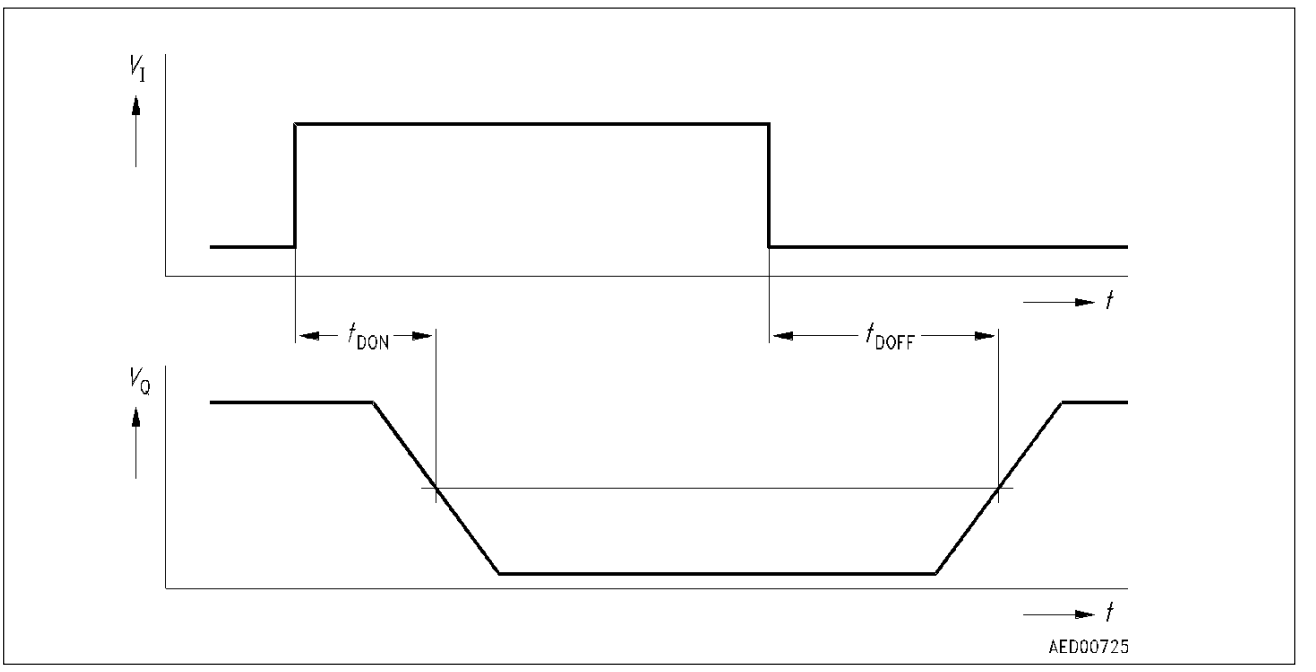
Permissible Load Inductance versus Load Current



Short-Circuit Current I_{QO} versus Output Voltage V_Q (0.5 A outputs)



When switching the maximum inductive loads, the maximum temperature T_j of 150 °C may be briefly exceeded. The IC will not be destroyed by this, but the restrictions concerning useful life should be observed.



SIEMENS

Intelligent 4-A Low-Side Switch

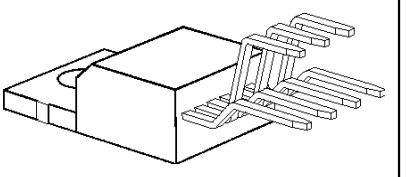
TLE 4224

Preliminary Data

SPT-IC

Features

- Single low-side switch, 4 A
- Low-ON-resistance (typ. 0.25 Ω)
- Power limitation
- Overtemperature shutdown
- Overload shutdown
- Reverse polarity protection
- Status monitoring
- Shorted-load protection
- Integrated clamp Z-diodes
- Temperature range – 40 to 110 °C



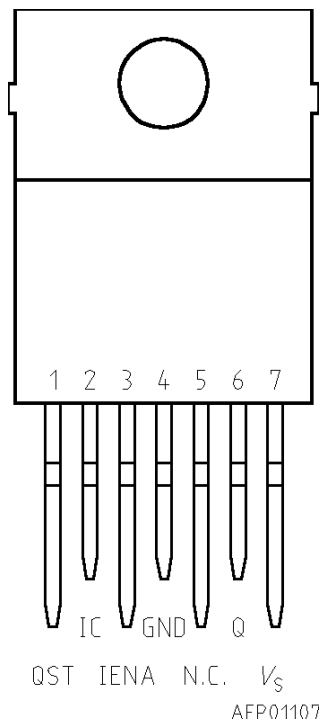
P-TO220-7-1

	Type	Ordering Code	Package
▼	TLE 4224	Q67000-A9062	P-TO220-7-1

▼ New type

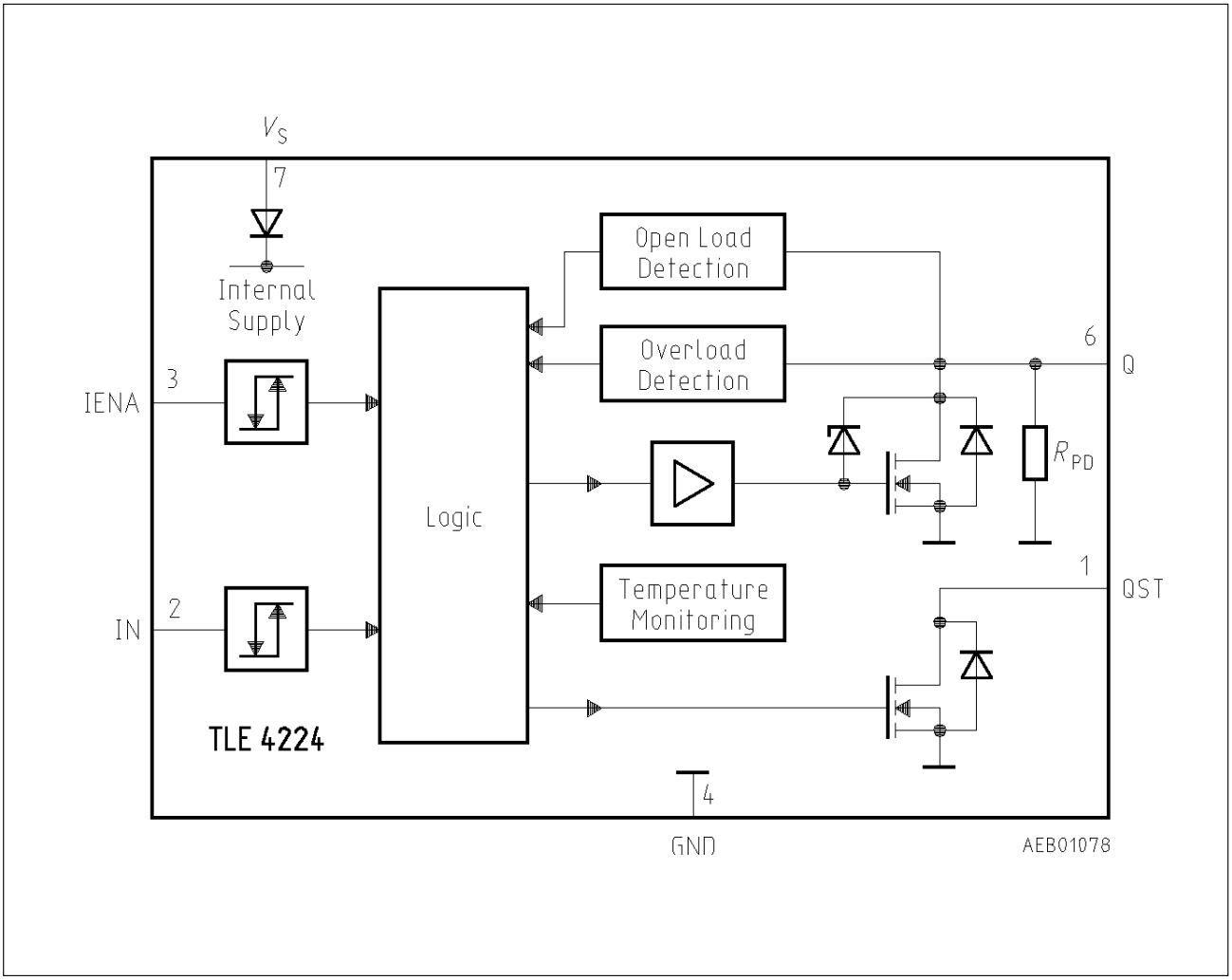
TLE 4224 is an integrated low-side power-switch with reverse-polarity protection, load interrupt and shorted-load detection, temperature monitoring, error signaling via a status output and an integrated Z-diode for output clamping. TLE 4224 is designed for automotive applications.

Pin Configuration
(top view)



Pin Definitions and Functions

Pin No.	Symbol	Function
1	QST	**Status output** (open collector) for error monitoring; shorted-load protected to $V_{ST} \leq 6.25$ V
2	IN	**Control input,** active high.
3	IENA	**Enable input,** active high.
4	GND	**Ground,** connected internally to cooling lug.
5	N.C.	Not connected
6	Q	**Power output** (open drain) for inductive loads; shorted-load protected.
7	V_S	**Supply voltage;** if there is overvoltage on this pin, the major part of the circuitry is shutdown.



Block Diagram

Application Description

This IC is specially designed to drive inductive loads (relays, electromagnetic valves). An integrated clamp diode limits output voltage when inductive loads are discharged. For the detection of errors there is a status output, which monitors the following errors by logic level:

- Thermal overload,
- Open and shorted load to ground in active and inactive mode,
- Overload (also shorted load to supply) in active mode.

Circuit Description

Input Circuits

The control and enable inputs, both active high, consist of Schmitt triggers with hysteresis. All inputs are connected with pull-down current sources. Unconnected inputs are intrepreted as “low”.

Switching Stages

The power output consists of a DMOS power transistor with open drain. The output stage is shorted-load-protected throughout the operating range. The integrated clamp-diode limits voltage spikes produced when inductive loads are discharged.

Protective Circuits

An integrated diode protects against reverse poling of the supply voltage within the operating range. The load circuit withstands reverse poling within the bounds of the maximum ratings (no shorted load permissible at the same time). A temperature protection guards the IC against thermal overload.

Error Detection

The status output signals the status of the switching stage at normal operation. (Low = OFF; high = ON). In case of any error the status output is set according to the table on the next page.

If current overload occurs, the error condition is stored in an internal register and the output is shut down. To reset this register the control input has to be switched off and then on again.

The status of the error detection circuit is directly dependent of the input state.

Status Monitoring

Operating Condition	Enable Input	Control Input	Power Output	Status Output
Normal Operation	LOW LOW HIGH HIGH	LOW HIGH LOW HIGH	OFF OFF OFF ON	LOW LOW LOW HIGH
Thermal Overload	RANDOM RANDOM	LOW HIGH	OFF OFF	HIGH LOW
Open Load or shorted Load to Ground	LOW LOW HIGH HIGH	LOW HIGH LOW HIGH	OFF OFF OFF ON	HIGH HIGH HIGH LOW
Overload or Shorted Load to V_S	LOW LOW HIGH HIGH	LOW HIGH LOW HIGH	OFF OFF OFF OFF	HIGH HIGH HIGH LOW

Absolute Maximum Ratings

T_A = – 40 to 125 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Voltages					
Supply voltage	V_S	– 15	60	V	–
Output voltage	V_Q	–	45	V	–
Output voltage	V_Q	–	60	V	$t \leq 500$ ms
Output voltage	V_{ST}	– 0.3	45	V	–
Input voltage	$V_{I,F}$	– 1.5	6	V	–

Absolute Maximum Ratings (cont'd)
T_A = – 40 to 125 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Currents					
Output current	I_Q	5	–	A	limited internally
Current on reverse poling	I_Q; I_{GND}	– 4	–	A	–
Output current, status pin	I_{ST}	– 5	5	mA	–
Discharging energy for inductive load	E	–	50	mJ	–
Junction temperature Junction temperature	T_j T_j	– 40	150 175	°C °C	 during clamping
Storage temperature	T_{stg}	– 50	150	°C	–
Operating Range					
Supply voltage	V_S	5.5	45	V	–
Supply voltage slew rate	dV_S/dt	– 1	1	V/µs	–
Output voltage	V_Q V_Q	– 0.3 –	45 60	V V	– during clamping
Output voltage	V_{ST}	– 0.3	45	V	–
Output current	I_{ST}	0	2	mA	–
Ambient temperature	T_A	– 40	125	°C	$T_j \leq 150$ °C
Thermal resistance junction to case junction to ambient	 $R_{th\ JC}$ $R_{th\ JA}$	 – –	 3 65	 K/W K/W	 – –

Characteristics

V_S = 6.5 to 18 V (typ. 12 V)
T_A = – 40 to 125 °C; $T_j \leq$ 150 °C (typ. 25 °C)
V_D = 5.1 V

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Quiescent current	I_S	–	0.3	1	mA	Output OFF
Supply current	I_S	–	2	5	mA	Output ON
Open load current	I_{Qu}	–	–	250	mA	–
Open load shutdown voltage threshold	V_{Qu}	6	–	7.2	V	Output ON V_S = 12 V
Overload shutdown current threshold	I_{QAB}	5 4	– –	– –	A A	T_j = – 40 to 50 °C T_j = 50 to 150 °C
Overtemperature shutdown threshold	T_{AB}	145	–	175	°C	only a design value
Overtemperature shutdown hysteresis	ΔT_{AB}	–	10	–	°C	only a design value

Control and Enable Input

H-input voltage	V_{IH}	2.0	–	6.0	V	–
L-input voltage	V_{IL}	– 0.3	–	1.0	V	–
Hysteresis	ΔV_I	0.2	–	–	V	–
H-input current	I_{IH}	50	100	140	µA	V_I = 5 V
H-input current	I_{FH}	5	15	20	µA	V_F = 5 V

Status Output

Low voltage level	V_{ST}	–	–	0.5	V	I_{ST} = 2 mA
Leakage current high	I_{ST}	–	–	2	µA	V_S = 0 V

Characteristics (cont'd)

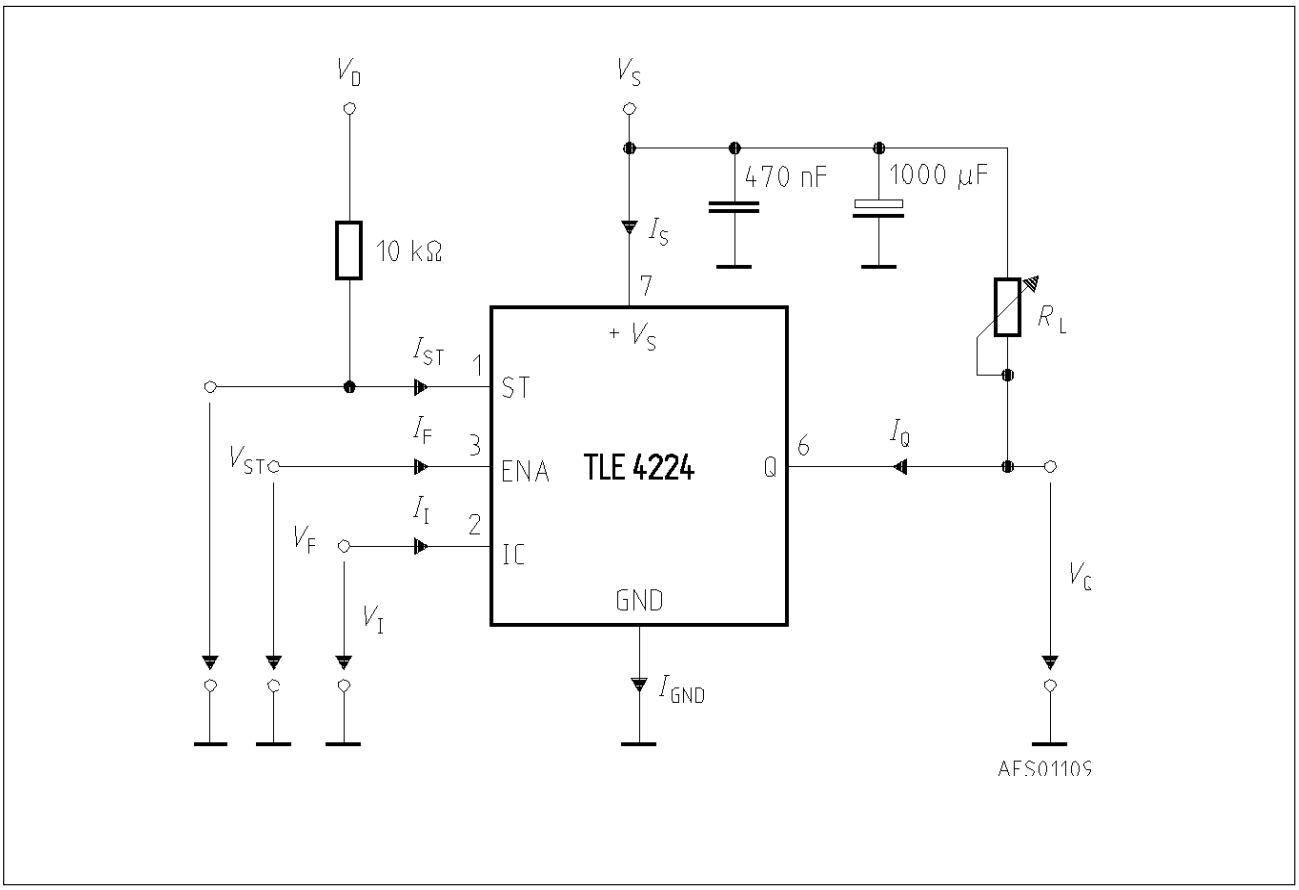
V_S = 6.5 to 18 V (typ. 12 V)

T_A = – 40 to 125 °C; $T_j \leq$ 150 °C (typ. 25 °C)

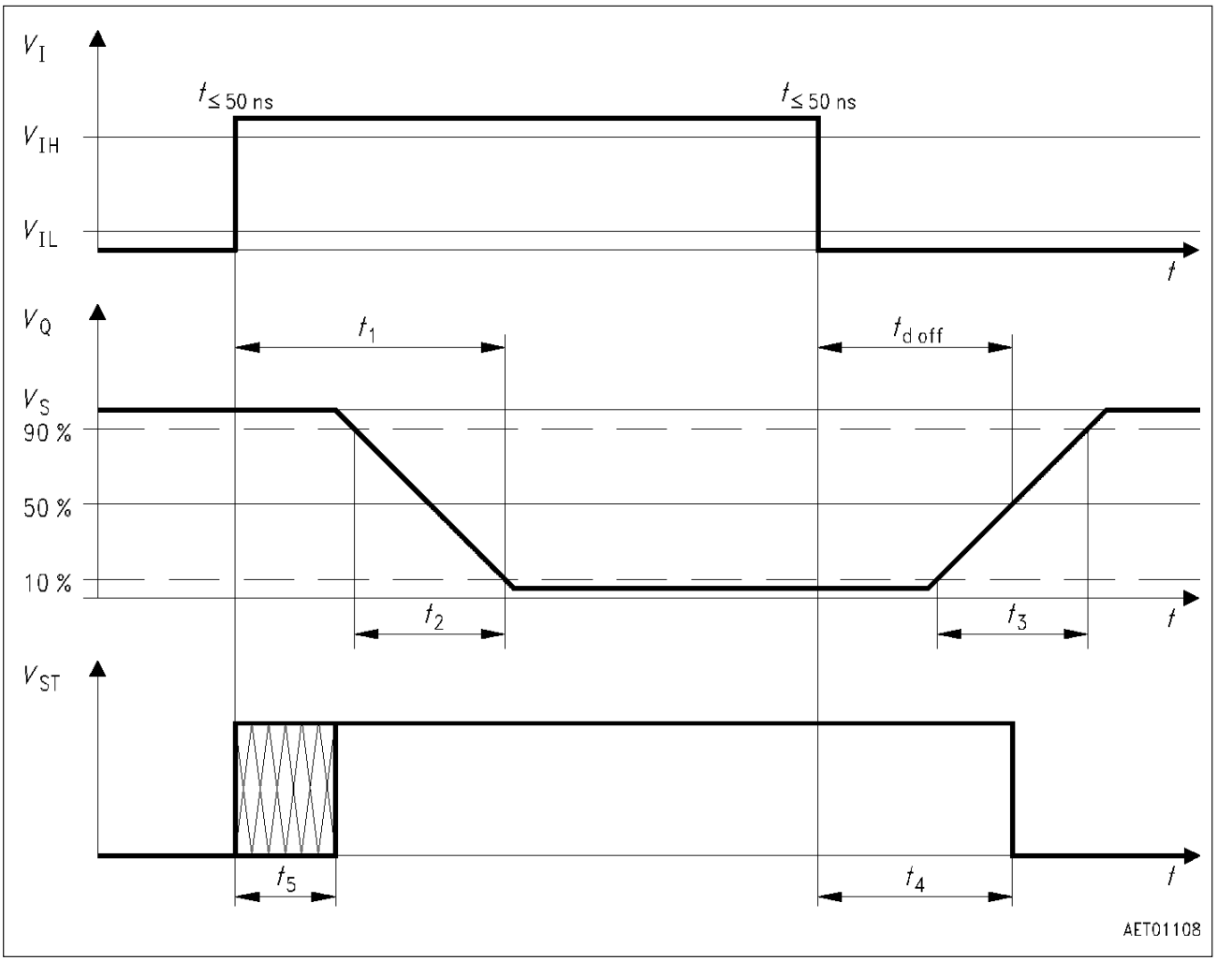
V_D = 5.1 V

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Power Output						
Static drain source ON-resistance	R_{DSON} R_{DSON}	– –	0.25 –	– 0.5	Ω Ω	$T_j \leq$ 25 °C T_j = 150 °C I_Q = 4 A, $V_S \geq$ 9.5 V
Pull-down resistance	R_{PD}	14	20	26	kΩ	T_j = 25 °C
Output ON delay time Output ON fall time Output OFF rise time Output OFF status delay Output ON status delay	t_1 t_2 t_3 t_4 t_5	– – – – –	25 20 25 30 –	– – – – 50	µs µs µs µs µs	I_Q = 0.2 A I_Q = 0.2 A I_Q = 2 A I_Q = 2 A 1)
Overload OFF delay time	t_{DSO}	50	–	150	µs	design value only
Clamp Diode						
Clamp diode clamping voltage	V_{QZ}	45	–	60	V	–

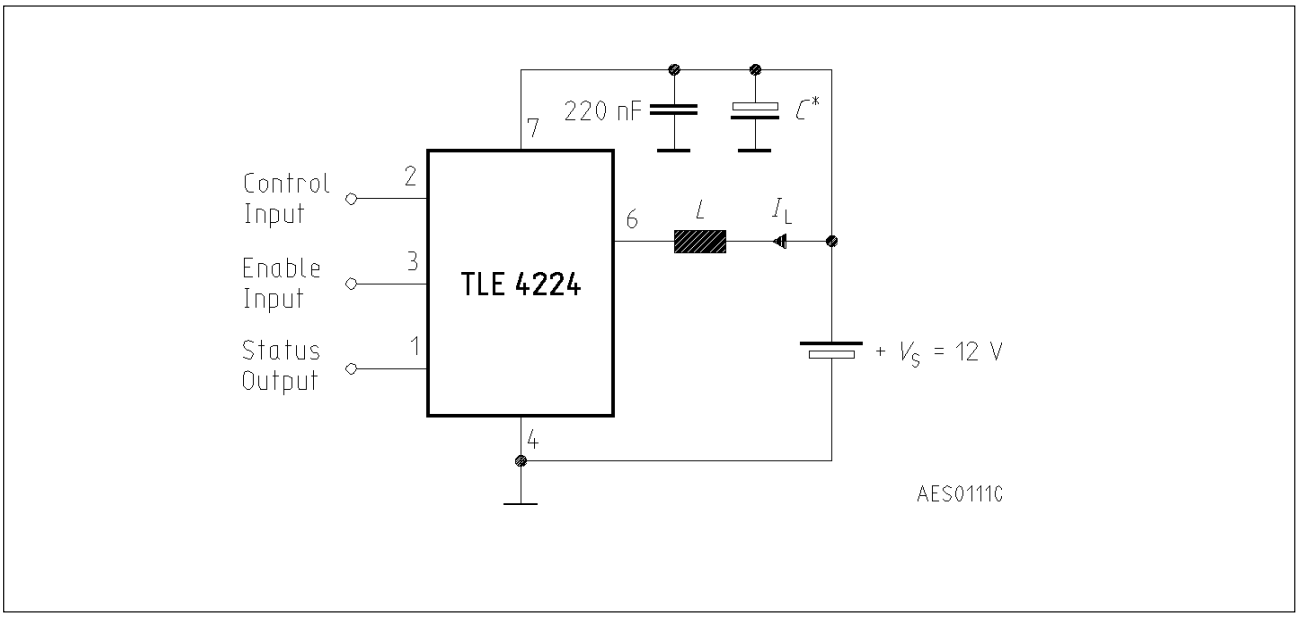
1) Time between status valid and switching on or error detection



Test Circuit



Timing Diagram



Application Circuit