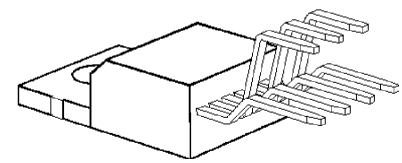
SIEMENS

Intelligent 4-A Low-Side Switch — TLE 4224

Preliminary Data — **SPT-IC**

Features

- Single low-side switch, 4 A
- Low-ON-resistance (typ. 0.25 Ω)
- Power limitation
- Overtemperature shutdown
- Overload shutdown
- Reverse polarity protection
- Status monitoring
- Shorted-load protection
- Integrated clamp Z-diodes
- Temperature range – 40 to 110 °C



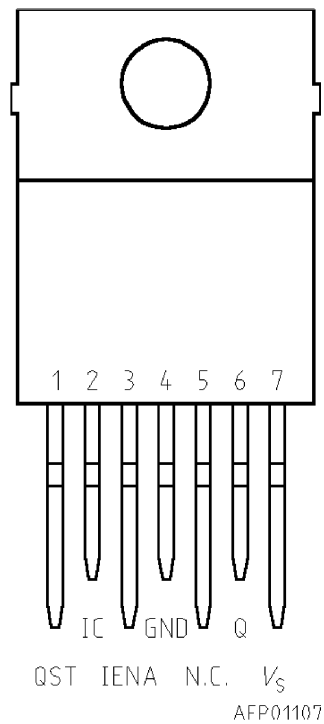
P-TO220-7-1

	Type	Ordering Code	Package
▼	TLE 4224	Q67000-A9062	P-TO220-7-1

▼ New type

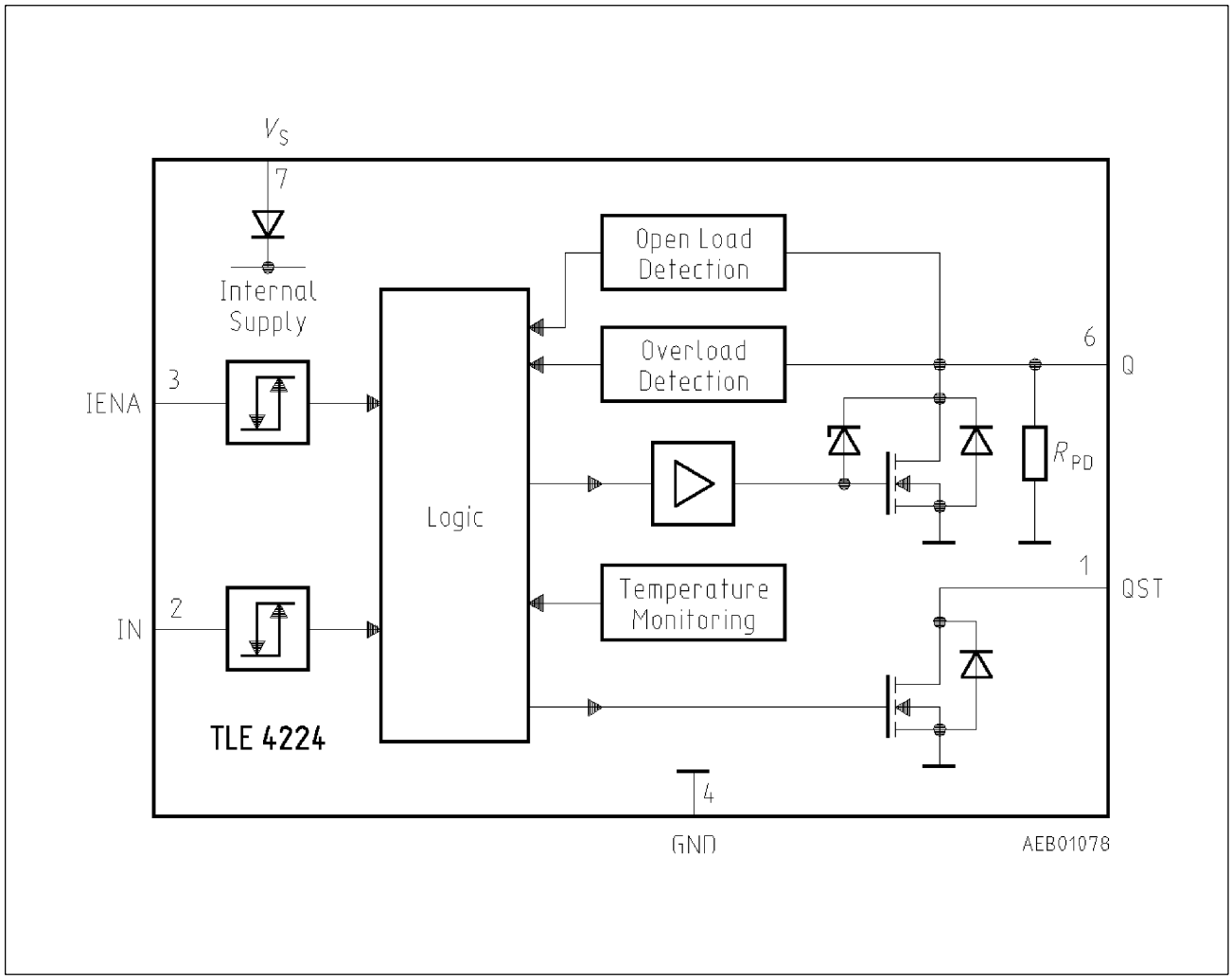
TLE 4224 is an integrated low-side power-switch with reverse-polarity protection, load interrupt and shorted-load detection, temperature monitoring, error signaling via a status output and an integrated Z-diode for output clamping. TLE 4224 is designed for automotive applications.

Pin Configuration
(top view)



Pin Definitions and Functions

Pin No.	Symbol	Function
1	QST	**Status output** (open collector) for error monitoring; shorted-load protected to $V_{ST} \leq 6.25$ V
2	IN	**Control input,** active high.
3	IENA	**Enable input,** active high.
4	GND	**Ground,** connected internally to cooling lug.
5	N.C.	Not connected
6	Q	**Power output** (open drain) for inductive loads; shorted-load protected.
7	V_S	**Supply voltage;** if there is overvoltage on this pin, the major part of the circuitry is shutdown.



Block Diagram

Application Description

This IC is specially designed to drive inductive loads (relays, electromagnetic valves). An integrated clamp diode limits output voltage when inductive loads are discharged. For the detection of errors there is a status output, which monitors the following errors by logic level:

- Thermal overload,
- Open and shorted load to ground in active and inactive mode,
- Overload (also shorted load to supply) in active mode.

Circuit Description

Input Circuits

The control and enable inputs, both active high, consist of Schmitt triggers with hysteresis. All inputs are connected with pull-down current sources. Unconnected inputs are intrepreted as “low”.

Switching Stages

The power output consists of a DMOS power transistor with open drain. The output stage is shorted-load-protected throughout the operating range. The integrated clamp-diode limits voltage spikes produced when inductive loads are discharged.

Protective Circuits

An integrated diode protects against reverse poling of the supply voltage within the operating range. The load circuit withstands reverse poling within the bounds of the maximum ratings (no shorted load permissible at the same time). A temperature protection guards the IC against thermal overload.

Error Detection

The status output signals the status of the switching stage at normal operation. (Low = OFF; high = ON). In case of any error the status output is set according to the table on the next page.

If current overload occurs, the error condition is stored in an internal register and the output is shut down. To reset this register the control input has to be switched off and then on again.

The status of the error detection circuit is directly dependent of the input state.

Status Monitoring

Operating Condition	Enable Input	Control Input	Power Output	Status Output
Normal Operation	LOW LOW HIGH HIGH	LOW HIGH LOW HIGH	OFF OFF OFF ON	LOW LOW LOW HIGH
Thermal Overload	RANDOM RANDOM	LOW HIGH	OFF OFF	HIGH LOW
Open Load or shorted Load to Ground	LOW LOW HIGH HIGH	LOW HIGH LOW HIGH	OFF OFF OFF ON	HIGH HIGH HIGH LOW
Overload or Shorted Load to V_S	LOW LOW HIGH HIGH	LOW HIGH LOW HIGH	OFF OFF OFF OFF	HIGH HIGH HIGH LOW

Absolute Maximum Ratings

T_A = – 40 to 125 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Voltages					
Supply voltage	V_S	– 15	60	V	–
Output voltage	V_Q	–	45	V	–
Output voltage	V_Q	–	60	V	$t \leq 500$ ms
Output voltage	V_{ST}	– 0.3	45	V	–
Input voltage	$V_{I,F}$	– 1.5	6	V	–

Absolute Maximum Ratings (cont'd)
T_A = – 40 to 125 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Currents					
Output current	I_Q	5	–	A	limited internally
Current on reverse poling	I_Q; I_{GND}	– 4	–	A	–
Output current, status pin	I_{ST}	– 5	5	mA	–
Discharging energy for inductive load	E	–	50	mJ	–
Junction temperature Junction temperature	T_j T_j	– 40	150 175	°C °C	 during clamping
Storage temperature	T_{stg}	– 50	150	°C	–
Operating Range					
Supply voltage	V_S	5.5	45	V	–
Supply voltage slew rate	dV_S/dt	– 1	1	V/µs	–
Output voltage	V_Q V_Q	– 0.3 –	45 60	V V	– during clamping
Output voltage	V_{ST}	– 0.3	45	V	–
Output current	I_{ST}	0	2	mA	–
Ambient temperature	T_A	– 40	125	°C	$T_j \leq 150$ °C
Thermal resistance junction to case junction to ambient	 $R_{th\ JC}$ $R_{th\ JA}$	 – –	 3 65	 K/W K/W	 – –

Characteristics

V_S = 6.5 to 18 V (typ. 12 V)
T_A = – 40 to 125 °C; $T_j \leq$ 150 °C (typ. 25 °C)
V_D = 5.1 V

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Quiescent current	I_S	–	0.3	1	mA	Output OFF
Supply current	I_S	–	2	5	mA	Output ON
Open load current	I_{Qu}	–	–	250	mA	–
Open load shutdown voltage threshold	V_{Qu}	6	–	7.2	V	Output ON V_S = 12 V
Overload shutdown current threshold	I_{QAB}	5 4	– –	– –	A A	T_j = – 40 to 50 °C T_j = 50 to 150 °C
Overtemperature shutdown threshold	T_{AB}	145	–	175	°C	only a design value
Overtemperature shutdown hysteresis	ΔT_{AB}	–	10	–	°C	only a design value

Control and Enable Input

H-input voltage	V_{IH}	2.0	–	6.0	V	–
L-input voltage	V_{IL}	– 0.3	–	1.0	V	–
Hysteresis	ΔV_I	0.2	–	–	V	–
H-input current	I_{IH}	50	100	140	µA	V_I = 5 V
H-input current	I_{FH}	5	15	20	µA	V_F = 5 V

Status Output

Low voltage level	V_{ST}	–	–	0.5	V	I_{ST} = 2 mA
Leakage current high	I_{ST}	–	–	2	µA	V_S = 0 V

Characteristics (cont'd)

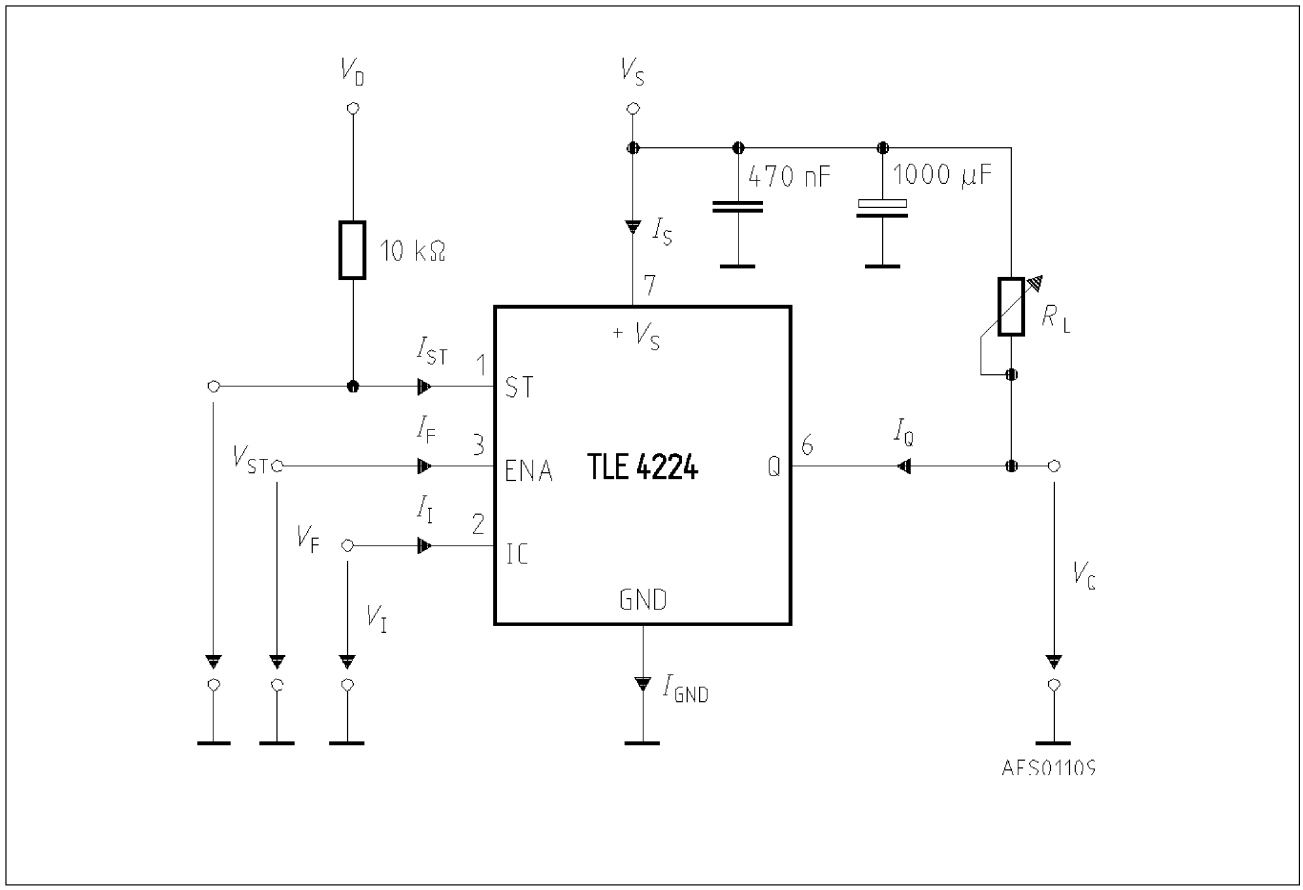
V_S = 6.5 to 18 V (typ. 12 V)

T_A = – 40 to 125 °C; $T_j \leq$ 150 °C (typ. 25 °C)

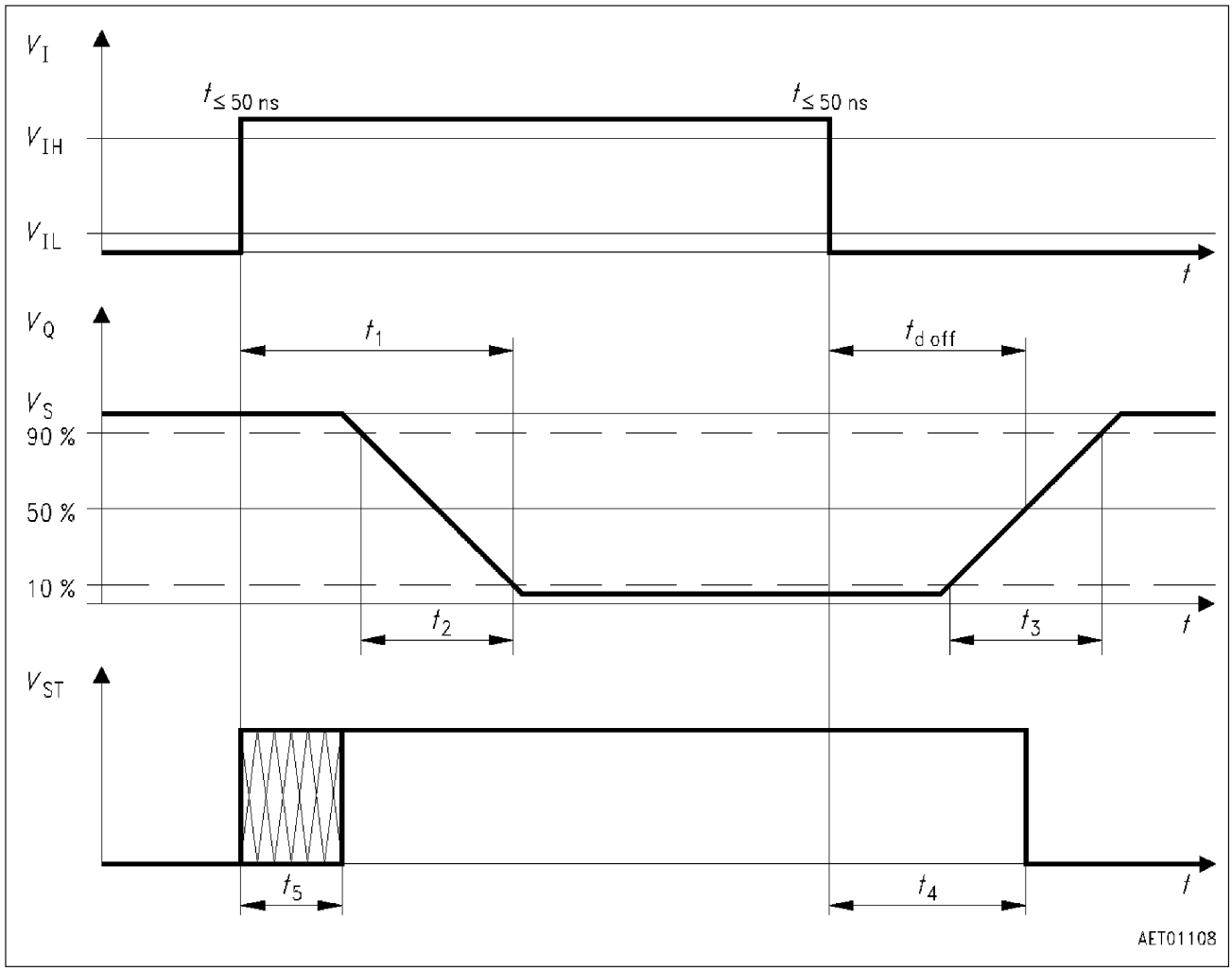
V_D = 5.1 V

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Power Output						
Static drain source ON-resistance	R_{DSON} R_{DSON}	– –	0.25 –	– 0.5	Ω Ω	$T_j \leq$ 25 °C T_j = 150 °C I_Q = 4 A, $V_S \geq$ 9.5 V
Pull-down resistance	R_{PD}	14	20	26	kΩ	T_j = 25 °C
Output ON delay time Output ON fall time Output OFF rise time Output OFF status delay Output ON status delay	t_1 t_2 t_3 t_4 t_5	– – – – –	25 20 25 30 –	– – – – 50	µs µs µs µs µs	I_Q = 0.2 A I_Q = 0.2 A I_Q = 2 A I_Q = 2 A 1)
Overload OFF delay time	t_{DSO}	50	–	150	µs	design value only
Clamp Diode						
Clamp diode clamping voltage	V_{QZ}	45	–	60	V	–

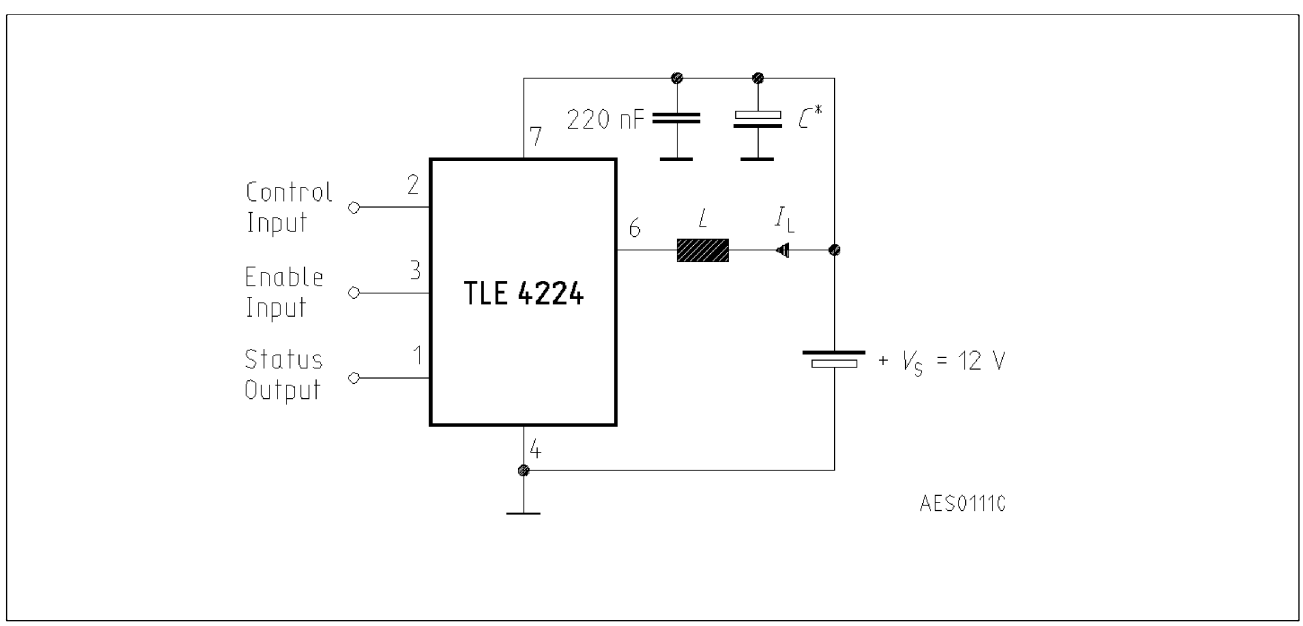
1) Time between status valid and switching on or error detection



Test Circuit



Timing Diagram



Application Circuit