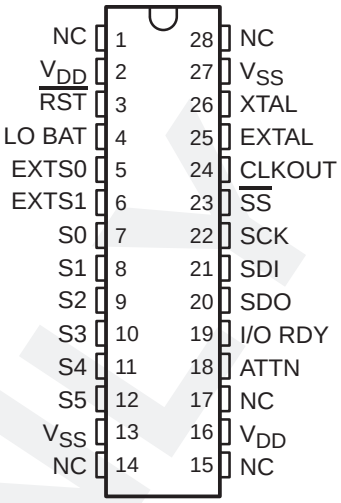
SLWS024– AUGUST 1995

- **FLEX™ Paging Protocol Signal Processor**
- **FLEX Roaming, Fragmentation, and Group Messaging Support**
- **FLEX Time-of-Day Stamping Support**
- **16 Address Words support any Combination of Long (2 Word) and Short (1 Word) Addresses**
- **16 Temporary Address Words Support Group Messaging**
- **1600, 3200, and 6400 Bits per Second Decoding**
- **Any Phase (1, 2, and 4) Decoding**
- **Serial Peripheral Interface Security Circuit Deters Unauthorized Reconfigurations**
- **2.0 Volt to 3.3 Volt Operation**
- **Allows Low Current STOP Mode Operation of Host Processor**
- **Uses standard Serial Peripheral Interface (SPI) in Slave Mode**
- **32-bit Packets for Bidirectional Communications over the Serial Peripheral Interface**
- **Universal Receiver Control Supports many RF Integrated Circuits**
- **Programmable Low Battery Monitoring**

**DW PACKAGE**
**(TOP VIEW)**




PRODUCT PREVIEW

## description

The TLV5591 signal processor is a FLEX™ signal processor that takes full advantage of the Motorola® FLEX paging protocol. This low-current device operates at synchronous data rates of 1600, 3200, and 6400 bits per second (bps) using a 76.8 kHz oscillator. This device is readily integrated with standard off-the-shelf electronic pager components thereby reducing start-up costs associated with pager manufacturing. An industry standard serial peripheral interface (SPI) transports simultaneous bidirectional 32-bit data packets between the TLV5591 and the host processor.

As a FLEX protocol decoder, the internal TLV5591 receiver control component makes use of 6-stage warm-up, 2-stage locking, and 3-stage warm-down sequences. This control information is passed to the receiver using six programmable data output lines. Warm-up control allows testing of battery condition, setting output line state, RF receiver power-on time, and other elements of a pager. The 2-stage locking sequence handles requirements associated with received FLEX signal baud rate changes. The warm-down control sets the program selectable time period when signal processing is complete, and the receiver can power-off. Battery condition can be checked, and the output line state can be changed under warm down control.



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POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
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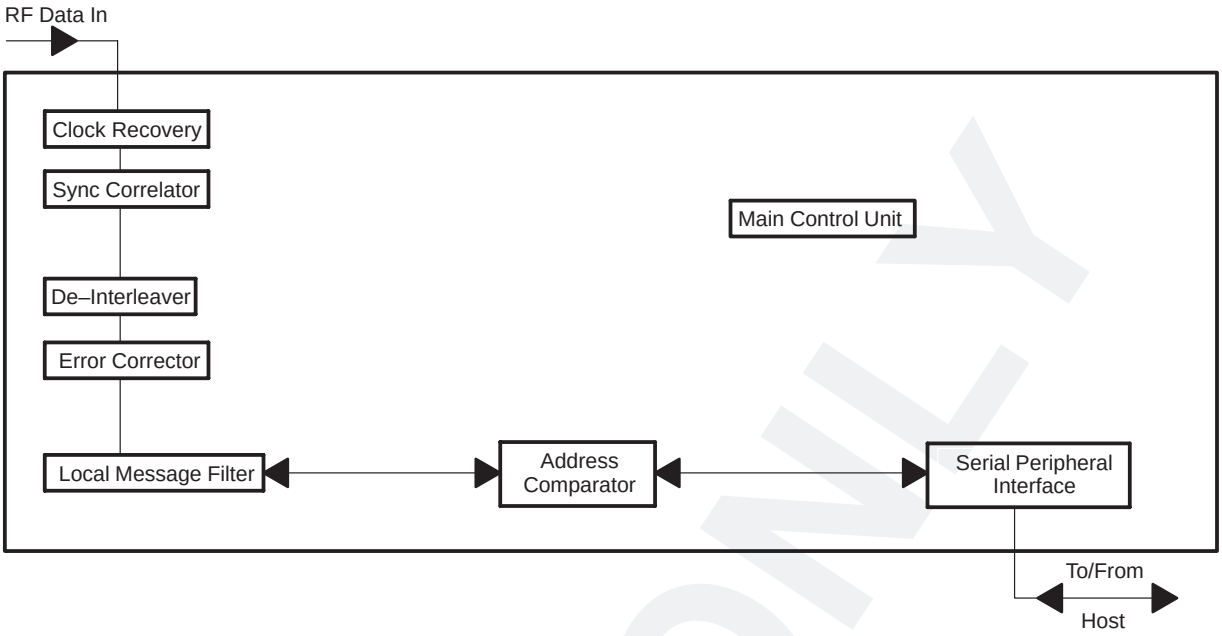
## functional block diagram




### main control unit

The main control unit (MCU) coordinates the functional blocks contained within the TLV5591 signal processor. Additional functions include controlling the receiver operational sequence and SPI timing associated with the host-to-TLV5591 signal processor interface.

### clock recovery

This functional block synchronizes FLEX protocol symbols. The centers of the symbols are returned for sampling. The clock also detects the validity of symbol baud rate.

### sync correlator

The sync correlator acquires and maintains synchronization to FLEX signals.

### de-interleaver

The de-interleaver disassembles the interleaved data blocks before sending to the appropriate registers. This process is a function of the data rates of 1600, 3200, and 6400 bits per second.

### error corrector

The error corrector performs variable bit-error correction on the de-interleaved 32,21,2 BCH FLEX code words.

### local message filter

The local message filter determines which FLEX code words to send to the host processor. The code words are filtered and placed into packets prior to sending.

### address comparator

This functional block checks each received FLEX code word for addresses corresponding to the 16 possible TLV5591 signal processor addresses and 16 temporary addresses.

### serial peripherial interface (SPI)

The SPI operates in the slave mode and handles all data sent between the TLV5591 signal processor and the host microprocessor.

**Terminal Functions**

| TERMINAL | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| ATTN | 18 | I | Used by the host to request communications with the TLV5591 signal processor. |
| CLKOUT | 24 | O | Clock Output (38.4 Hz)—May be used to clock a companion audio-to- data IC having a dual-bandwidth switched-capacitor filter designed for FLEX 4-level symbols. It may also be used to clock other functions of the pager circuitry. |
| EXTAL | 25 | I | Crystal oscillator input. |
| XTAL | 26 | O | Crystal oscillator output. |
| EXTS0 | 5 | I | EXTS0 and EXTS1 pair carries digitized FLEX 4-level symbols. |
| EXTS1 | 6 | | |
| I/O RDY | 19 | O | Used to indicate the TLV5591 signal processor is ready for communication with the host. |
| LO BAT | 4 | I | Used to test a low battery voltage input signal. |
| NC | 1, 14, 15, 17, 28 | | No internal connection. |
| RST | 3 | I | Used to reset the TLV5591 signal processor. |
| SCK | 22 | I | Serial Clock—Used to clock synchronous data on the SPI. |
| SDI | 21 | I | Serial Data Input—Carries data sent to the TLV5591 signal processor from the host on the SPI. |
| SDO | 20 | O | Serial Data Output—Carries data sent from the TLV5591 signal processor to the host on the SPI. |
| SS | 23 | I | Slave Select—Used to select the TLV5591 signal processor's SPI for data transfer. |
| S0 | 7 | O | Control lines for RF receiver functions. |
| S1 | 8 | | |
| S2 | 9 | | |
| S3 | 10 | | |
| S4 | 11 | | |
| S5 | 12 | | |
| VDD | 2, 16 | Power | Supply voltage |
| VSS | 13, 27 | Ground | Ground |

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