CMOS 8-Bit Microcontroller

TMP86CS43F

The TMP86CS43F is the high-speed, high-performance and low power consumption 8-bit microcomputer, including large-capacity ROM, RAM, multi-function timer/counter, serial bus interface (SIO, UART), 10-bit AD converter and motor control.

Product No.	ROM	RAM	Package	OTP MCU
TMP86CS43F	60 K × 8 bits	2 K × 8 bits	P-QFP80-1420-0.80B	TMP86PS43F

Features

◆ 8-bit single chip microcomputer TLCS-870/C series

• Instruction execution time: $0.25 \mu s$ (at 16 MHz) $122 \mu s (at 32.768 kHz)$

◆ 132 types and 731 basic instructions

24 interrupt sources (External: 6, Internal: 18)

Input/Output ports (71 pins)

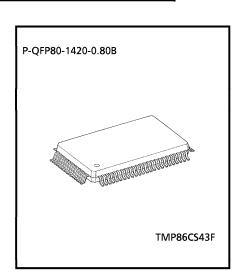
16-bit timer counter: 2 ch

• Timer, Event counter, Pulse width measurement, Programmable divider output mode, External-triggered timer, Window modes.

◆ 8-bit timer counter: 4 ch

• Timer, Event counter, PWM output Programmable divider output mode, PPG mode.

- Time Base Timer
- Divider output function



• For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled

Quality and Reliability Assurance / Handling Precautions.

TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.

In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the "Handling Guide for Semiconductor Devices," or "TOSHIBA Semiconductor Reliability Handbook" etc..

The TOSHIBA products listed in this document are intended for usage in general electronics applications (computer, personal equipment, office equipment, measuring equipment, industrial robotics, domestic, applicances, etc.). These

personal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.). These TOSHIBA products are neither intended nor warranted for usage in equipment that requires extraordinarily high quality and/or reliability or a malfunction or failure of which may cause loss of human life or bodily injury ("Unintended Usage"). Unintended Usage include atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, all types of safety devices, etc.. Unintended Usage of TOSHIBA products listed in this document shall be made at the customer's

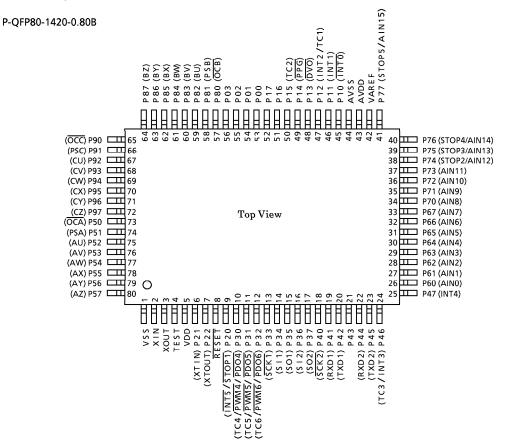
The products described in this document are subject to the foreign exchange and foreign trade laws. The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.

The information contained herein is subject to change without notice.

86CS43-1 2002-10-09

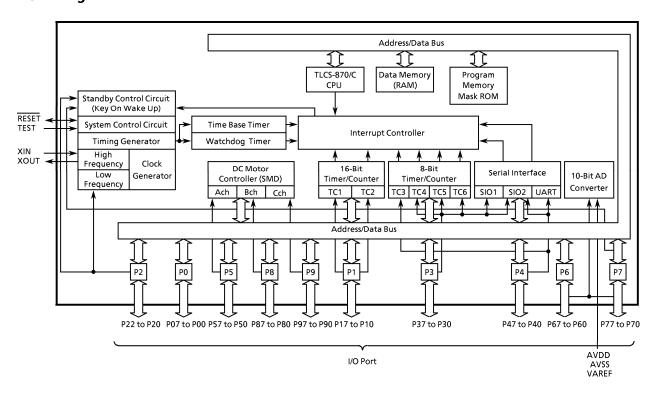
- ♦ Watchdog timer
 - Interrupt source/Reset output (programmable)
- ◆ Serial interface
 - SIO: 2ch
 - UART: 1ch
- ♦ Motor control: 3ch
 - Sensorless DC motor control
 - Overload protection function
- ◆ 10-bit AD converter with sample and hold
 - 16 analog inputs
- ◆ Clock operation
 - Single clock mode
 - Dual clock mode
- ♦ Power saving operating modes
 - STOP mode: Oscillation stops (Battery/Capacitor back-up).
 - SLOW1 mode: Low power consumption operation using low-frequency clock (high-frequency clock stop).
 - SLOW2 mode: Low power consumption operation using low-frequency clock (high-frequency clock oscillator).
 - IDLE0 mode : CPU stops, and only the Time Base Timer (TBT) on Peripherals operate using high-frequency clock. Release by falling edge of the source clock which is set by TBTCR<TBTCK>
 - IDLE1 mode : CPU stops, and Peripherals operate using high-frequency clock. Release by interrupts (CPU restarts).
 - IDLE2 mode : CPU stops, and Peripherals operate using high-and low-frequency clock. Release by interruput (CPU restarts).
 - SLEEP0 mode: CPU stops, and only the Time Base Timer (TBT) on Peripherals operate using low-frequency clock. Release by falling edge of the source clock which is set by TBTCR<TBTCK>
 - SLEEP1 mode: CPU stops, and Peripherals operate using low-frequency clock. Release by interrupts (CPU restarts).
 - SLEEP2 mode: CPU stops, and Peripherals operate using high-and low-frequency clock. Release by interrupt (CPU restarts).
- ◆ Operating voltage: 4.5 V to 5.5 V at 16 MHz/32.768 kHz, 2.7 V to 5.5 V at 8.0 MHz/32.768 kHz

Pin Assignments (Top View)



86CS43-3 2002-10-09

Block Diagram



Pin Functions (1/2)

Pin Name	I/O	Functions					
P00							
P01	1/0	4-bit programmable input/output port.					
P02	I/O	Input or output specified on bit basis.	_				
P03							
P10 (INTO)			External interrupt input				
P11 (INT1)	1/0 (1		External interrupt input				
P12 (INT2/TC1)	I/O (Input)	8-bit programmable input/output port. Input or output specified on bit basis.	External interrupt input/ Timer counter input				
P13 (DVO)	110 (0 · · ·)	When using pins for external interrupt input or timer/counter input, set them to	DVO output				
P14 (PPG)	I/O (Output)	input mode. When using pins for DVO	PPG output				
P15 (TC2)	I/O (Input)	output or PPG output, the output latches set to 1.	Timer counter input				
P16							
P17	I/O		_				
P20 (STOP1/INT5)	I/O (Input)	3-bit input/output ports.	STOP mode release input/				
P21 (XTIN)	o (input)	When used as input port, external interrupt input, STOP mode release signal input, the	External interrupt input				
P22 (XTOUT)	I/O (Output)	input mode is configured.	Low-frequency oscillator connecting pin				
P30 (TC4/PWM4/PDO4)							
P31 (TC5/PWM5/PDO5)	I/O (Input/Output/ Output)		Timer/Counter input PWM output/ PDO output				
P32 (TC6/PWM6/PDO6)	output,	8-bit programmable input/output port. Input or output specified on bit basis.					
P33 (SCK1)	I/O (Input/Output)	When using pins for timer/counter input or SI, set them to input mode. When using	SIO clock input/output				
P34 (SI1)	I/O (Input)	pins PWM output, PDO output or SO, set them to output mode.	SIO1 data input				
P35 (SO1)	I/O (Output)	·	SIO1 data output				
P36 (SI2)	I/O (Input)		SIO2 data input				
P37 (SO2)	I/O (Output)		SIO2 data output				
P40 (SCK2)	I/O (Input/Output)		SIO clock input/output				
P41 (RXD1)	I/O (Input)		UART data input				
P42 (TXD1)	I/O (Output)	 8-bit programmable input/output port.	UART data output				
P43	1/O	Input or output specified on bit basis.	_				
P44 (RXD2)	I/O (Input)	When using pins for UART, set to output latches. When using pins for open-drain	UART data input				
P45 (TXD2)	I/O (Output)	output, set to P4ODE and P4CR.	UART data output				
P46 (INT3/TC3)			External interrupt input/ Timer counter input				
P47 (INT4)	I/O (Input)		External interrupt input				
P50 (OCA)	_						
P51 (PSA)	I/O (Input)		Motor control input				
P52 (AU)		1					
P53 (AV)		8-bit programmable input/output ports. Input or output specified on bit basis. With					
P54 (AW)		a Nch large current output, the direct					
P55 (AX)	I/O (Output)	operation of LED enable.	Motor control output				
P56 (AY)							
P57 (AZ)							

Pin Functions (2/2)

Pin Name	I/O	Functi	ons			
P60 (AIN0)						
P61 (AIN1)						
P62 (AIN2)						
P63 (AIN3)		8-bit programmable input/output port.	AB assurantes analysis insurt			
P64 (AIN4)	I/O (Input)	Input or output specified on bit basis.	AD converter analog input			
P65 (AIN5)						
P66 (AIN6)						
P67 (AIN7)						
P70 (AIN8)						
P71 (AIN9)						
P72 (AIN10)			AD converter analog input			
P73 (AIN11)		8-bit programmable input/output port.				
P74 (AIN12/STOP2)	I/O (Input)	Input or output specified on bit basis.				
P75 (AIN13/STOP3)			AD converter analog input			
P76 (AIN14/STOP4)			STOP mode release input			
P77 (AIN15/STOP5)						
P80 (OCB)						
P81 (PSB)	I/O (Input)		Motor control input			
P82 (BU)						
P83 (BV)		8-bit programmable input/output port.				
P84 (BW)	1/0/0 ()	Input or output specified on bit basis.				
P85 (BX)	I/O (Output)		Motor control output			
P86 (BY)						
P87 (BZ)						
P90 (OCC)	1/O (Inn.ut)		N/oton control in mut			
P91 (PSC)	I/O (Input)		Motor control input			
P92 (CU)		Obit and an arranged a facility of the standard and a second				
P93 (CV)		8-bit programmable input/output port. Input or output specified on bit basis. With				
P94 (CW)	I/O (Output)	a Nch large current output, the direct operation of LED enable.	Matar control output			
P95 (CX)	//O (Output)	operation of LED enable.	Motor control output			
P96 (CY)						
P97 (CZ)						
TEST	Input	Shipment test pin, fix to "L" level				
RESET	I/O	_				
XIN	Input	High-frequency oscillator connecting pins.				
XOUT	Output	For external clock input, input to XIN and leav	ve XOUT open.			
VSS		GND				
VDD		vcc				
AVSS	Power Supply	Analog reference GND for AD conversion.				
AVDD		Analog voltage for AD conversion.				
VAREF		Analog reference voltage for AD conversion.				

Operational Description

1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, and an interrupt controller.

This section provides a description of the CPU core, the program memory, the data memory, and the reset circuit.

1.1 Memory Address Map

The TMP86CS43 memory consist of 4 blocks: ROM, RAM, DBR (Data Buffer Register) and SFR (Special Function Register). They are all mapped in 64-Kbyte address space. Figure 1-1 shows the TMP86CS43 memory address map. The general-purpose registers are not assigned to the RAM address space.

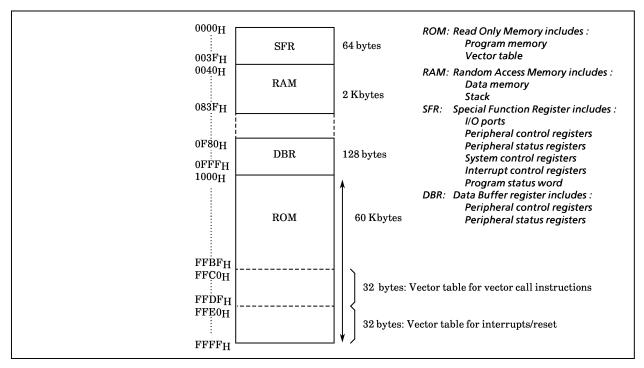


Figure 1-1. Memory Address Map

1.2 Program Memory (ROM)

The TMP86CS43 has a 60 K×8 bits (Address 1000_H to FFFF_H) of program memory (mask programmed ROM). However, placing program memory on the internal RAM is deregulated if a certain procedure is executed (See 2.4.5 Address Trap).

86CS43-7 2002-10-09

Electrical Characteristics

Absolute Maximum Ratings $(V_{SS} = 0 V)$

Parameter	Symbol	Pins	Ratings	Unit	
Supply Voltage	V _{DD}		- 0.3 to 6.5		
Input Voltage	V _{IN}		- 0.3 to V _{DD} + 0.3	7 v	
Output Voltage	V _{OUT}		- 0.3 to V _{DD} + 0.3		
	louth	Except open drain	- 3.2		
	I _{OUT1}	Except P5, P8, P9	3.2	1	
Output Current (Per 1 pin)	I _{OUT2}	P5		1	
	I _{OUT3}	P8	30	mA	
	I _{OUT4}	P9			
	Σl _{OUT1}	Except P5, P8, P9			
Output Current (Total)	Σl _{OUT2}	P5	60		
Output Current (Total)	Σl _{OUT3}	P8] 00		
	ΣI _{OUT4}	P9			
Power Dissipation $[T_{opr} = 85^{\circ}C]$	PD		250	mW	
Soldering Temperature (time)	Tsld		260 (10 s)		
Storage Temperature	Tstg		– 55 to 125	ີ ∘c	
Operating Temperature	Topr		- 40 to 85		

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant.

Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Condition

 $(V_{SS} = 0 \text{ V, Topr} = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Pins	С	ondition	Min	Max	Unit		
			fc = Each ope		4.5	5.5			
Supply Voltage	V _{DD}		fc = 1 to 8 MHz	Each operation modes	2.7	5.5			
			fs = 32.768 kHz	Each operation modes	2.7	5.5			
			STOP mode		2.0	5.5	V		
	V _{IH1}	Hysteresis	V > 4.5.V		$V_{DD} \times 0.70$				
Input high Level	V _{IH2}	Hysteresis] v _c	_{DD} ≥ 4.5 V	$V_{DD} \times 0.75$	V_{DD}			
	V _{IH3}		V _{DD} < 4.5 V		$V_{DD} \times 0.90$				
	V _{IL1}	Hysteresis	.,,	> 4.5.7		$V_{DD} \times 0.30$			
Input low Level	V _{IL2}	Hysteresis	$V_{DD} \ge 4.5 V$		$V_{DD} \leq 4.5 \text{ V}$		0	V _{DD} × 0.25	
	V _{IL3}		V	V _{DD} < 4.5 V		V _{DD} × 0.10			
Clock Frequency	4.	VIN VOUT	V _{DD} = 4.5 to 5.5 V		1.0	16.0	NALL-		
	Clock Frequency	fc	XIN, XOUT	V _{DD} :	V _{DD} = 2.7 to 5.5 V		8.0	MHz	
	fs	XTEN, XTOUT			30.0	34.0	kHz		

Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

DC Characteristics $(V_{SS} = 0 \text{ V}, \text{Topr} = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Pins	Condition	Min	Тур.	Max	Unit
Hysteresis Voltage	V _{HS}	Hysteresis input		-	0.9	_	٧
	I _{IN1}	TEST					
Input Current	I _{IN2}	Sink Open Drain, Tri-state port			_	± 2	μΑ
	I _{IN3}	STOP, RESET					
Input Resistance	R _{IN1}	RESET		100	220	450	kΩ
OSC. Feedback	Rfx	XIN-XOUT		_	1.2	_	
resistance	Rfxt	XTIN-XTOUT		_	6	_	ΜΩ
Output Leakage	I _{LO1}	Sink Open Drain port	V _{DD} = 5.5 V, V _{OUT} = 5.5 V	_	-	2	
Current	I _{LO2}	Tri-state port	V _{DD} = 5.5 V, V _{OUT} = 5.5 V/0 V	= 5.5 V/0 V – -		± 2	μΑ
"H" output Voltage	V _{OH}	Tri-state port	$V_{DD} = 4.5 \text{ V}, I_{OH} = -0.7 \text{ mA}$	4.1	-	_	
"L" output Voltage	V _{OL3}	Except XOUT, P5, P8, P9	$V_{DD} = 4.5 \text{ V, } I_{OL} = 1.6 \text{ mA}$	_	-	0.4	V
#1.# · · · · · · · · · · · · · · · · · · ·	I _{OL1}	Except XOUT, P5, P8, P9	$V_{DD} = 4.5 \text{ V}, V_{OL} = 0.4 \text{ V}$	_	1.6	_	
"L" output Current	I _{OL3}	High current port (P5, P8, P9)	$V_{DD} = 4.5 \text{ V}, V_{OL} = 1.0 \text{ V}$	_	20	_	
Supply Current in			V _{DD} = 5.5 V		15	20	mA
Normal 1, 2 mode			V _{IN} = 5.3 V/0.2 V		15	20	l IIIA
Supply Current in			fc = 16 MHz	_	9	13	
IDLE 1, 2 mode			fs = 32.768 kHz				
Supply Current in	I _{DD}		V _{DD} = 3.0 V	_	30	60	
SLOW 1 mode			V _{IN} = 2.8 V/0.2 V				
Supply Current in			fs = 32.768 kHz	_	15	30	μA
SLEEP 0, 1 mode			13 - 32.7 65 KHZ		,,		<i>μ</i> `.
Supply Current in			$V_{DD} = 5.5 V$	_	0.5	10	
STOP mode	1		$V_{IN} = 5.3 V/0.2 V$		"		

Note 1: Typical values show those at Topr = 25° C, $V_{DD} = 5 V$

Note 2: Input current (I_{IN1} , I_{IN3}); The current through pull-up or pull-down resistor is not included.

Note 3: IDD does not include IREF current.

AD Conversion Characteristics

(V_{SS} = 0 V, 4.5 V
$$\leq$$
 V_{DD} \leq 5.5 V, Topr = -40 to 85°C)

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Analog Reference Voltage	V _{AREF}		A _{VDD} – 1.0	-	A _{VDD}	
Power Supply Voltage of	A _{VDD}			V_{DD}		
Analog Control Circuit	A _{VSS}			V_{SS}] _v
Analog Reference of Voltage Range	$\triangle V_{AREF}$	V _{AREF} – V _{SS}	3.5	-	V _{DD}	'
Analog Input Voltage	V _{AIN}		V _{SS}	_	V _{AREF}	
Power Supply Current of Analog Reference Voltage	I _{REF}	$V_{DD} = A_{VDD} = V_{AREF} = 5.5 \text{ V}$ $V_{SS} = 0.0 \text{ V}$	-	0.6	1.0	mA
Non linearity Error			-	-	± 2	
Zero Point Error		$V_{DD} = A_{VDD} = 5.0 \text{ V}$	_	-	± 2] , , ,
Full Scale Error		$V_{SS} = A_{VSS} = 0.0 \text{ V}$ $V_{AREF} = 5.0 \text{ V}$	-	_	± 2	LSB
Total Error			_	-	± 4	

- Note 1: Total error includes all error except a quantization error, and is defined as a maximum deviation from the ideal conversion line.
- Note 2: Conversion time is different in recommended value by power supply voltage. About conversion time, please refer to "2.14.2 Register Configuration".
- Note 3: Please use input voltage to AIN input Pin in limit of V_{AREF} V_{SS}.

 When voltage of range outside is input, conversion value becomes unsettled and gives affect to other channel conversion value.

AC Characteristics

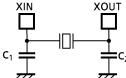
(V_{SS} = 0 V,
$$4.5 \le V_{DD} \le 5.5$$
 V, Topr = -40 to 85° C)

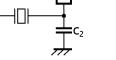
Parameter	Symbol	Condition	Min	Тур.	Max	Unit
		NORMAL 1, 2 mode	0.25	-	4	
Machine Cycle Time		IDLE 0, 1, 2 mode				μS
	tcy	SLOW 1, 2 mode			422.2	
		SLEEP 0, 1, 2 mode	117.6	1	133.3	ms
High Level Clock Pulse Width	t _{WCH}	For external clock operation (XIN input) fc = 16 MHz		24.25		_
Low Level Clock Pulse Width	t _{WCL}			31.25	I	μS
High Level Clock Pulse Width	t _{WSH}	For external clock operation (XTIN input)		45.26		
Low Level Clock Pulse Width	t _{WSL}	fs = 32.768 kHz	-	15.26	-	ms

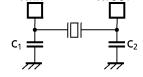
Recommended Oscillating Conditions-1

$$(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, \text{ Topr} = -40 \text{ to } 85^{\circ}\text{C})$$

Parameter	On Alleston	Oscillation	D	Recommended Oscillator		ed Constant
Parameter	Oscillator	Frequency	Recom			C ₂
			MURATA	CSA16.00MXZ040	10 pF	10 pF
Link francis	Ceramic Resonator	0.0411=	MURATA	CSA8.00MTZ	30 pF	30 pF
High-frequency Oscillation		8 MHz		CST8.00MTW	30 pF (built-in)	30 pF (built-in)
Oscillation		4 40 0411-	MURATA	CSA4.19MG	30 pF	30 pF
		4.19 MHz		CST4.19MGW	30 pF (built-in)	30 pF (built-in)
Low-frequency Oscillation	Crystal Oscillator	32.768 kHz	SII	VT-200	6 pF	6 pF







(1) High-frequency Oscillation

(2) Low-frequency Oscillation

- Note 1: An electrical shield by metal shield plate on the surface of IC package is recommended in order to protect the device from the high electric field stress applied from CRT (Cathodic Ray Tube) for continuous reliable operation.
- Note 2: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL; http://www.murata.co.jp/search/index.html