CMOS 8-Bit Microcontroller

TMP87CK43N, TMP87CM43N

The 87CK43/M43 is the high speed and high performance 8-bit single chip microcomputer. This MCU contains CPU core, ROM, RAM, input/output ports, an A/D converter, six multi-function timer/counters, serial bus interface, and two clock generators on a chip.

Part No.	ROM	RAM	Package	OTP MCU
TMP87CK43N	24 Kbytes	1 Kbytes	P-SDIP42-600-1.78	TMP87PM43N
TMP87CM43N	32 Kbytes			

Features

◆8-bit single chip microcomputer TLCS-870 Series
◆Instruction execution time: 0.5 μs (at 8 MHz), 122 μs (at 32.768kHz)
◆412 basic instructions
- Multiplication and Division (8bits × 8bits , 16bits ÷ 8bits)
- Bit manipulations (Set/Clear/Complement/Load/Store/Test/Exclusive or)
- 16-bit data operations
- 1-byte jump/subroutine-call (Short relative jump / Vector call)

◆13 interrupt sources (External: 5, Internal: 8)
- All sources have independent latches each, and nested interrupt control is available.
- 3 edge-selectable external interrupts with noise reject
- High-speed task switching by register bank changeover

◆5 Input/Output ports (35 pins)
◆Two 16-bit Timer/Counters
- Timer, Event counter modes

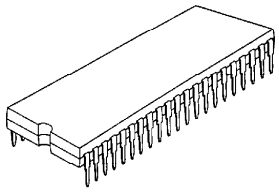
◆Two 8-bit Timer/Counters
- Timer, Event counter, Capture (Pulse width/duty measurement) modes

◆Time Base Timer (Interrupt frequency: 1 Hz to 16 kHz)
◆Divider output function (frequency: 1 kHz to 8 kHz)
◆Watchdog Timer
- Interrupt source/reset output (programmable)

◆Serial Bus Interface
- I²C-Bus / 8-bit SIO modes
- Selectable two I/O channels

◆8-bit successive approximate type A/D converter with sample and hold
- 6 analog inputs
- Conversion time: 23 μs at 8MHz

P-SDIP42-600-1.78



TMP87CK43N
TMP87CM43N
TMP87PM43N

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◆PWM outputs
- 14-bit PWM output (1 channel)
- 7-bit PWM output (1 channel)

◆Dual clock operation
- Single/Dual-clock mode (option)

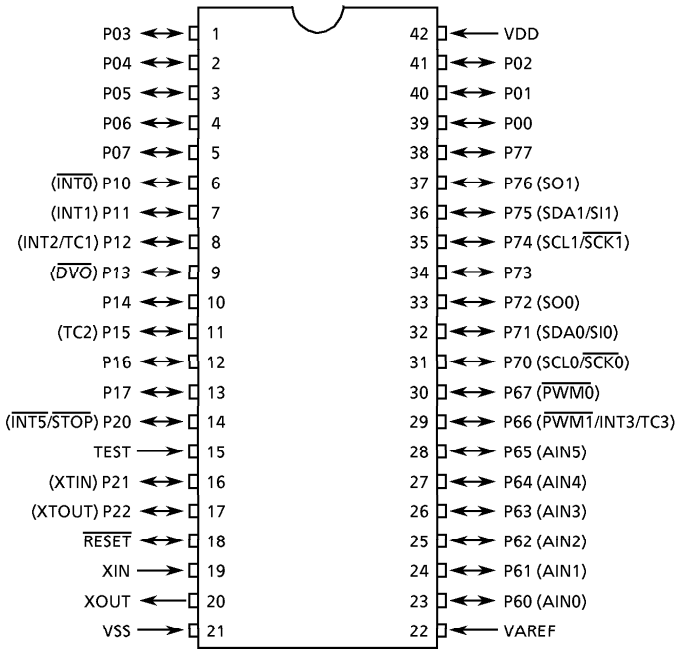
◆Five Power saving operating modes
- STOP mode: Oscillation stops. Battery/Capacitor back-up. Port output hold/High-impedance.
- SLOW mode: Low power consumption operation using low-frequency clock (32.768 kHz).
- IDLE1 mode: CPU stops, and Peripherals operate using high-frequency clock. Release by interrupts.
- IDLE2 mode: CPU stops, and Peripherals operate using high and low frequency clock. Release by interrupts.
- SLEEP mode: CPU stops, and Peripherals operate using low-frequency clock. Release by interrupts.

◆Wide operating voltage: 4.5 to 5.5 V at 8 MHz, 2.7 to 5.5 V at 4.19 MHz/32.768 kHz

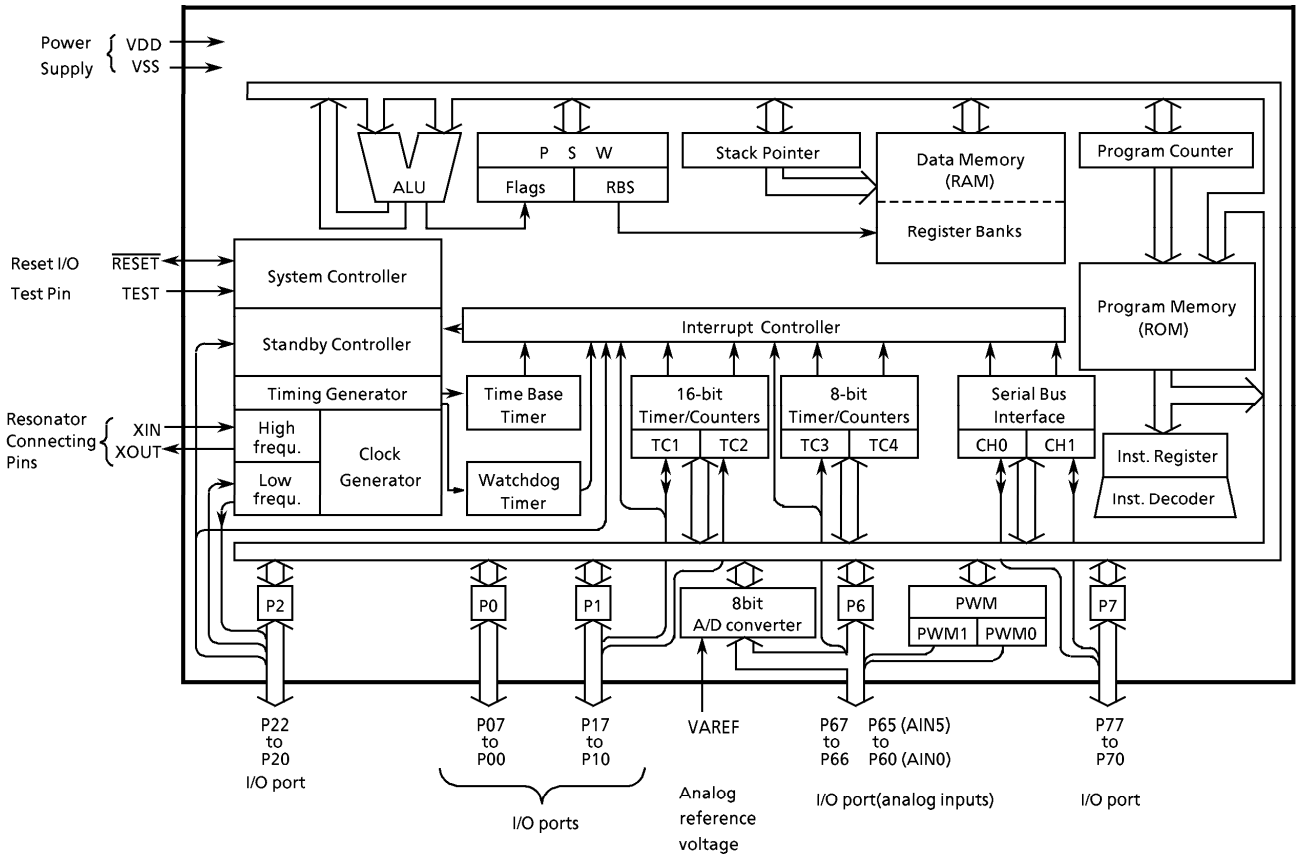
◆Emulation Pod: BM87CM43N0A

Pin Assignments (Top View)

P-SDIP42-600-1.78



Block Diagram



Pin Function

Pin Name	Input / Output	Function	
P07 to P00	I/O	Two 8-bit programmable input/output ports (tri-state).	
P17, P16, P14	I/O	Each bit of these ports can be individually configured as an input or an output under software control.	
P15 (TC2)	I/O (Input)	When used as an external interrupt input or a timer/counter input, these ports must be as inputs.	Timer/Counter 2 input
P13 ($\overline{DVO}$)	I/O (Output)	When used as a divider output, the data and input/output control latch must be set to "1".	Divider output
P12 (INT2 / TC1)	I/O (Input/Input)		External interrupt input 2 or Timer/Counter 1 input
P11 (INT1)	I/O (Input)		External interrupt input 1
P10 ($\overline{INT0}$)			External interrupt input 0
P22 (XTOUT)	I/O (Output)	3-bit input/output port with latch.	Resonator connecting pins (32.768 kHz).
P21 (XTIN)	I/O (Input)	When used as an input port, the latch must be set to "1".	For inputting external clock, XTIN is used and XTOUT is opened.
P20 ($\overline{INT5}$ / $\overline{STOP}$)			External interrupt input 5 or STOP mode release signal input
P67 ($\overline{PWM0}$)	I/O (Output)	8-bit programmable input/output port. Each bit of the port can be individually configured as an input or an output under software control. When used as a PWM output, the data and input/output control latch must be set to "1".	14-bit PWM output
P66 ($\overline{PWM1}$/ INT3/TC3)	I/O (Output/ Input/Input)		7-bit PWM output, External interrupt input 3 or Timer/Counter 3 input
P65 (AIN5) to P60 (AIN0)	I/O (Input)		A/D converter analog inputs
P77	I/O	8-bit programmable input/output port. Each bit of the port can be individually configured as an input or an output under software control. When used as output or I/O port of the Serial Bus Interface, the data and input/output control latch must be set to "1".	
P76 (SO1)	I/O (Output)		Serial data output 1 (SIO)
P75 (SDA1/SI1)	I/O (I or O/Input)		Serial data input/output 1 (I^2C-BUS) / Serial data input 1 (SIO)
P74 (SCL1/$\overline{SCK1}$)	I/O (I or O)		Serial clock input/output 1 (I^2C-BUS/SIO)
P73	I/O		
P72 (SO0)	I/O (Output)		Serial data output 0 (SIO)
P71 (SDA0/SI0)	I/O (I or O/Input)		Serial data input/output 0 (I^2C-BUS) / Serial data input 0 (SIO)
P70 (SCL0/$\overline{SCK0}$)	I/O (I or O)		Serial clock input/output 0 (I^2C-BUS/SIO)
XIN, XOUT	Input, Output	Resonator connecting pins for high-frequency clock. For inputting external clock, XIN is used and XOUT is opened.	
$\overline{RESET}$	I/O	Reset signal input or watchdog timer output/address-trap-reset output/system-clock-reset output.	
TEST	Input	Test pin for out-going test. Be tied to low.	
VDD, VSS	Power Supply	+ 5 V, 0 V (GND)	
VAREF		Analog reference voltage input	

OPERATIONAL DESCRIPTION

1. CPU CORE FUNCTIONS

The CPU core consists of a CPU, a system clock controller, an interrupt controller, and a watchdog timer. This section provides a description of the CPU core, the program memory (ROM), the data memory (RAM), and the reset circuit.

1.1 Memory Address Map

The TLCS-870 Series is capable of addressing 64K bytes of memory. Figure 1-1 shows the memory address maps of the 87CK43/M43. In the 87CK43/M43, the memory is organized 3 address spaces (ROM, RAM, and SFR). It uses a memory mapped I/O system, and all I/O registers are mapped in the SFR address spaces. There are 16 banks of general-purpose registers. The register banks are also assigned to the first 128 bytes of the RAM address space.

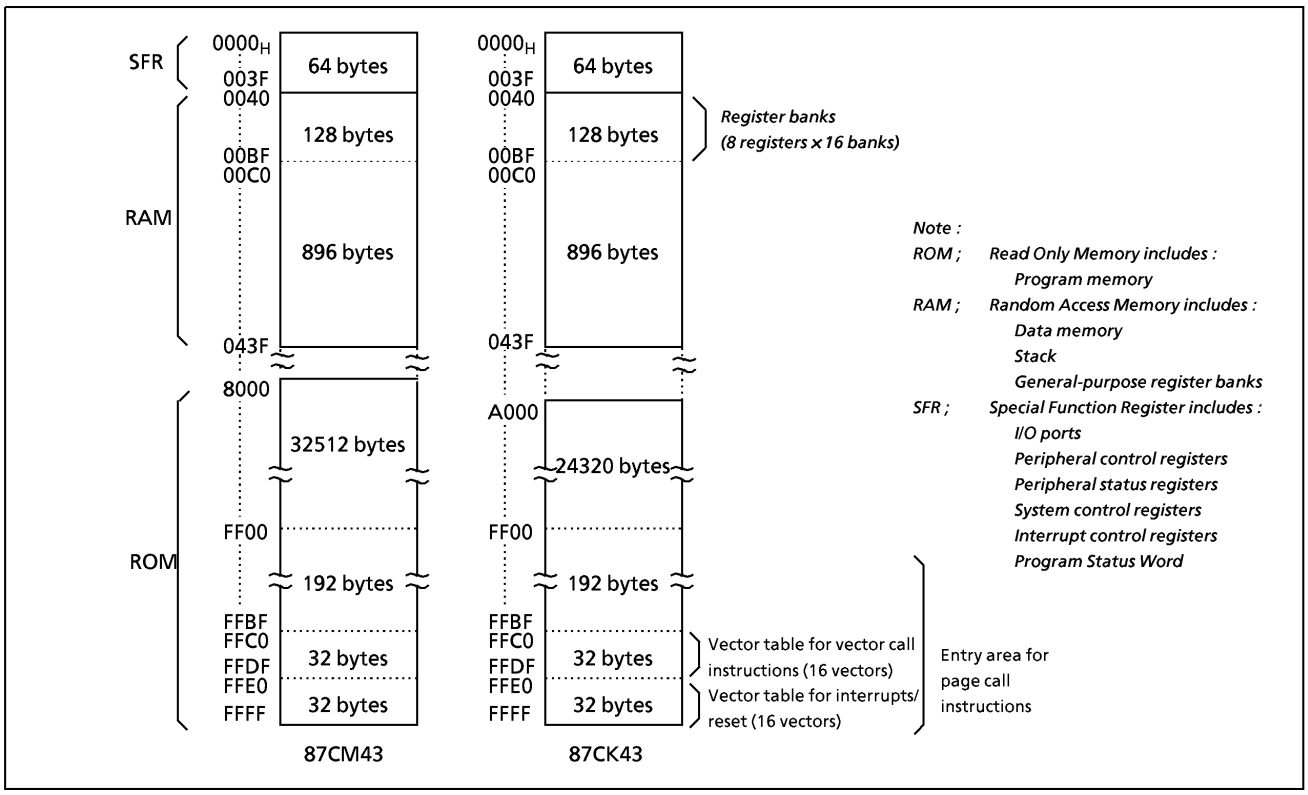


Figure 1-1. Memory Address Maps

Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	V_{DD}		– 0.3 to 6.5	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	Ports P0, P1, P21, P22, P60 to P65, $\overline{RESET}$, XOUT	– 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	Ports P20, P66, P67, P7	– 0.3 to V_{DD} + 0.3	
Output Current (Per 1 pin)	I_{OUT1}	Ports P0, P1, P2, P6, P7	3.2	mA
Output Current (Total)	ΣI_{OUT1}	Ports P0, P1, P2, P6, P7	120	mA
Power Dissipation [Topr = 70°C]	PD		600	mW
Soldering Temperature (time)	Tsld		260 (10s)	°C
Storage Temperature	Tstg		– 55 to 125	°C
Operating Temperature	Topr		– 30 to 70	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Conditions (V_{SS} = 0 V, Topr = – 40 to 85°C)

Parameter	Symbol	Pins	Conditions		Min	Max	Unit
Supply Voltage	V_{DD}		fc = 8 MHz	NORMAL1, 2 mode	4.5	5.5	V
				IDLE1, 2 mode			
			fs = 32.768 kHz	SLOW mode	2.7		
				SLEEP mode			
				STOP mode	2.0		
Input High Voltage	V_{IH1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		$V_{DD} \times 0.70$	V_{DD}	V
	V_{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.90$		
Input Low Voltage	V_{IL1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		0	$V_{DD} \times 0.30$	V
	V_{IL2}	Hysteresis input				$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$ V			$V_{DD} \times 0.10$	
Clock Frequency	fc	XIN, XOUT	V_{DD} = 4.5 to 5.5 V		2.0	8.0	MHz
	fs	XTIN, XTOUT	V_{DD} = 2.7 to 5.5 V		30.0	34.0	kHz

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: fc: The condition of power supply voltage is limited to NORMAL1, NORMAL2, IDLE1, and IDLE2 mode.

D.C. Characteristics

(V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions	Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis inputs		–	0.9	–	V
Input Current	I_{IN1}	TEST	V_{DD} = 5.5 V V_{IN} = 5.5 V / 0 V	–	–	± 2	μA
	I_{IN2}	Open drain ports and tri-state ports					
	I_{IN3}	$\overline{RESET}$, $\overline{STOP}$					
Input Resistance	R_{IN2}	$\overline{RESET}$		100	220	450	kΩ
Output Leakage Current	I_{LO}	Open drain ports and tri-state ports	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	–	–	2	μA
Output High Voltage	V_{OH2}	Tri- state ports	V_{DD} = 4.5 V, I_{OH} = – 0.7 mA	4.1	–	–	V
Output Low Voltage	V_{OL}	Except XOUT	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	–	–	0.4	V
Supply Current in NORMAL 1 , 2 mode	I_{DD}		V_{DD} = 5.5 V V_{IN} = 5.3 V / 0 .2 V fc = 8 MHz fs = 32.768 kHz	–	10	16	mA
Supply Current in IDLE 1, 2 mode				–	4.5	6	mA
Supply Current in SLOW mode			V_{DD} = 3.0 V V_{IN} = 2.8 V / 0 .2 V fs = 32.768 kHz	–	30	60	μA
Supply Current in SLEEP mode				–	15	30	μA
Supply Current in STOP mode			V_{DD} = 5.5 V V_{IN} = 5.3 V / 0 .2 V	–	0.5	10	μA

Note 1: Typical values show those at Topr = 25°C , V_{DD} = 5 V.
Note 2: Input Current ; The current through pull-up or pull-down resistor is not included.

A / D Conversion Characteristics

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}	$V_{DD} \geqq 4.5$ V, V_{SS} = 0 V	V_{DD} – 1.5	—	V_{DD}	V
Analog Reference Voltage Range	$_{\Delta}V_{AREF}$		3.0	—	—	V
Analog Input Voltage Range	V_{AIN}		V_{SS}	—	V_{AREF}	V
Analog Supply Current	I_{REF}		—	0.5	1.0	mA
Nonlinearity Error		V_{DD} = 5.0 V, V_{SS} = 0.000 V V_{AREF} = 5.000 V	—	—	± 1	LSB
Zero Point Error			—	—	± 1	
Full Scale Error			—	—	± 1	
Total Error			—	—	± 2	

Note : $_{\Delta}V_{AREF} = V_{AREF} - V_{SS}$

A.C. Characteristics

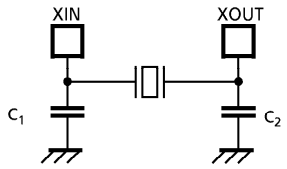
(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Machine Cycle Time	t_{cy}	In NORMAL1, 2 modes	0.5	–	10	μs
		In IDLE1, 2 modes				
		In SLOW mode	117.6	–	133.3	
		In SLEEP mode				
High Level Clock Pulse Width	t_{WCH}	For external clock operation (XIN input), fc = 8 MHz	50	–	–	ns
Low Level Clock Pulse Width	t_{WCL}					
High Level Clock Pulse Width	t_{WSH}	For external clock operation (XTIN input), fs = 32.768 kHz	14.7	–	–	μs
Low Level Clock Pulse Width	t_{WSL}					

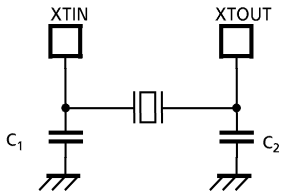
Recommended Oscillating Condition

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Oscillator	Frequency	Recommended Oscillator		Recommended Condition C_1	Recommended Condition C_2
High-frequency	Ceramic Resonator	8 MHz	KYOCERA	KBR8.0M	30 pF	30 pF
		4 MHz	KYOCERA	KBR4.0MS		
			MURATA	CSA4.00MG		
	Crystal Oscillator	8 MHz	TOYOCOM	210B 8.0000	20 pF	20 pF
		4 MHz	TOYOCOM	204B 4.0000		
Low-frequency	Crystal Oscillator	32.768 kHz	NDK	MX-38T	15 pF	15 pF



(1) High-frequency



(2) Low-frequency

Note: An electrical shield by metal shield plate on the surface of the IC package should be recommendable in order to prevent the device from the high electric fieldstress applied from CRT (Cathode Ray Tube) for continuous reliable operation.