CMOS 16-Bit Microcontrollers

TMP91CW18AF

1. Outline and Features

TMP91CW18A is a high-speed 16-bit microcontroller designed for the control of various mid-to large-scale equipment.

TMP91CW18A comes in a 80-pin flat package.

Listed below are the features.

(1) High-speed 16-bit CPU (900/L1 CPU)
- Instruction mnemonics are upward-compatible with TLCS-90/900/900H
- 16 Mbytes of linear address space
- General-purpose registers and register banks
- 16-bit multiplication and division instructions; Bit transfer and arithmetic instructions
- Micro DMA: 4 channels (0.64 μs/2 bytes at 25 MHz)

(2) Minimum instruction execution time: 160 ns (at 25 MHz)

(3) Built-in RAM: 4 Kbytes
Built-in ROM: 128 Kbytes

(4) External memory expansion
- Expandable up to 16 Mbytes (shared program/data area)

(5) Wait controller: 1 channel

(6) 8-bit timers: 8 channels

(7) 16-bit timer: 1 channel

(8) General-purpose serial interface (UART): 1 channel

(9) Serial bus interface (I^2C/Select of synchronous): 1 channel

(10) Serial bus interface (I^2C): 2 channels

(11) 10-bit AD converter (S/H): 12 channels

- Conversion time: 84 states (6.72 μs at f_{FPH} = 25 MHz)

(12) Watchdog timer

(13) Interrupts function

- 9 CPU interrupts: Software interrupt instruction and illegal instruction
- 22 internal interrupts: ┐
- 8 external interrupts: ┘ Seven selectable priority levels

(14) Input/Output ports: 62 pins

- I/O: 50 pins (Programmable open-drain: 12 pins)
- Input: 12 pins

(15) Standby mode

Three HALT modes: Programmable-IDLE2, IDLE1, STOP

(16) Clock controller

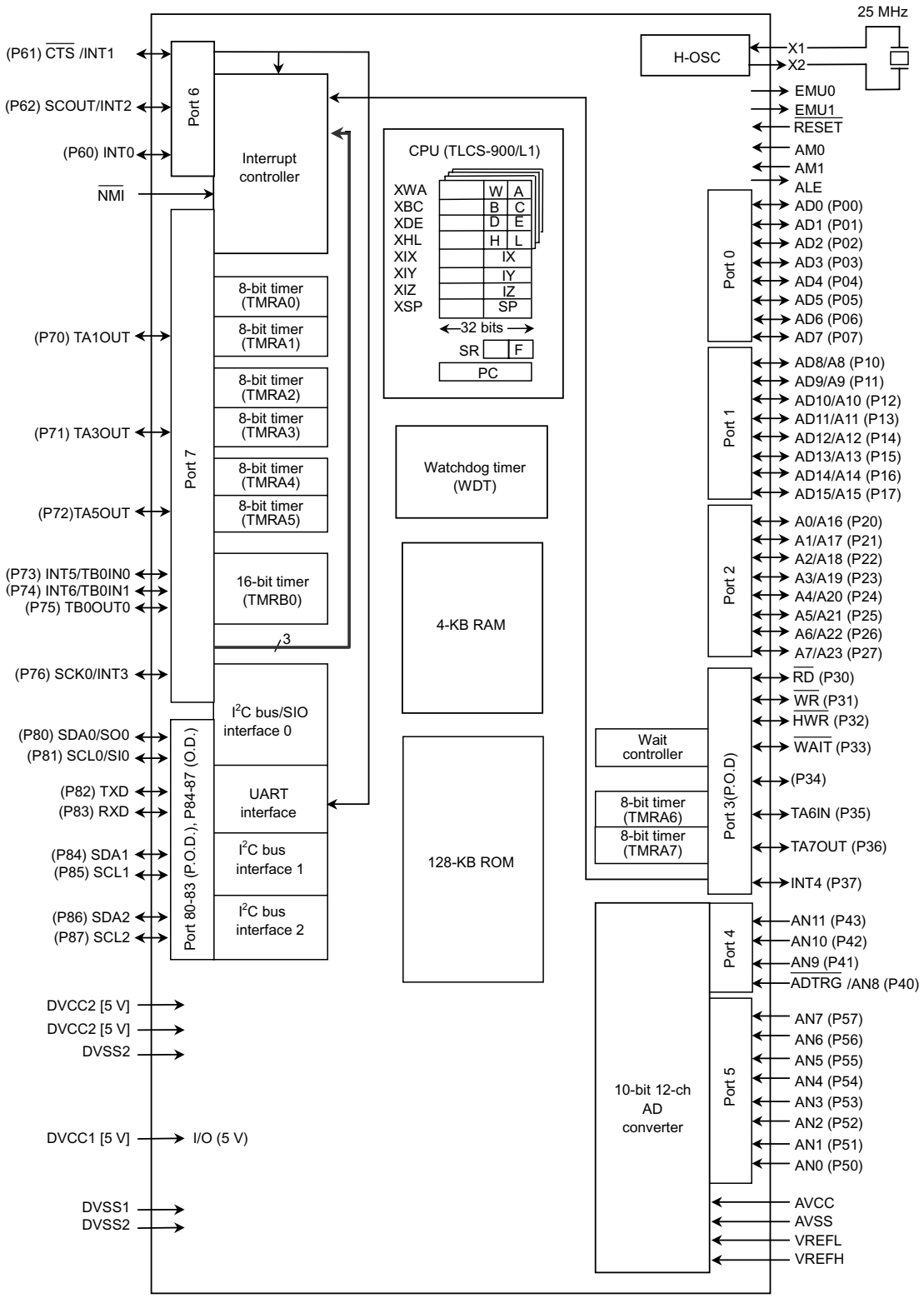
- Clock gear: changes high frequency clock fc to fc/16

(17) Open voltage

- Vcc = 4.5 V to 5.5 V (fc max = 25 MHz)

(18) Package

- P-QFP80-1420-0.80B



( ) : Initial function after reset

Figure 1 TMP91CW18A block diagram

2. Pin Assignment and Pin Functions

The assignment of input/output pins for the TMP91CW18A, their names and functions are as follows:

2.1 Pin Assignment Diagram

Figure 2.1.1 shows the pin assignment of the TMP91CW18A.

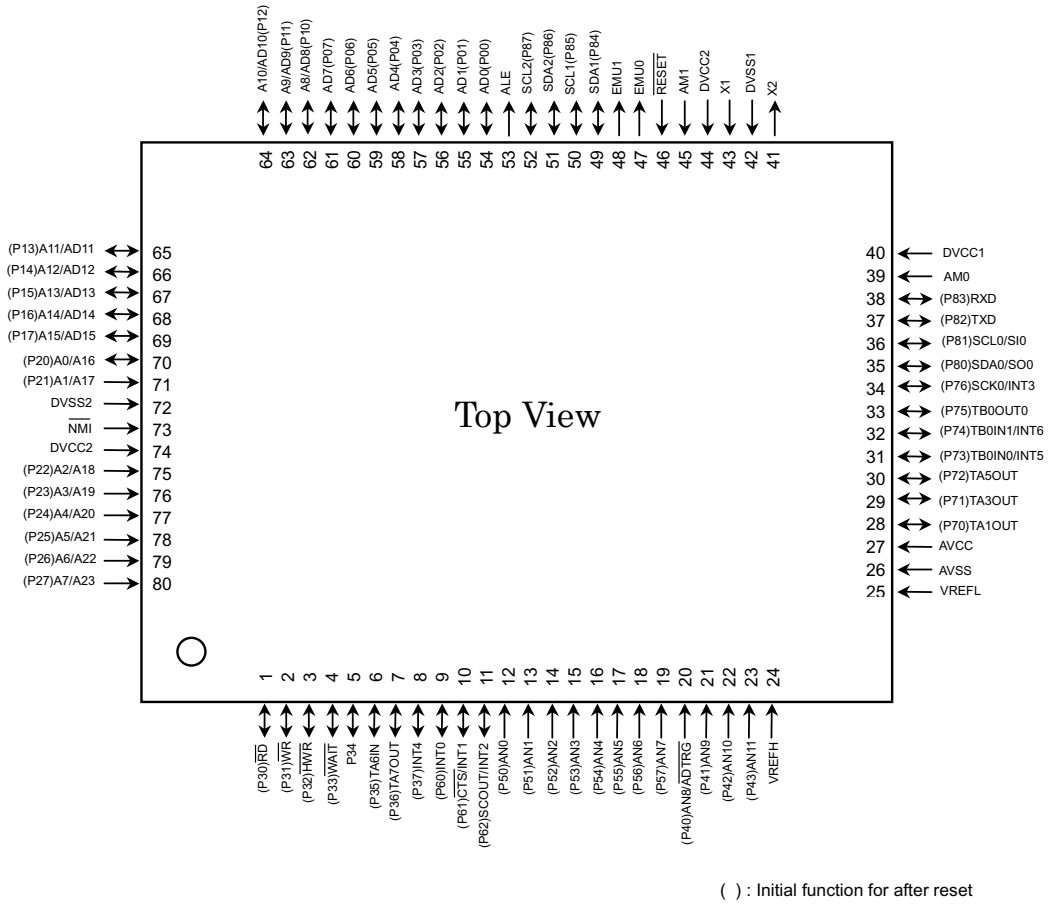


Figure 2.1.1 Pin assignment diagram (80-pin QFP)

2.2 Pin Names and Functions

The names of the input/output pins and their functions are described below.

Table 2.2.1 Pin names and functions (1/3)

Pin name	Number of pins	I/O	Functions
P00 to P07 AD0 to AD7	8	I/O Tri-state	Port 0: I/O port that allows I/O to be selected at the bit level Address and data (lower): bits 0 to 7 of address and data bus
P10 to P17 AD8 to AD15 A8 to A15	8	I/O Tri-state Output	Port 1: I/O port that allows I/O to be selected at the bit level Address and data (upper): bits 8 to 15 for address and data bus Address: bits 8 to 15 of address bus
P20 to P27 A0 to A7 A16 to A23	8	I/O Output Output	Port 2: I/O port that allows I/O to be selected at the bit level Address: bits 0 to 7 of address bus Address: bits 16 to 23 of address bus
P30 $\overline{RD}$	1	I/O Output	Port 30: output port By setting (P3<P30> = 0 , P3FC<P30FC> = 1), $\overline{RD}$ signal is generated during reading internal areas. Read: strobe signal for reading external memory Open-drain output pin by programmable
P31 $\overline{WR}$	1	I/O Output	Port 31: output port Write: strobe signal for writing data to pins AD0 to AD7 Open-drain output pin by programmable
P32 $\overline{HWR}$	1	I/O Output	Port 32: I/O port (with pull-up resistor) High Write: strobe signal for writing data to pins AD8 to AD15 Open-drain output pin by programmable
P33 $\overline{WAIT}$	1	I/O Input	Port 33: I/O port (with pull-up resistor) Wait: pin used to request CPU bus wait Open-drain output pin by programmable
P34	1	I/O	Port 34: I/O port Open-drain output pin by programmable
P35 TA6IN	1	I/O Input	Port 35: I/O port Timer A6 Input Open-drain output pin by programmable
P36 TA7OUT	1	I/O Output	Port 36: I/O port Timer A7 Output Open-drain output pin by programmable
P37 INT4	1	I/O Input	Port 37: I/O port Interrupt request pin 4: Interrupt request pin with programmable rising edge/falling edge levels Open-drain output pin by programmable
P40 to P43 AN8 to AN11 $\overline{ADTRG}$	4	Input Input Input	Port 40: pin used to input port Analog input: pin used to input to AD converte AD Trigger: signal used to request start of AD conversion
P50 to P57 AN0 to AN7	8	Input Input	Port 5: pin used to input port Analog input: pin used to input to AD converter
P60 INT0	1	I/O Input	Port 60: I/O port Interrupt request pin 0: Interrupt request pin with programmable rising edge/falling edge levels
P61 $\overline{CTS}$ INT1	1	I/O Input Input	Port 61: I/O port Serial data send enable (Clear to send) Interrupt request pin 1: Interrupt request pin with programmable rising edge/falling edge levels
P62 SCOUT INT2	1	I/O Output Input	Port 62: I/O port System clock output: outputs f_{FPH} or fs clock Interrupt request pin 2: Interrupt request pin with programmable rising edge/falling edge levels

Table 2.2.2 Pin names and functions (2/3)

Pin name	Number of pins	I/O	Functions
P70	1	I/O	Port 70: I/O port
TA1OUT		Output	Timer A1 output
P71	1	I/O	Port 71: I/O port
TA3OUT		Output	Timer A3 output
P72	1	I/O	Port 72: I/O port
TA5OUT		Output	Timer A5 output
P73	1	I/O	Port 73: I/O port
TB0IN0		Input	Timer B0 input 0
INT5		Input	Interrupt request pin 5: Interrupt request pin with programmable rising edge/falling edge levels
P74	1	I/O	Port 74: I/O port
TB0IN1		Input	Timer B0 input 1
INT6		Input	Interrupt request pin 6: Interrupt request pin with programmable rising edge/falling edge levels
P75	1	I/O	Port 75: I/O port
TB0OUT0		Output	Timer B0 output0
P76	1	I/O	Port 76: I/O port
SCK0		I/O	Serial clock I/O 0
INT3		Input	Interrupt request pin 3: Interrupt request pin with programmable rising edge/falling edge levels
P80	1	I/O	Port 80: I/O port
SO0		Output	Serial bus interface send data at SIO mode 0.
SDA0		I/O	Serial bus interface send/receve data at I^2C mode 0. Open-drain output pin by programmable
P81	1	I/O	Port 81: I/O port
SI0		Input	Serial bus interface receve data at SIO mode 0.
SCL0		I/O	Serial bus interface clock I/O data at I^2C mode 0. Open-drain output pin by programmable
P82	1	I/O	Port 82: I/O port
TXD		Output	Serial send data (UART) Open-drain output pin by programmable
P83	1	I/O	Port 83: I/O port
RXD		Input	Serial recive data (UART) Open-drain output pin by programmable
P84	1	I/O	Port 84: I/O port
SDA1		I/O	Serial bus interface send/receve data at I^2C mode 1 N-ch FET open-drain output
P85	1	I/O	Port 85: I/O port
SCL1		I/O	Serial bus interface clock I/O data at I^2C mode 1 N-ch FET open-drain output
P86	1	I/O	Port 86: I/O port
SDA2		I/O	Serial bus interface send/receve data at I^2C mode 2 N-ch FET open-drain output
P87	1	I/O	Port 87: I/O port
SCL2		I/O	Serial bus interface clock I/O data at I^2C mode 2 N-ch FET open-drain output

Table 2.2.3 Pin names and functions (3/3)

Pin name	Number of pins	I/O	Functions
ALE	1	Output	Address latch enable Can be disabled to reduce noise.
$\overline{NMI}$	1	Input	Non-maskable interrupt request pin: Interrupt request pin with programmable falling edge level or with both edge levels programmable
AM0 to 1	2	Input	Address mode: The Vcc pin should be connected.
EMU0/EMU1	1	Output	Test pins: open pins
$\overline{RESET}$	1	Input	Reset: initializes TMP91CW18A. (with pull-up resistor)
VREFH	1	Input	Pin for reference voltage input to AD converter (H)
VREFL	1	Input	Pin for reference voltage input to AD converter (L)
AVCC	1	I/O	Power supply pin for AD converter
AVSS	1		GND pin for AD converter (0 V)
X1/X2	2	I/O	High-frequency oscillator connection pins
DVCC	3		Power supply pins
DVSS	2		GND pins (0 V)

3. Operation

This section describes the basic components, functions and operation of the TMP91CW18A.

Notes and restrictions which apply to the various items described here are outlined in Section 7. Precautions and Restrictions at the end of this databook.

3.1 CPU

The TMP91CW18A incorporates a high-performance 16-bit CPU (the 900/L1 CPU). For a description of this CPU's operation, please refer to the section of this databook which describes the TLCS-900/L1 CPU.

The following sub-sections describe functions peculiar to the CPU used in the TMP91CW18A; these functions are not covered in the section devoted to the TLCS-900/L1 CPU.

3.1.1 Reset

When resetting the TMP91CW18A microcontroller, ensure that the power supply voltage is within the operating voltage range, and that the internal high-frequency oscillator has stabilized. Then hold the RESET input Low for at least 10 system clocks (ten states: 80 μs at 4 MHz).

When the Reset has been accepted, the CPU performs the following:

- Sets the Program Counter (PC) as follows in accordance with the Reset Vector stored at address FFFF00H to FFFF02H:

  PC<0:7> ← data in location FFFF00H
  PC<8:15> ← data in location FFFF01H
  PC<16:23> ← data in location FFFF02H

- Sets the Stack Pointer (XSP) to 100H.
- Sets bits <IFF0:2> of the Status Register (SR) to 111 (thereby setting the Interrupt Level Mask Register to level 7).
- Sets the <MAX> bit of the Status Register to 1 (MAX mode).

  Note: As this product does not support MIN mode, do not write a 0 to the <MAX> bit.

- Clears bits <RFP0:2> of the Status register to 000 (thereby selecting register bank 0).

When the Reset is cleared, the CPU starts executing instructions according to the program counter settings. CPU internal registers not mentioned above do not change when the Reset is cleared.
When the Reset is accepted, the CPU sets internal I/O, ports and other pins as follows.

- Initializes the internal I/O registers.
- Sets the port pins, including the pins that also act as internal I/O, to General-purpose input or Output port mode.
- Sets the ALE pin to High-Z.

Note: By resetting, register in CPU except program counter (PC),status register (SR), and stack
Pointer (XSP) and the data in internal RAM are not changed.

Figure 3.1.1 shows the timing of a Reset for the TMP91CW18A.

3.2 Memory Map

Figure 3.2.1 is a memory map of the TMP91CW18A.

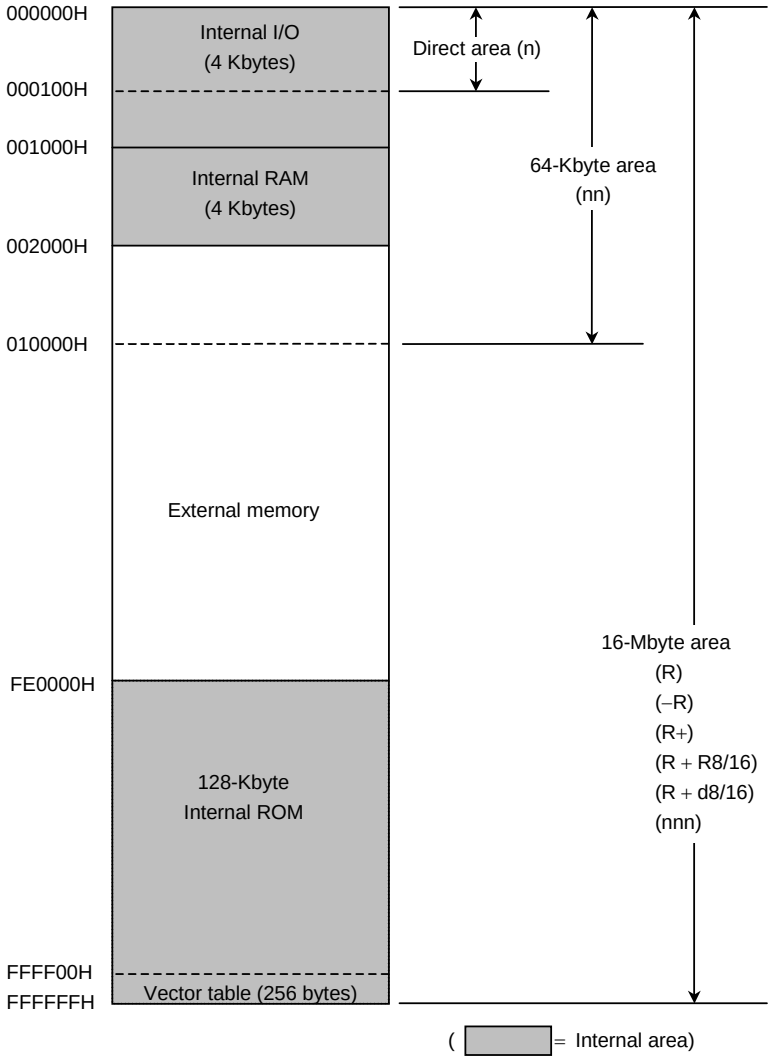


Figure 3.2.1 Memory map

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Supply Voltage	Vcc	−0.5 to 6.5	V
Input Voltage	VIN	−0.5 to Vcc + 0.5	V
Output Current	IOL	2	mA
Output Current	IOH	−2	mA
Output Current (total)	ΣIOL	80	mA
Output Current (total)	ΣIOH	−80	mA
Power Dissipation (Ta = 70°C)	PD	600	mW
Soldering Temperature (10 s)	TSOLDER	260	°C
Storage Temperature	TSTG	−65 to 150	°C
Operating Temperature	TOPR	−30 to 70	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

4.2 DC Characteristics (1/2)

Parameter		Symbol	Condition	Min	Typ. (Note1)	Max	Unit
Power Supply Voltage (Avcc = DVcc, Avss = DVss = 0 V)		VCC	fc = 8 to 25 MHz	4.5		5.5	V
Input Low Voltage	P00 to P17 (AD0 to 15)	VIL	Vcc ≥ 4.5V	−0.3		0.8	V
	P20 to P87	VIL1	Vcc = 4.5 to 5.5 V			0.3 Vcc	
	$\overline{\text{RESET}}$, $\overline{\text{NMI}}$	VIL2				0.25 Vcc	
	AM0, 1	VIL3				0.3	
	X1	VIL4				0.2 Vcc	
	P00 to P17 (AD0 to 15)	VIH	Vcc = 4.5 to 5.5 V	0.7 Vcc		Vcc + 0.3	
	P20 to P87	VIH1	Vcc = 4.5 to 5.5 V	0.7 Vcc			
	$\overline{\text{RESET}}$, $\overline{\text{NMI}}$	VIH2		0.75 Vcc			
	AM0 to 1	VIH3		Vcc − 0.3			
	X1	VIH4		0.8 Vcc			
Output Low Voltage		VOL	IOL = 1.6 mA (Vcc = 4.5 to 5.5 V)			0.45	V
Output High Voltage		VOH	IOH = − 400 μA (Vcc = 5.0 V ± 10 %)	0.8Vcc			

Note: Typical values are for when Ta = 25°C and Vcc = 5.0 V uncles otherwise noted.

4.2 DC Characteristics (2/2)

Parameter	Symbol	Condition		Min	Typ. (Note 1)	Max	Unit
Input Leakage Current	ILI	$0.0 \leq V_{IN} \leq Vcc$			0.02	±1	μA
Output Leakage Current	ILO	$0.2 \leq V_{IN} \leq Vcc - 0.2$			0.05	±10	
Power Down Voltage (at STOP, RAM Back up)	VSTOP	V IL2 = 0.2 Vcc, V IH2 = 0.8 Vcc		2.0		5.5	V
$\overline{\text{RESET}}$ Pull-Up Resister	RRST	Vcc = 5 V ± 10%		40		200	kΩ
Pin Capacitance	CIO	fc = 1 MHz				10	pF
Schmitt Width $\overline{\text{RESET}}$, $\overline{\text{NMI}}$	VTH			0.4	1.0		V
Programmable Pull-Up Resistor	RKH	Vcc = 5 V ± 10%		40		200	kΩ
NORMAL (Note 2)	Icc	Vcc = 5 V ± 10 % fc = 25 MHz (Typ. Vcc = 5.0 V)			20.5	35.0	mA
IDLE2					8.6	13.0	
IDLE1					3.5	7.0	
STOP		Ta ≤ 70°C	Vcc = 4.5 to 5.5 V		0.2	20	μA

Note 1: Typical values are for when Ta = 25°C and Vcc = 5.0 V unless otherwise noted.

Note 2: Icc measurement conditions (NORMAL):
All functions are operational; output pins are open and input pins are fixed.

4.3 AC Characteristics

(1) Vcc = 5.0 V ± 10 %

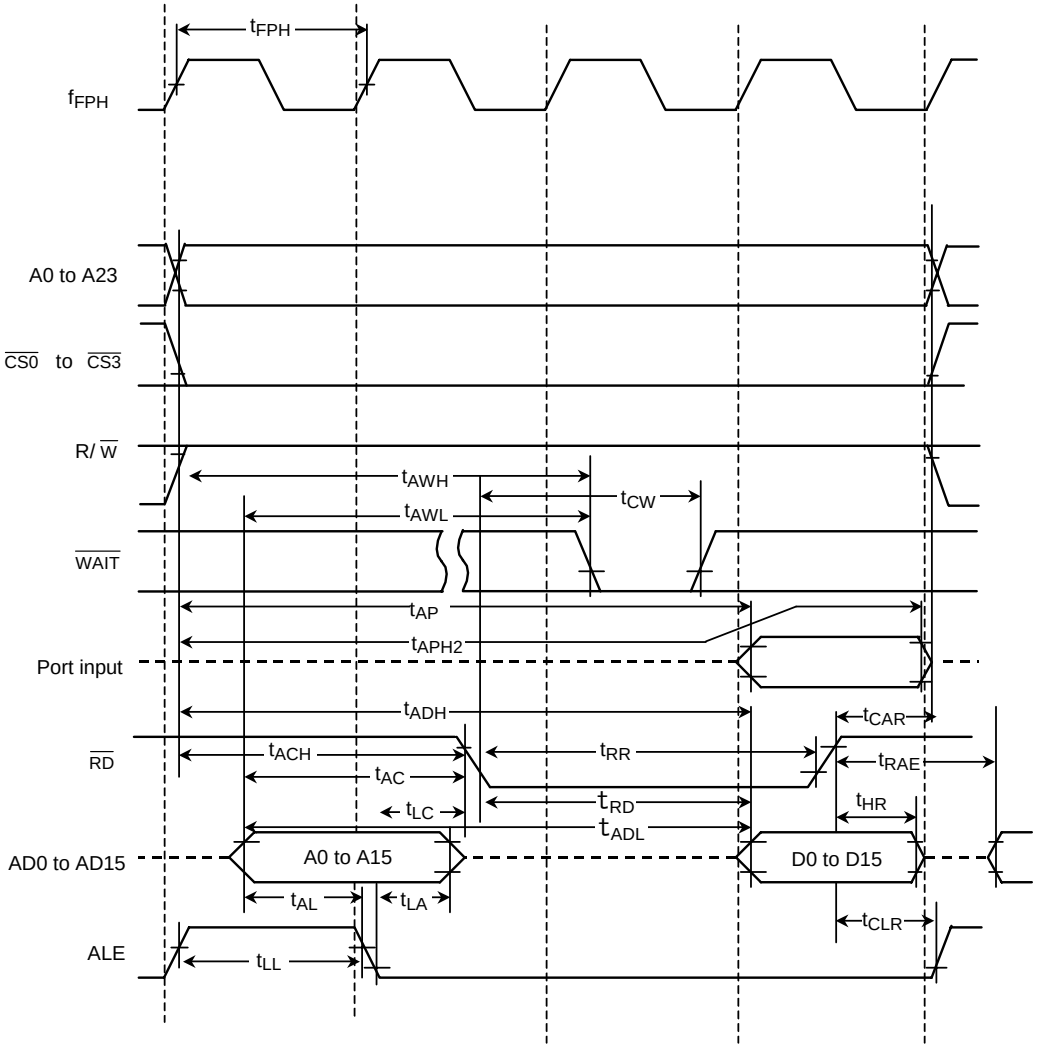
No.	Parameter	Symbol	Variable		f_{FPH} = 25 MHz		Unit
			Min	Max	Min	Max	
1	f_{FPH} Period (= x)	t_{FPH}	40	31250	40		ns
2	A0 to A15 Vaild → ALE Fall	t_{AL}	0.5x – 15		5		ns
3	ALE Fall → A0 to A15 Hold	t_{LA}	0.5x – 15		5		ns
4	ALE High Width	t_{LL}	x – 20		20		ns
5	ALE Fall → $\overline{RD}$ / $\overline{WR}$ Fall	t_{LC}	0.5x – 20		0		ns
6	$\overline{RD}$ Rise → ALE Rise	t_{CLR}	0.5x – 15		5		ns
7	$\overline{WR}$ Rise → ALE Rise	t_{CLW}	x – 15		25		ns
8	A0 to A15 Valid → $\overline{RD}$ / $\overline{WR}$ Fall	t_{ACL}	x – 25		15		ns
9	A0 to A23 Valid → $\overline{RD}$ / $\overline{WR}$ Fall	t_{ACH}	1.5x – 50		10		ns
10	$\overline{RD}$ Rise → A0 to A23 Hold	t_{CAR}	0.5x – 20		0		ns
11	$\overline{WR}$ Rise → A0 to A23 Hold	t_{CAW}	x – 20		20		ns
12	A0 to A15 Valid → D0 to D15 Input	t_{ADL}		3.0x – 45		75	ns
13	A0 to A23 Valid → D0 to D15 Input	t_{ADH}		3.5x – 35		105	ns
14	$\overline{RD}$ Fall → D0 to D15 Input	t_{RD}		2.0x – 40		40	ns
15	$\overline{RD}$ Low Width	t_{RR}	2.0x – 20		60		ns
16	$\overline{RD}$ Rise → D0 to A15 Hold	t_{HR}	0		0		ns
17	$\overline{RD}$ Rise → A0 to A15 Output	t_{RAE}	x – 15		25		ns
18	$\overline{WR}$ Low Width	t_{WW}	1.5x – 20		40		ns
19	D0 to D15 Valid → $\overline{WR}$ Rise	t_{DW}	1.5x – 50		10		ns
20	$\overline{WR}$ Rise → D0 to D15 Hold	t_{WD}	x – 15		25		ns
21	A0 to A23 Valid → $\overline{WAIT}$ Input (1 wait +n Mode)	t_{AWH}		3.5x – 90		50	ns
22	A0 to A15 Valid → $\overline{WAIT}$ Input (1 wait +n Mode)	t_{AWL}		3.0x – 80		40	ns
23	$\overline{RD}$ / $\overline{WR}$ Fall → $\overline{WAIT}$ Hold (1 wait +n Mode)	t_{CW}	2.0x + 0		80		ns
24	A0 to A23 Valid → Port Input	t_{APH}		3.5x – 120		20	ns
25	A0 to A23 Valid → Port Hold	t_{APH2}	3.5x		140		ns
26	A0 to A23 Valid → Port Valid	t_{AP}		3.5x + 100		319	ns

AC measuring conditions

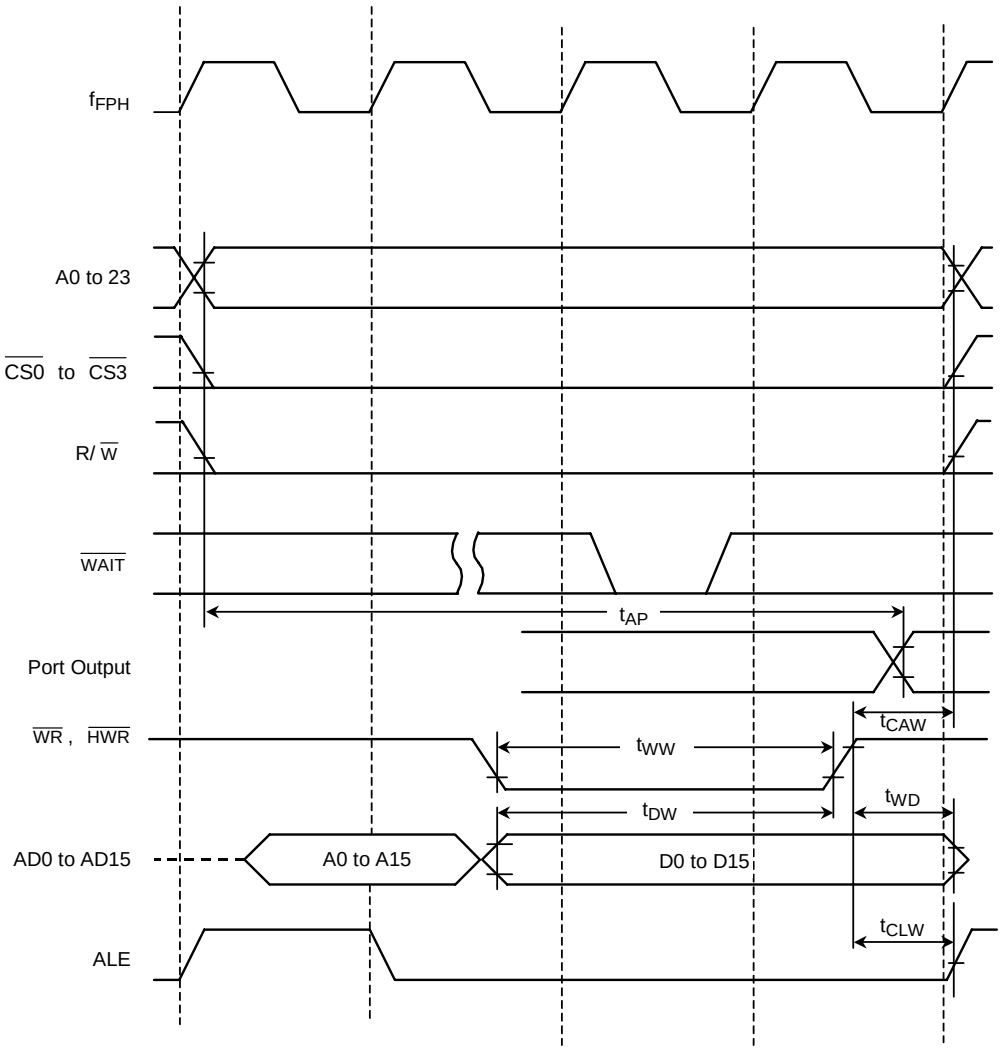
- Output level: High = 0.7 Vcc, Low = 0.3 Vcc, CL = 50 pF
- Input level: High = 0.9 Vcc, Low = 0.1 Vcc

(2) Vcc = 5.0 V ± 10 %

1. Raed cycle



2. Write cycle



4.4 AD Conversion Characteristics

AVcc = Vcc, AVss = Vss

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog Input Voltage Range(+)	VREFH	V_{CC} = 5 V ± 10 %	V_{CC} − 1.5 V	Vcc	Vcc	V
Analog Input Voltage Range(−)	VREFL	V_{CC} = 5 V ± 10 %	V_{SS}	Vss	Vss + 0.2 V	
Analog Input Voltage Range	VAIN		V_{REFL}		V_{REFH}	
Analog Input Voltage Range <VREFON> = 1	IREF (VREFL = 0 V)	V_{CC} = 5 V ± 10 %		1.44	2.00	mA
<VREFON> = 0		V_{CC} = 2.7 V to 5.5 V		0.02	5.0	μA
Error (Not including quantizing erros)	−	V_{CC} = 5 V ± 10 %		±1.0	±4.0	LSB

Note 1: 1 LSB = (VREFH − VREFL)/1024 [V]

Note 2: The operation above is guaranteed for $f_{FPH} \geq 4$ MHz.

Note 3: The value for I_{CC} includes the current which flows through the AV_{CC} pin.

4.5 Event Counter (TA0IN, TA4IN, TB0IN0, TB0IN1, TB1IN0, TB1IN1)

Parameter	Symbol	Variable		25 MHz		Unit
		Min	Max	Min	Max	
Clock Perild	t_{VCK}	8X + 100		420		ns
Clock Low Level Width	t_{VCKL}	4X + 40		200		ns
Clock High Level Width	t_{VCKH}	4X + 40		200		ns

4.6 Interrupt, Capture

(1) $\overline{NMI}$, INT0 to INT4 Interrupts

Parameter	Symbol	Variable		25 MHz		Unit
		Min	Max	Min	Max	
$\overline{NMI}$, INT0 to INT4 Low Level Width	t_{INTAL}	4X + 40		200		ns
$\overline{NMI}$, INT0 to INT4 High Level Width	t_{INTAH}	4X + 40		200		ns

(2) INT5 to INT6 Interrupts, Capture

The INT5 to INT6 input width depends on the system clock and prescaler clock settings.

System Clock Selected <SYSCK>	Prescaler Clock Selected <PRCK1:0>	t_{INTBL} (INT5 to INT6 Low level Width)		t_{INTBH} (INT5 to INT6 High Level Width)		Unit
		Variable	f_{FPH} = 25 MHz	Variable	f_{FPH} = 25 MHz	
		Min	Max	Min	Max	
0 (fc)	00 (f_{FPH})	8X + 100	420	8X + 100	420	ns
	10 (fc/16)	128Xc + 0.1	5.22	128Xc + 0.1	5.22	μs

Note: Xc = Perild of clock fc

4.7 SCOUT Pin AC Characteristics

Parameter	Symbol	Variable		25 MHz		Condition	Unit
		Min	Max	Min	Max		
Low Level Width	t_{SCH}	0.5T –15		5		Vcc = 5 V ± 10%	ns
High Level Width	t_{SCL}	0.5T – 15		5		Vcc = 5 V ± 10%	ns

Note: T = Period of SCOUT