Low Voltage/Low power

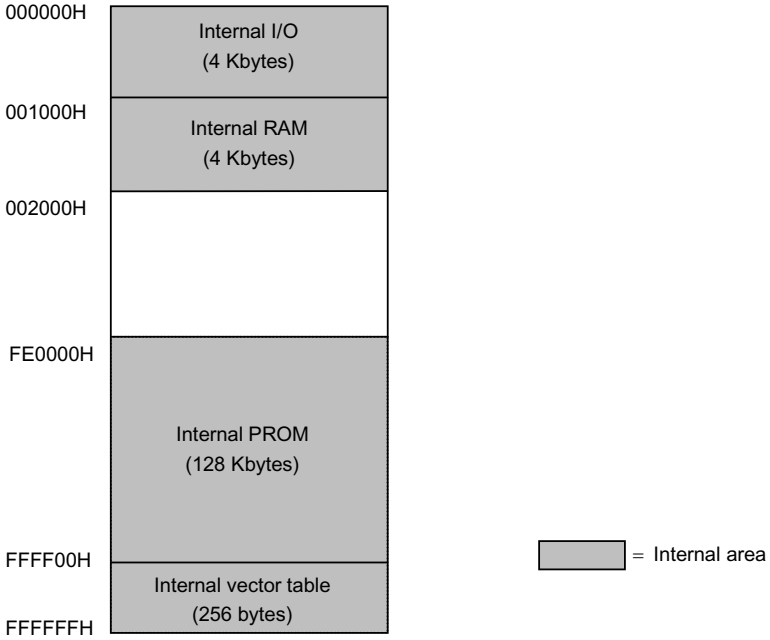
CMOS 16-Bit Microcontrollers

TMP91PW18AF

1. Outline and Device Characteristics

TMP91PW18A is OTP type MCU which 128-Kbyte One-time PROM. Using the adapter-socket, you can write and verify the data for TMP91PW18A. TMP91PW18A has the same pin-assignment with TMP91CW18A (Mask ROM type).

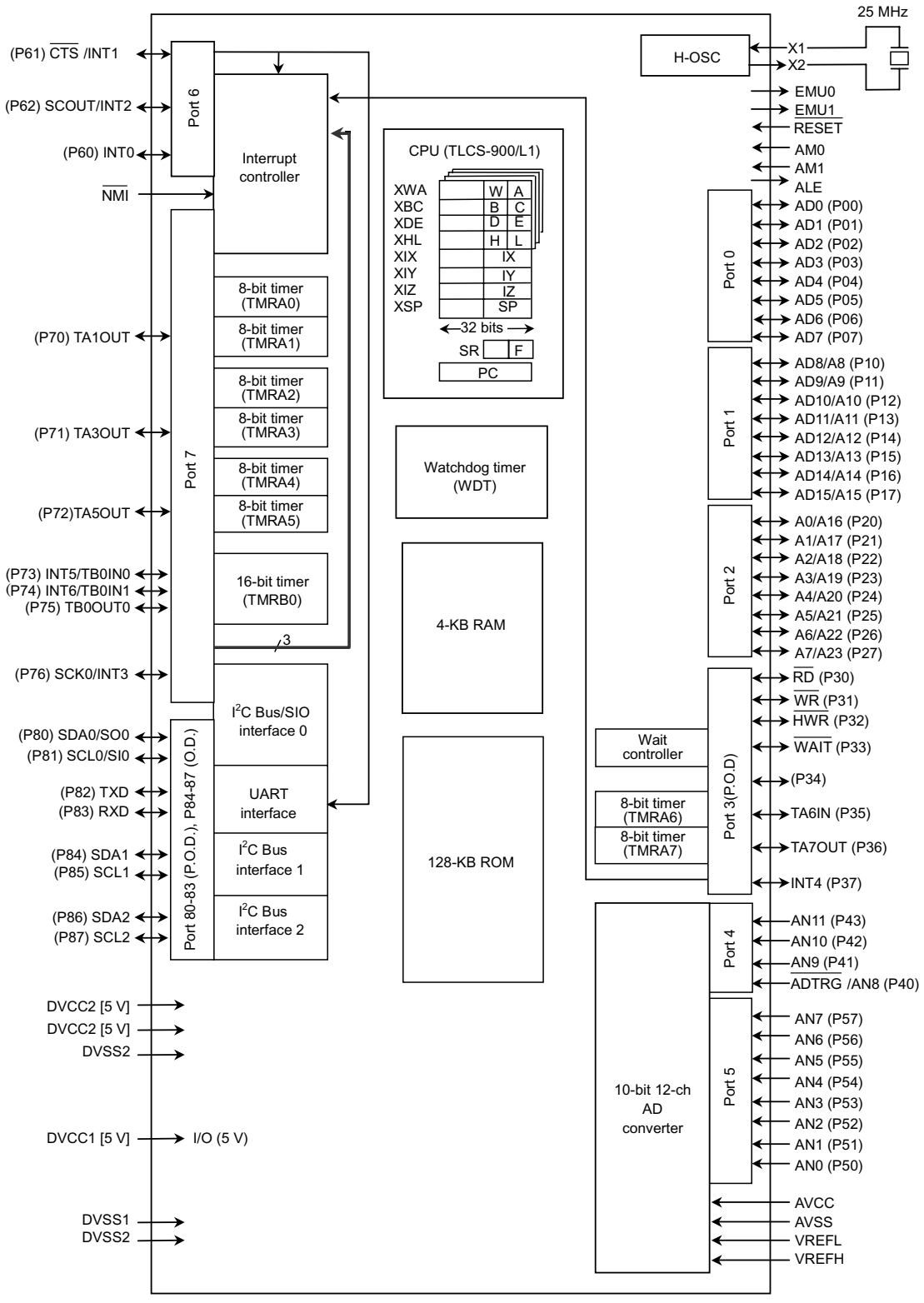
Writing the program to Built-in PROM, TMP91PW18A operates as the same way with TMP91CW18A.



Momery map of TMP91PW18A

Product No.	ROM	RAM	Packege	Adaptor socket
TMP91PW18AF	OTP 128 Kbytes	4 Kbytes	80-QFP	BM11179

000707EBP1



( ): Initial function after reset

Figure 1.1 Block diagram of TMP91PW18A

2. Pin Assignment and Functions

This section shows TMP91PW18A pin assignment, and the names and an outline of the functions of the input/output pins.

2.1 Pin Assignment Diagram

Figure 2.1.1 is a pin assignment diagram for TMP91PW18A.

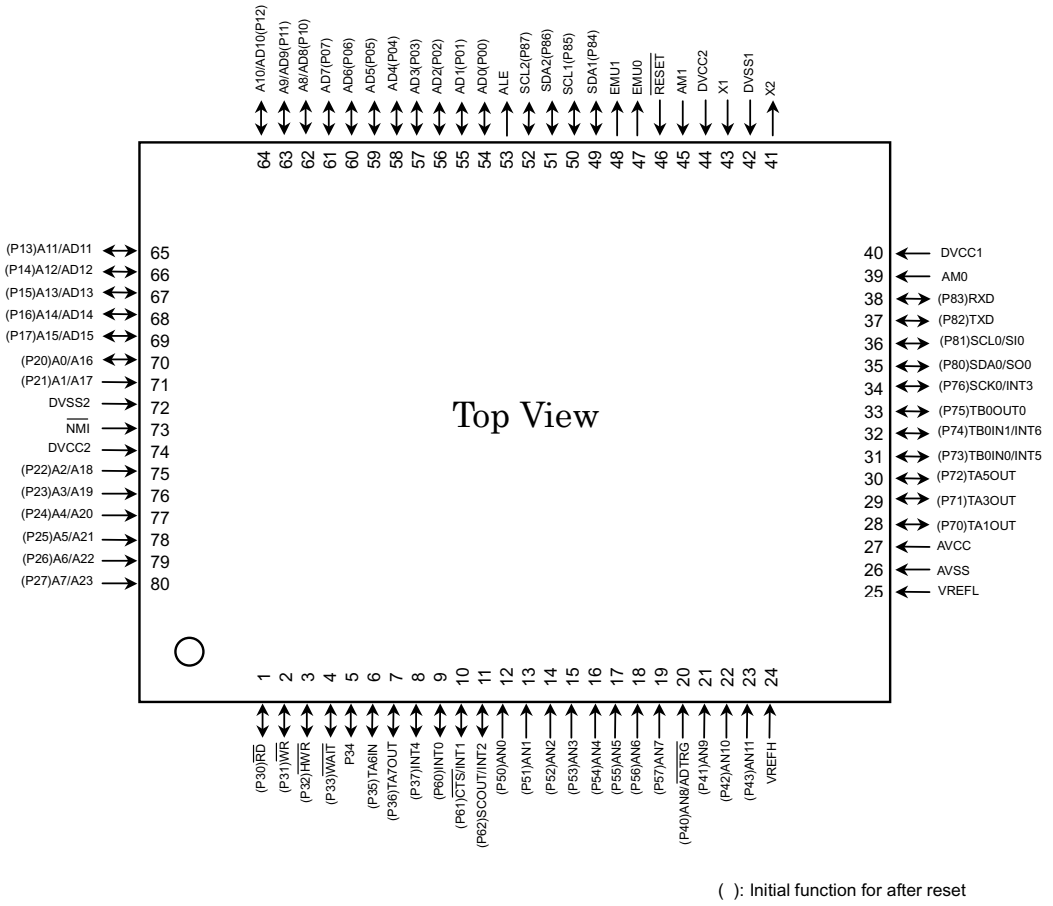


Figure 2.1.1 Pin assignment diagram (80-pin QFP)

2.2 Pin Names and Functions

The names of the input/output pins and their functions are described below.

Table 2.2.1 Pin names and functions (1/3)

Pin name	Number of pins	I/O	Functions
P00 to P07 AD0 to AD7	8	I/O Tri-state	Port 0: I/O port that allows I/O to be selected at the bit level Address and data (lower): Bits 0 to 7 of address and data bus
P10 to P17 AD8 to AD15 A8 to A15	8	I/O Tri-state Output	Port 1: I/O port that allows I/O to be selected at the bit level Address and data (upper): Bits 8 to 15 for address and data bus Address: Bits 8 to 15 of address bus
P20 to P27 A0 to A7 A16 to A23	8	I/O Output Output	Port 2: I/O port that allows I/O to be selected at the bit level Address: Bits 0 to 7 of address bus Address: Bits 16 to 23 of address bus
P30 $\overline{RD}$	1	I/O Output	Port 30: Output port By setting (P3<P30> = 0, P3FC<P30FC> = 1), $\overline{RD}$ signal is generated during reading internal areas. Read: Strobe signal for reading external memory Open-drain output pin by programmable
P31 $\overline{WR}$	1	I/O Output	Port 31: Output port Write: Strobe signal for writing data to pins AD0 to AD7 Open-drain output pin by programmable
P32 $\overline{HWR}$	1	I/O Output	Port 32: I/O port (with pull-up resistor) High Write: Strobe signal for writing data to pins AD8 to AD15 Open-drain output pin by programmable
P33 $\overline{WAIT}$	1	I/O Input	Port 33: I/O port (with pull-up resistor) Wait: Pin used to request CPU bus wait Open-drain output pin by programmable
P34	1	I/O	Port 34: I/O port Open-drain output pin by programmable
P35 TA6IN	1	I/O Input	Port 35: I/O port Timer A6 input Open-drain output pin by programmable
P36 TA7OUT	1	I/O Output	Port 36: I/O port Timer A7 output Open-drain output pin by programmable
P37 INT4	1	I/O Input	Port 37: I/O port Interrupt request pin 4: Interrupt request pin with programmable rising edge/falling edge levels Open-drain output pin by programmable
P40 to P43 AN8 to AN11 $\overline{ADTRG}$	4	Input Input Input	Port 40: Pin used to input port Analog input: Pin used to input to AD converte AD Trigger: Signal used to request start of AD conversion
P50 to P57 AN0 to AN7	8	Input Input	Port 5: Pin used to input port Analog input: Pin used to input to AD converter
P60 INT0	1	I/O Input	Port 60: I/O port Interrupt request pin 0: Interrupt request pin with programmable rising edge/falling edge levels
P61 $\overline{CTS}$ INT1	1	I/O Input Input	Port 61: I/O port Serial data send enable (Clear to Send) Interrupt request pin 1: Interrupt request pin with programmable rising edge/falling edge levels
P62 SCOUT INT2	1	I/O Output Input	Port 62: I/O port System clock output: outputs f_{FPH} or fs clock Interrupt request pin 2: Interrupt request pin with programmable rising edge/falling edge levels

Table 2.2.2 Pin names and functions (2/3)

Pin name	Number of pins	I/O	Functions
P70 TA1OUT	1	I/O Output	Port 70: I/O port Timer A1 output
P71 TA3OUT	1	I/O Output	Port 71: I/O port Timer A3 output
P72 TA5OUT	1	I/O Output	Port 72: I/O port Timer A5 output
P73 TB0IN0 INT5	1	I/O Input Input	Port 73: I/O port Timer B0 input 0 Interrupt request pin 5: Interrupt request pin with programmable rising edge/falling edge levels
P74 TB0IN1 INT6	1	I/O Input Input	Port 74: I/O port Timer B0 input 1 Interrupt request pin 6: Interrupt request pin with programmable rising edge/falling edge levels
P75 TB0OUT0	1	I/O Output	Port 75: I/O port Timer B0 output 0
P76 SCK0 INT3	1	I/O I/O Input	Port 76: I/O port Serial clock I/O 0 Interrupt request pin 3: Interrupt request pin with programmable rising edge/falling edge levels
P80 SO0 SDA0	1	I/O Output I/O	Port 80: I/O port Serial bus interface send data at SIO mode 0. Serial bus interface send/receve data at I^2C mode 0. Open-drain output pin by programmable
P81 SI0 SCL0	1	I/O Input I/O	Port 81: I/O port Serial bus interface receve data at SIO mode 0. Serial bus interface clock I/O data at I^2C mode 0. Open-drain output pin by programmable
P82 TXD	1	I/O Output	Port 82: I/O port Serial send data (UART) Open-drain output pin by programmable
P83 RXD	1	I/O Input	Port 83: I/O port Serial recive data (UART) Open-drain output pin by programmable
P84 SDA1	1	I/O I/O	Port 84: I/O port Serial bus interface send/receve data at I^2C mode 1 N-ch FET open-drain output
P85 SCL1	1	I/O I/O	Port 85: I/O port Serial bus interface clock I/O data at I^2C mode 1 N-ch FET open-drain output
P86 SDA2	1	I/O I/O	Port 86: I/O port Serial bus interface send/receve data at I^2C mode 2 N-ch FET open-drain output
P87 SCL2	1	I/O I/O	Port 87: I/O port Serial bus interface clock I/O data at I^2C mode 2 N-ch FET open-drain output

Table 2.2.3 Pin names and functions (3/3)

Pin name	Number of pins	I/O	Functions
ALE	1	Output	Address latch enable can be disabled to reduce noise.
$\overline{NMI}$	1	Input	Non-maskable interrupt request pin: Interrupt request pin with programmable falling edge level or with both edge levels programmable
AM0 to 1	2	Input	Address mode: The Vcc pin should be connected.
EMU0/EMU1	1	Output	Test pins: Open pins
$\overline{RESET}$	1	Input	Reset: Initializes TMP91CW18. (with pull-up resistor)
VREFH	1	Input	Pin for reference voltage input to AD converter (H)
VREFL	1	Input	Pin for reference voltage input to AD converter (L)
AVCC	1		Power supply pin for AD converter
AVSS	1		GND pin for AD converter (0 V)
X1/X2	2	I/O	High-frequency oscillator connection pins
DVCC	3		Power supply pins
DVSS	2		GND pins (0 V)

2.3 PROM Mode

Table 2.3.1 Names and functions of PROM mode

Pin function	Pin number	I/O	Function	Pin name (MCU mode)
A7 to A0	8	Input	Program memory address input	P27 to P20
A15 to A8	8	Input		P17 to P10
A16	1	Input		P33
D7 to D0	8	Input/Output	Program memory data I/O	P07 to P00
$\overline{CE}$	1	Input	Chip enable input	P32
$\overline{OE}$	1	Input	Output control input	P30
$\overline{PGM}$	1	Input	Program control input	P31
VPP	1	Power supply	12.75 V/5 V (Power supply of program)	AM1
VCC	4	Power supply	6.25 V/5 V	DVCC, AVCC
VSS	4	Power supply	0V	DVSS, AVSS
P34	1	Input	Fix to low level (security pin)	
$\overline{RESET}$	1	Input	Fix to low level (PROM mode)	
AM0	1	Input		
ALE	1	Output	Open	
X1	1	Input	Crystal	
X2	1	Output		
P43 to P41, P37 to P35, P75 to P70	12	Input	Fix to high level	
P40 P57 to P50 P62 to P60 P87 to P80 VREFH VREFL $\overline{NMI}$, EMU1, 0	51	Input/Output	Open	

3. Operation

This section describes in blocks the functions and basic operations of TMP91PW18A.

TMP91PW18A has PROM in place of the mask ROM which is included in the TMP91CW18A.

The other configuration and functions are the same as the TMP91CW18A.

Regarding the function of the TMP91PW18A, which is not described herein, see the TMP91CW18A.

The TMP91PW18A has two operational modes: MCU mode and PROM mode.

3.1 MCU Mode

(1) Mode-setting and function

The MCU mode is set by driving AM1 pin and AM0 pin. In the MCU mode, the operation is same as TMP91CW18A.

3.2 Memory Map

Figure 3.2.1, 2 are memory map of TMP91PW18A.

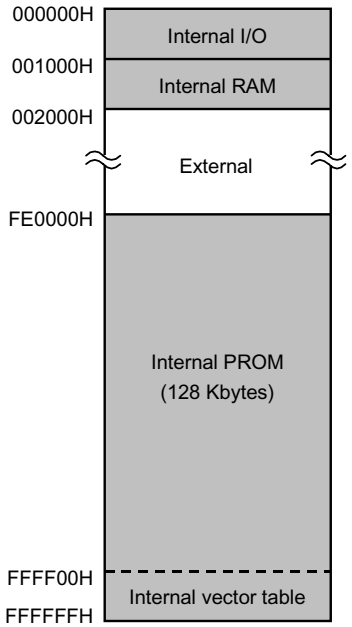


Figure 3.2.1 Memory map in MCU mode

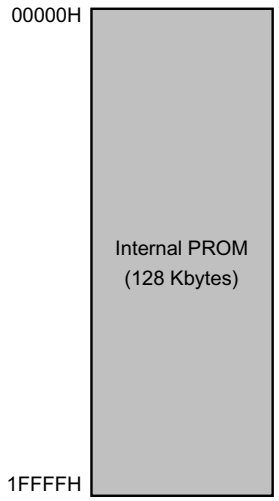


Figure 3.2.2 Memory map in PROM mode

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Supply Voltage	Vcc	−0.5 to 6.5	V
Input Voltage	VIN	−0.5 to Vcc + 0.5	V
Output Current	IOL	2	mA
Output Current	IOH	−2	mA
Output Current (total)	ΣIOL	80	mA
Output Current (total)	ΣIOH	−80	mA
Power Dissipation (Ta = 70°C)	PD	600	mW
Soldering Temperature (10 s)	TSOLDER	260	°C
Storage Temperature	TSTG	−65 to 150	°C
Operating Temperature	TOPR	−30 to 70	°C

4.2 DC Characteristics (1/2)

Parameter		Symbol	Condition	Min	Typ. (Note)	Max	Unit
Power Supply Voltage (Avcc = DVcc, Avss = DVss = 0 V)		VCC	fc = 8 to 25 MHz	4.5		5.5	V
Input Low Voltage	P00 to P17 (AD0 to 15)	VIL	Vcc ≥ 4.5 V	−0.3		0.8	V
	P20 to P87	VIL1	Vcc = 4.5 to 5.5 V			0.3 Vcc	
	$\overline{\text{RESET}}$, $\overline{\text{NMI}}$	VIL2				0.25 Vcc	
	AM0, 1	VIL3				0.3	
	X1	VIL4				0.2 Vcc	
	P00 to P17 (AD0 to 15)	VIH	Vcc = 4.5 to 5.5 V	0.7 Vcc		Vcc + 0.3	
	P20 to P87	VIH1	Vcc = 4.5 to 5.5 V	0.7 Vcc			
	$\overline{\text{RESET}}$, $\overline{\text{NMI}}$	VIH2		0.75 Vcc			
	AM0 to 1	VIH3		Vcc − 0.3			
	X1	VIH4		0.8 Vcc			
Output Low Voltage		VOL	IOL = 1.6 mA (Vcc = 4.5 to 5.5 V)			0.45	V
Output High Voltage		VOH	IOH = − 400 μA (Vcc = 5.0 V ± 10 %)	0.8Vcc			

Note: Typical values are for when Ta = 25°C and Vcc = 5.0 V uncles otherwise noted.

4.2 DC Characteristics (2/2)

Parameter	Symbol	Condition		Min	Typ. (Note 1)	Max	Unit
Input Leakage Current	ILI	$0.0 \leq V_{IN} \leq Vcc$			0.02	±5	μA
Output Leakage Current	ILO	$0.2 \leq V_{IN} \leq Vcc - 0.2$			0.05	±10	
Power Down Voltage (at STOP, RAM Back up)	VSTOP	V IL2 = 0.2 Vcc, V IH2 = 0.8 Vcc		2.0		5.5	V
$\overline{\text{RESET}}$ Pull-up Resistor	RRST	Vcc = 5 V ± 10%		40		200	kΩ
Pin Capacitance	CIO	fc = 1 MHz				10	pF
Schmitt Width $\overline{\text{RESET}}$, $\overline{\text{NMI}}$	VTH			0.4	1.0		V
Programmable Pull-up Resistor	RKH	Vcc = 5 V ± 10%		40		200	kΩ
NORMAL (Note 2)	Icc	Vcc = 5 V ± 10 %			23.5	35.0	mA
IDLE2		fc = 25 MHz			9.5	15.0	
IDLE1		(Typ. Vcc = 5.0 V)			4.4	9.0	
STOP		Ta ≤ 70°C	Vcc = 4.5 to 5.5 V		0.2	20	μA

Note 1: Typical values are for when Ta = 25°C and Vcc = 5.0 V unless otherwise noted.

Note 2: Icc measurement conditions (NORMAL):
All functions are operational; output pins are open and input pins are fixed.

4.3 AC Characteristics

(1) Vcc = 5.0 V ± 10 %

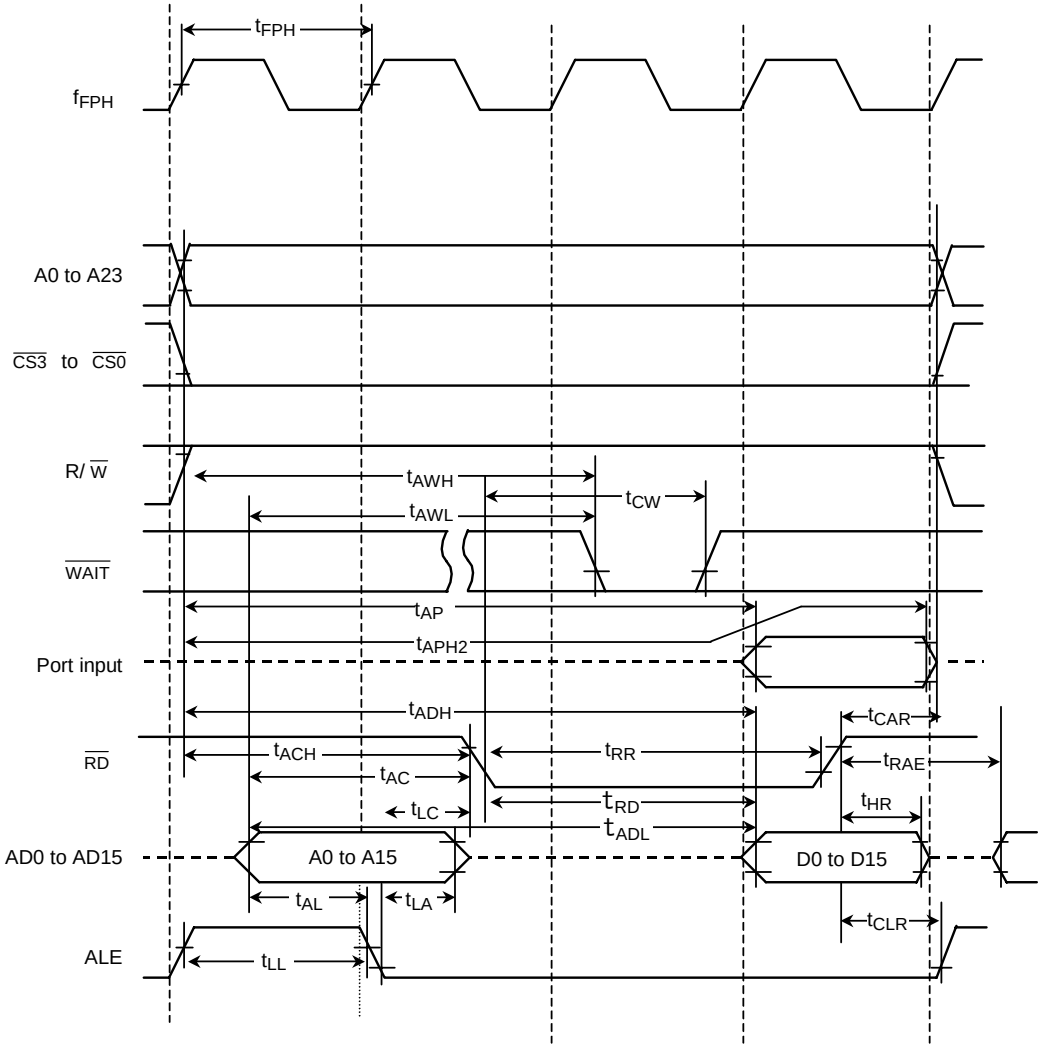
No.	Parameter	Symbol	Variable		f_{FPH} = 25 MHz		Unit
			Min	Max	Min	Max	
1	f_{FPH} Period (= x)	t_{FPH}	40	31250	40		ns
2	A0 to A15 Vaild → ALE Fall	t_{AL}	0.5x – 15		5		ns
3	ALE Fall → A0 to A15 Hold	t_{LA}	0.5x – 15		5		ns
4	ALE High Width	t_{LL}	x – 20		20		ns
5	ALE Fall → $\overline{RD}$ / $\overline{WR}$ Fall	t_{LC}	0.5x – 20		0		ns
6	$\overline{RD}$ Rise → ALE Rise	t_{CLR}	0.5x – 15		5		ns
7	$\overline{WR}$ Rise → ALE Rise	t_{CLW}	x – 15		25		ns
8	A0 to A15 Valid → $\overline{RD}$ / $\overline{WR}$ Fall	t_{ACL}	x – 25		15		ns
9	A0 to A23 Valid → $\overline{RD}$ / $\overline{WR}$ Fall	t_{ACH}	1.5x – 50		10		ns
10	$\overline{RD}$ Rise → A0 to A23 Hold	t_{CAR}	0.5x – 20		0		ns
11	$\overline{WR}$ Rise → A0 to A23 Hold	t_{CAW}	x – 20		20		ns
12	A0 to A15 Valid → D0 to D15 Input	t_{ADL}		3.0x – 45		75	ns
13	A0 to A23 Valid → D0 to D15 Input	t_{ADH}		3.5x – 35		105	ns
14	$\overline{RD}$ Fall → D0 to D15 Input	t_{RD}		2.0x – 40		40	ns
15	$\overline{RD}$ Low Width	t_{RR}	2.0x – 20		60		ns
16	$\overline{RD}$ Rise → D0 to A15 Hold	t_{HR}	0		0		ns
17	$\overline{RD}$ Rise → A0 to A15 Output	t_{RAE}	x – 15		25		ns
18	$\overline{WR}$ Low Width	t_{WW}	1.5x – 20		40		ns
19	D0 to D15 Valid → $\overline{WR}$ Rise	t_{DW}	1.5x – 50		10		ns
20	$\overline{WR}$ Rise → D0 to D15 Hold	t_{WD}	x – 15		25		ns
21	A0 to A23 Valid → $\overline{WAIT}$ Input (1 wait +n Mode)	t_{AWH}		3.5x – 90		50	ns
22	A0 to A15 Valid → $\overline{WAIT}$ Input (1 wait +n Mode)	t_{AWL}		3.0x – 80		40	ns
23	$\overline{RD}$ / $\overline{WR}$ Fall → $\overline{WAIT}$ Hold (1 wait +n Mode)	t_{CW}	2.0x + 0		80		ns
24	A0 to A23 Valid → Port Input	t_{APH}		3.5x – 120		20	ns
25	A0 to A23 Valid → Port Hold	t_{APH2}	3.5x		140		ns
26	A0 to A23 Valid → Port Valid	t_{AP}		3.5x + 100		319	ns

AC Measuring Conditions

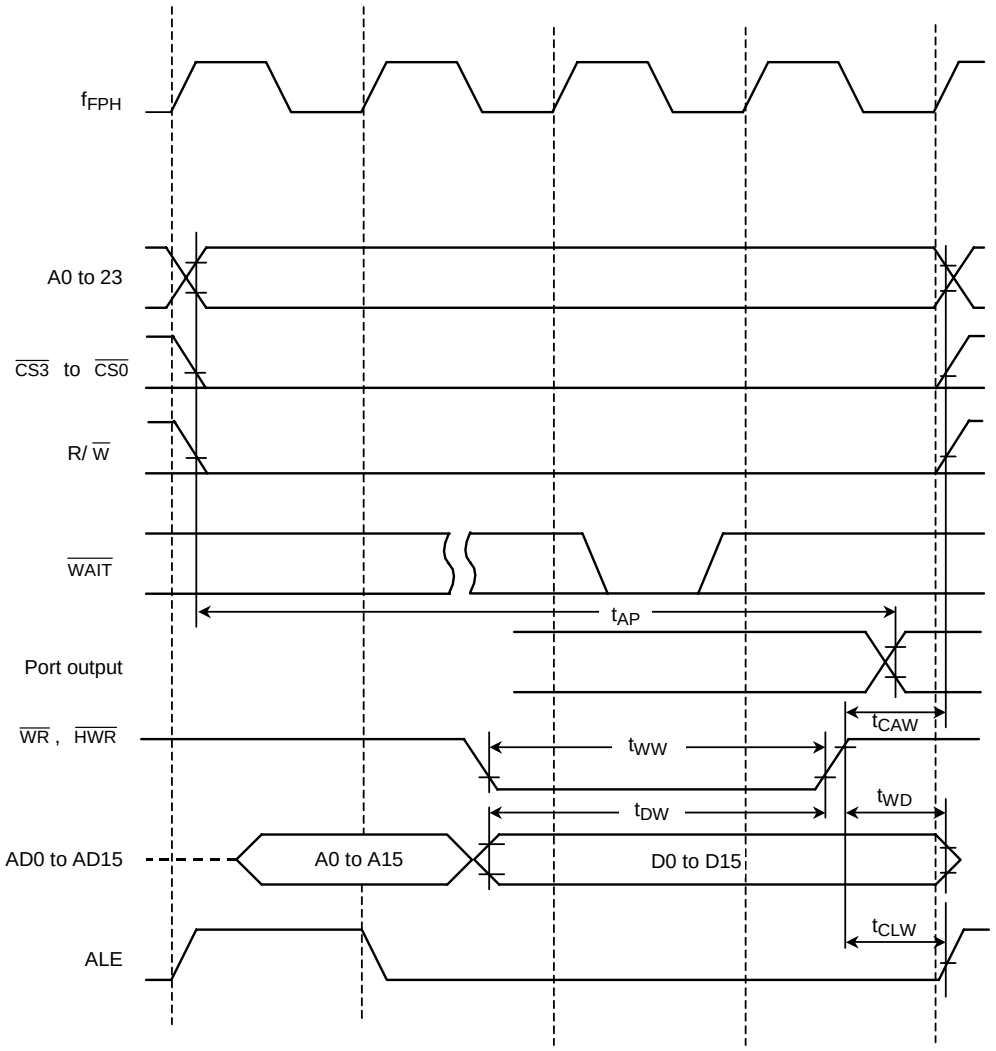
- Output level: High = 0.7 Vcc, Low = 0.3 Vcc, CL = 50 pF
- Input level: High = 0.9 Vcc, Low = 0.1 Vcc

(2) Vcc = 5.0 V ± 10 %

1. Raed cycle



.2 Write cycle



4.4 AD Conversion Characteristics

AVcc = Vcc, AVss = Vss

parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog Input Voltage Range(+)	VREFH	V_{CC} = 5 V ± 10%	V_{CC} − 1.5 V	Vcc	Vcc	V
Analog Input Voltage Range(−)	VREFL	V_{CC} = 5 V ± 10%	V_{SS}	Vss	Vss + 0.2 V	
Analog Input Voltage Range	VAIN		V_{REFL}		V_{REFH}	
Analog Input Voltage Range <VREFON> = 1	IREF (VREFL = 0 V)	V_{CC} = 5 V ± 10%		1.44	2.00	mA
<VREFON> = 0		V_{CC} = 2.7 V to 5.5 V		0.02	5.0	μA
Error (Not including quantizing erros)	−	V_{CC} = 5 V ± 10%		±1.0	±4.0	LSB

Note 1: 1 LSB = (VREFH − VREFL)/1024 [V]

Note 2: The operation above is guaranteed for $f_{FPH} \geq 4$ MHz.

Note 3: The value for I_{CC} includes the current which flows through the AV_{CC} pin.

4.5 Event Counter (TA0IN, TA4IN, TB0IN0, TB0IN1, TB1IN0, TB1IN1)

Parameter	Symbol	Variable		25 MHz		Unit
		Min	Max	Min	Max	
Clock Perild	t_{VCK}	8X + 100		420		ns
Clock Low Level Width	t_{VCKL}	4X + 40		200		ns
Clock High Level Width	t_{VCKH}	4X + 40		200		ns

4.6 Interrupt, Capture

(1) $\overline{NMI}$, INT0 to INT4 Interrupts

Parameter	Symbol	Variable		25 MHz		Unit
		Min	Max	Min	Max	
$\overline{NMI}$, INT0 to INT4 Low Level Width	t_{INTAL}	4X + 40		200		ns
$\overline{NMI}$, INT0 to INT4 High Level Width	t_{INTAH}	4X + 40		200		ns

(2) INT5 to INT6 Interrupts, Capture

The INT5 to INT6 input width depends on the system clock and prescaler clock settings.

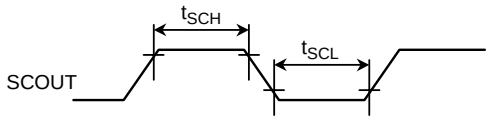
System Clock Selected <SYSCK>	Prescaler Clock Selected <PRCK1:0>	t_{INTBL} (INT5 to INT6 low level width)		t_{INTBH} (INT5 to INT6 high level width)		Unit
		Variable	f_{FPH} = 25 MHz	Variable	f_{FPH} = 25 MHz	
		Min	Max	Min	Max	
0 (fc)	00 (f_{FPH})	8X + 100	420	8X + 100	420	ns
	10 (fc/16)	128Xc + 0.1	5.22	128Xc + 0.1	5.22	μs

Note: Xc = Perild of clock fc

4.7 SCOUT Pin AC Characteristics

Parameter	Symbol	Variable		25 MHz		Condition	Unit
		Min	Max	Min	Max		
Low Level Width	t_{SCH}	0.5T − 15		5		Vcc = 5 V ± 10%	ns
High Level Width	t_{SCL}	0.5T − 15		5		Vcc = 5 V ± 10%	ns

Note: T = Period of SCOUT



4.8 Read Operation in PROM Mode

DC/AC characteristics

Ta = 25 ± 5°C Vcc = 5 V ± 10 %

Parameter	Symbol	Condition	Min	Max	Unit
V_{PP} Read Voltage	V_{PP}	−	4.5	5.5	V
Input High Voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	V_{IH1}	−	2.2	Vcc + 0.3	V
Input Low Voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	V_{IL1}	−	−0.3	0.8	V
Address to Output Delay	t_{ACC}	C_L = 50 pF	−	2.25 TCYC + α	ns

TCYC = 400 ns (10 MHz Clock)
α = 200 ns

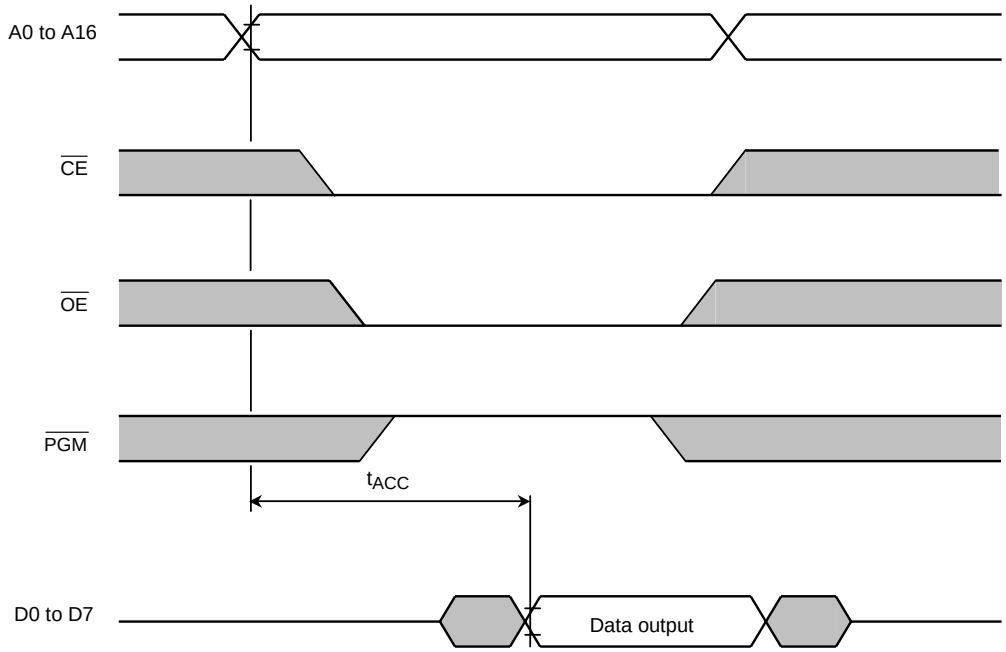
4.9 Program Operation in PROM Mode

DC/AC characteristics

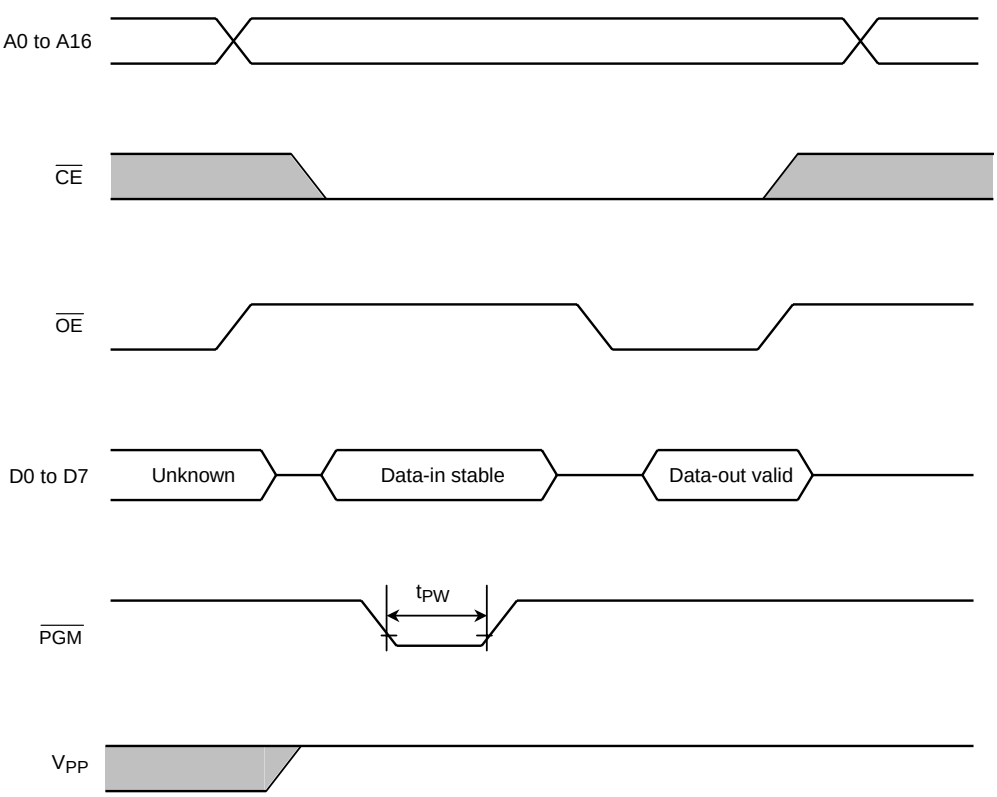
Ta = 25 ± 5°C Vcc = 6.25 V ± 0.25 V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Programing Supply Voltage	V_{PP}	−	12.50	12.75	13.00	V
Input High Voltage (D0 to D7, A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	V_{IH}	−	2.6		Vcc + 0.3	V
Input Low Voltage (D0 to D7, A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	V_{IL}	−	−0.3		0.8	V
Vcc Supply Current	I_{CC}	fc = 10 MHz	−		50	mA
V_{PP} Supply Current	I_{PP}	V_{PP} = 13.00 V	−		50	mA
$\overline{PGM}$ Program Pulse Width	t_{PW}	C_L = 50 pF	0.095	0.1	0.105	ms

4.10 Timing Chart of Read Operation in PROM Mode



4.11 Timing Chart of Program Operation in PROM Mode



Note 1: The power supply of Vpp (12.75 V) must be turned on at the same time or the later time for a power supply of Vcc and must be turned off at the same time or early time for a power supply of Vcc.

Note 2: The device suffers a damage taking out and putting in on the condition of Vpp = 12.75 V.

Note 3: The maximum spec of Vpp pin is 14.0 V. Be carefull a overshoot at the programming.