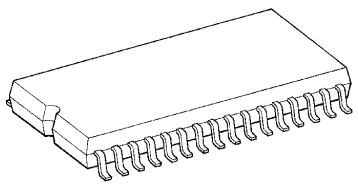
TENTATIVE TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TMPN3120A20M, TMPN3120A20U

Neuron® Chip For Distributed Intelligent Control Networks (LONWORKS®)

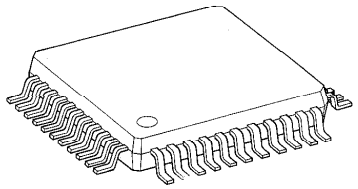
The Neuron Chip TMPN3120A20M and TMPN3120A20U provides double the performance of previous Neuron Chips. It supports a response time of 3 to 4ms across a LONWORKS Network and has double the input / output (I / O) performance of the previous Neuron Chip in terms of both response time and data transmission speed. Neuron Chips have all the built-in communications and control functions required to implement LONWORKS nodes. These nodes may then be easily integrated into highly-reliable distributed intelligent control networks. The typical functions for this chip are explained below.

TMPN3120A20M



SOP32-P-525-1.27

TMPN3120A20U



QFP44-P-1010-0.80

Weight
SOP32-P-525-1.27 : 1.1g (Typ.)
QFP44-P-1010-0.80 : 0.6g (Typ.)

FEATURES

- New features
  (In comparison with TMPN3120FE3M and TMPN3120A20M / U)
  - Enhanced communication port
  - 16-bit A / D converter
  - The package is QFP44-P-1010-0.80 (TMPN3120A20U only)

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- Main features of the 20MHz Neuron Chip
  (In comparison with the TMPN3120E1M and TMPN3120A20M / U)
  - Increased communication speed

    The maximum transmission speed has been increased two-fold.
    1.25Mbps → 2.5Mbps
  - Shortened response time

    The amount of time required from I / O input to I / O output has been greatly reduced.
    Maximum speed 7ms → 3~4ms
  - Increased IO object speed

    The execution time for all objects has been halved.
    Example) Serial I / O 9600bps
    Parallel I / O 1.2μs / byte
  - Development tool support

    The current LonBuilder® and NodeBuilder® development tools can be used to develop applications for the TMPN3120A20M and TMPN3120A20U. Updated symbol table files for the Neuron Chip firmware are available from Toshiba. If your application requires a 20MHz input clock, a utility program available from Echelon may be used to convert the programmer files.

* The conversion utilities can be obtained from the Echelon Web Site at http://www.echelon.com. * Use the 3120 programmer manufactured by Echelon when downloading to the chip.

- I / O Functions
  - Eleven programmable I / O pins.
  - Two programmable 16-bit timers and counters built in.
  - 34 different types of I / O functions to handle a wide range of input and output.
  - ROM firmware image containing pre-programmed I / O drivers, greatly simplifying application programs.
- Network functions
  - Two CPUs for communication protocol processing built in.

    The communications and application CPUs execute in parallel.
  - Equipped with a built-in LonTalk protocol which supports all seven levels of the OSI reference model with ISO.
  - The ROM firmware image contains a complete network operating system, greatly simplifying application programs.
  - Built-in twisted-pair wire transceiver with improved common mode and drive current capabilities.
  - Equipped with communications modes and communication speeds which support various types of external transceivers.
    Supports twisted-pair wire, power line, radio (RF), infrared, coaxial cables, and fiber optics.
  - Communication port transceiver modes and logical addresses stored within the EEPROM.
    Can be amended via the network.

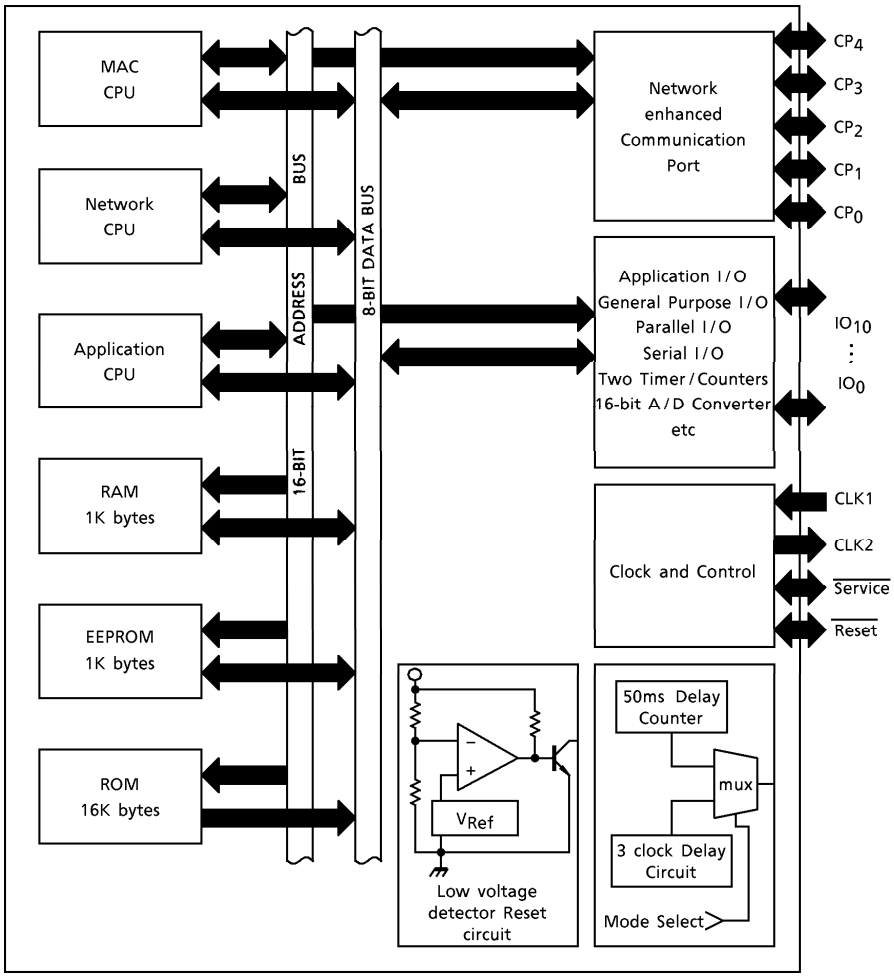
- Other functions
  - Application programs are also stored within the EEPROM.
    May be updated by downloading over the network.
  - Built-in watch-dog timer.
  - Each chip has a unique ID number.
    Effective during the logical installation of networks.
  - Low electrical consumption mode supported with a sleep mode.
  - Built in Selectable Reset time
    Prolongs the power-ON reset time for at least 50ms and keeps the operation stable during that time. The reset time can be selected 50ms delay mode or 3 clock delay mode by program after the device is in power-ON.
  - High-impedance communication port (CP0 to CP3) when powered down.
    The Communication port pins (CP0 to CP3) attain high impedance when the Neuron Chip is powered down. The eliminates the need for an external relay.
  - Built-in low-voltage detection circuit.
    Prevents incorrect operations and writing errors in the EEPROM during drops in power voltage.
    The external LVD must be use, if Neuron Chip operated at 20MHz.
    Because of the possibility of improper operation at power supply voltages below 4.5V, a low voltage detector (LVD) capability is built in to the chip to assert reset when power falls below the specified voltage.
  - Firmware version 9.
- Timing for the main I/O objects during 20MHz Neuron Chip operations

I/O MODEL	10MHz TIMING	20MHz TIMING
Parallel	2.4μs/byte	1.2μs/byte
Bitshift	1, 10 or 15kbps	2, 20 or 30kbps
Magcard	Up to 8334bps	Up to 16668bps
Magtrack1	Up to 7246bps	Up to 14492bps
Neurowire Master	1, 10 or 20kbps	2, 20 or 40kbps
Neurowire Slave	Up to 18kbps	Up to 36kbps
Serial	600, 1200, 2400 or 4800bps	1200, 2400, 4800 or 9600bps
Touch	Supported	Not supported
Frequency Output	Resolution0.4 to 51.2μs Max Range 26.21 to 3355ms	Resolution0.2 to 25.6μs Max Range 13.1 to 1678ms
Other Timer/Counter	Resolution0.2 to 25.6μs Max Range 13.1 to 1678ms	Resolution0.1 to 12.8μs Max Range 6.55 to 839ms

The specifications for the main timers during 20MHz operations are as follows :

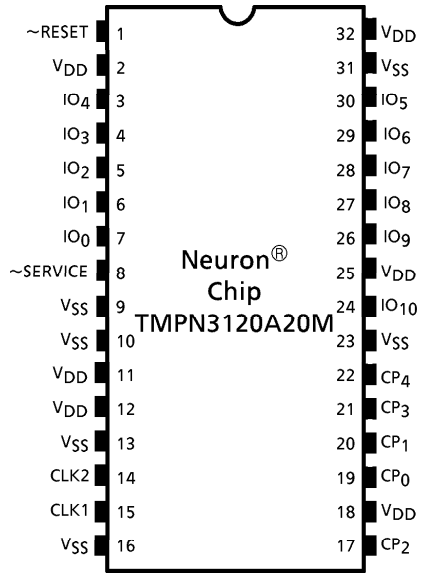
Watchdog Timer	420ms
Millisecond Timers	1 to **32000**ms
Second Timers	1 to 65000s
Delay ( ) Function	1 to 32767 counts
Get_Tick_Count ( ) Function	409.6μs per count

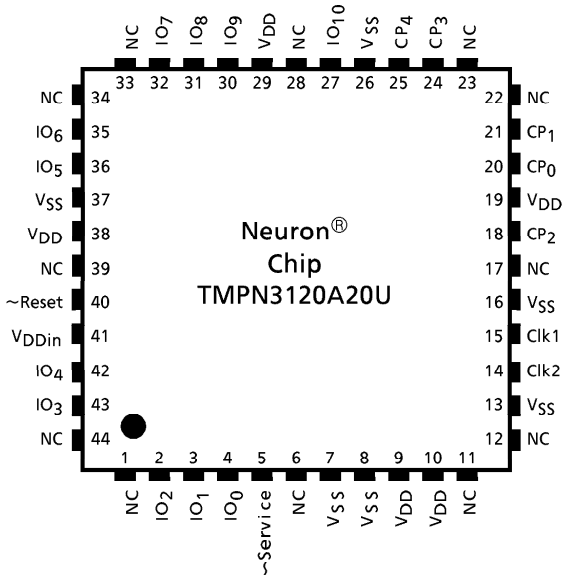
BLOCK DIAGRAM



ITEM	TMPN3120A20M	TMPN3120A20U
CPU	8-bit CPU × 3	8-bit CPU × 3
RAM	1,024 bytes	1,024 bytes
ROM	16,384 bytes	16,384 bytes
EEPROM	1,024 bytes	1,024 bytes
16-bit Timer / Counter	2	2
External Memory Interface	No	No
Package	32 pin SOP	μQFP44pin

PIN CONNECTION





PIN FUNCTION

PIN No.		PIN NAME	I/O	PIN FUNCTION
TMPN3120A20M	TMPN3120A20U			
15	15	CLK1	Input	Oscillator connection, or external clock input.
14	14	CLK2	Output	Oscillator connection. Leave open when external clock is input to CLK1.
1	40	~RESET	I/O (built-in pull-up)	Reset pin. (Active low)
8	5	~SERVICE	I/O (built-in configurable pull-up)	Service pin. Indicator output during operation.
7~4	4~2, 43	IO_0~IO_3	I/O	Large current sink capacity (20mA). General I/O port. When the A/D converter is used, pin IO_3 is reserved for connection of an external resistor.
3, 30~28	42, 36, 35, 32	IO_4~IO_7	I/O (built-in configurable pull-up)	General I/O port. One of IO_4 to IO_7 can be specified as No.1 timer/counter input. Output signal can be output to IO_0. IO_4 can be used as the No.2 timer/counter input with IO_1 as output. When using the 16-bit A/D converter, One of IO_4 to IO_6 can be used as analog input and then IO_7 must be attached the external capacitor of proper valve. When the A/D converter is used, pin IO_7 is reserved for connection of an external capacitor. One or more of pins IO_4 to IO_6 may be used as the analog input.
27, 26, 24	31, 30, 27	IO_8~IO_{10}	I/O	General I/O port. Can be used for serial communication with other device.
2, 11, 12, 18, 25, 32	9, 10, 19, 29, 38, 41	V_{DD}	Input	Power input (5.0V Typ.)
9, 10, 13, 16, 23, 31	7, 8, 13, 16, 26, 37	V_{SS}	Input	Power input (0V GND)
19, 20, 17, 21, 22	20, 21, 18, 24, 25	CP_0~CP_4	I/O	Bidirectional port for communications. Supports several communications protocols by specifying mode.

(*) ● The ~SERVICE and IO_4 to IO_7 terminals are programmable pull-ups.
● All V_{DD} terminals must be externally connected.
● All V_{SS} terminals must be externally connected.

MAXIMUM RATINGS (V_{SS} = 0V, V_{SS} typ)

ITEM	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{DD}	− 0.3~7.0	V
Input Voltage	V_{IN}	− 0.3 to V_{DD} + 0.3	V
Input Voltage CP_0-CP_3	V_{IN}	− 1.2 to V_{DD} + 1.2	V
Power Dissipation	P_D	800	mW
Storage Temperature	T_{stg}	− 65~150	°C

OPERATING CONDITIONS

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V_{DD}	4.5	5.0	5.5	V
Input Voltage (TTL)	V_{IH}	2.0	—	V_{DD}	V
	V_{IL}	V_{SS}	—	0.8	V
Input Voltage (CMOS)	V_{IH}	V_{DD} − 0.8	—	V_{DD}	V
	V_{IL}	V_{SS}	—	0.8	V
Input Voltage CP_0-CP_3 (differential mode)	V_{IH}	—	—	V_{DD} + 1.0	V
	V_{IL}	—	—	− 1.0	
Operating Frequency	f_{osc}	0.625	—	20	MHz
Operating Temperature	T_{opr}	− 40	—	85	°C

ELECTRICAL CHARACTERISTICS

DC characteristic (V_{DD} = 5.0V ± 10%, V_{SS} = 0V, Ta = − 40~85°C)
(Above operating conditions apply unless otherwise states.)

ITEM	SYMBOL	PINS	TEST CONDITION		MIN.	MAX.	UNIT
LOW Level Input Voltage (1)	V_{IL} (1)	IO_0~IO_{10} CP_0, CP_3, CP_4, ~SERVICE	—		0	0.8	V
LOW Level Input Voltage (2)	V_{IL} (2)	~RESET	—		0	V_{DD} ×0.3	V
HIGH Level Input Voltage (1)	V_{IH} (1)	IO_0~IO_{10} CP_0, CP_3, CP_4, ~SERVICE	—		2.0	V_{DD}	V
HIGH Level Input Voltage (2)	V_{IH} (2)	~RESET	—		V_{DD} − 0.7	V_{DD}	V
LOW Output Voltage (1)	V_{OL} (1)	IO_0~IO_3 ~SERVICE, ~RESET	I_{OL} = 20mA		0	0.8	V
			I_{OL} = 10mA		0	0.4	
LOW Output Voltage (2)	V_{OL} (2)	CP_2, CP_3	I_{OL} = 40mA		0	1.0	V
LOW Output Voltage (3)	V_{OL} (3)	(Note 1)	I_{OL} = 1.4mA		0	0.4	V
HIGH Output Voltage (1)	V_{OH} (1)	IO_0~IO_3	I_{OH} = − 1.4mA		V_{DD} − 0.4	V_{DD}	V
HIGH Output Voltage (2)	V_{OH} (2)	~SERVICE	I_{OH} = − 1.4mA		V_{DD} − 0.4	V_{DD}	V
HIGH Output Voltage (3)	V_{OH} (3)	CP_2, CP_3	I_{OH} = − 40mA		V_{DD} − 1.0	V_{DD}	V
HIGH Output Voltage (4)	V_{OH} (4)	(Note 1)	I_{OH} = − 1.4mA		V_{DD} − 0.4	V_{DD}	V
Input Current	I_{IN}	(Note 2)	V_{IN} = V_{SS}~V_{DD}		− 10	10	μA
Pull-up Current	I_{PU} (Note 3)	IO_4~IO_7 ~SERVICE, ~RESET	V_{IN} = 0V		− 30	− 300	μA
Current (operating)	I_{DD} (1)	V_{DD}	V_{DD} = 5.5V (no load)	20MHz	—	55	mA
				10MHz	—	30	
Current (SLEEP mode)	I_{DD} (2)	V_{DD}	V_{DD} = 5.5V (no load)		—	0.1	mA
Low-voltage Detection Level	V_{LVD}	V_{DD}	—		3.8	4.4	V
Differential Output Voltage	V_{OD}	CP_2, CP_3	I_O = 60mA		1.5	—	V

(Note 1) Output voltage characteristics exclude the ~RESET pin and CLK2 pin.
(Note 2) Excludes pull-up input pins.
(Note 3) The IO_4 to IO_7 and ~SERVICE pins have programmable pull-ups. ~RESET has a fixed pull-up.

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  "PORTABLE DEVICES"

  (Ⅰ) A portable device defined by ISO standard 7816 as having a width or length of ±10mm and a thickness of ±3mm.

  (Ⅱ) A portable device that conforms to the electrical connection placement and shape stipulated by ISO standard 7816 Part 2.

  (Ⅲ) A pocket-sized portable device in which the ID or history of the holder or the ID or history of the device can be stored as information.

  「BULL CP8 patent: America patent number 4,382,279」
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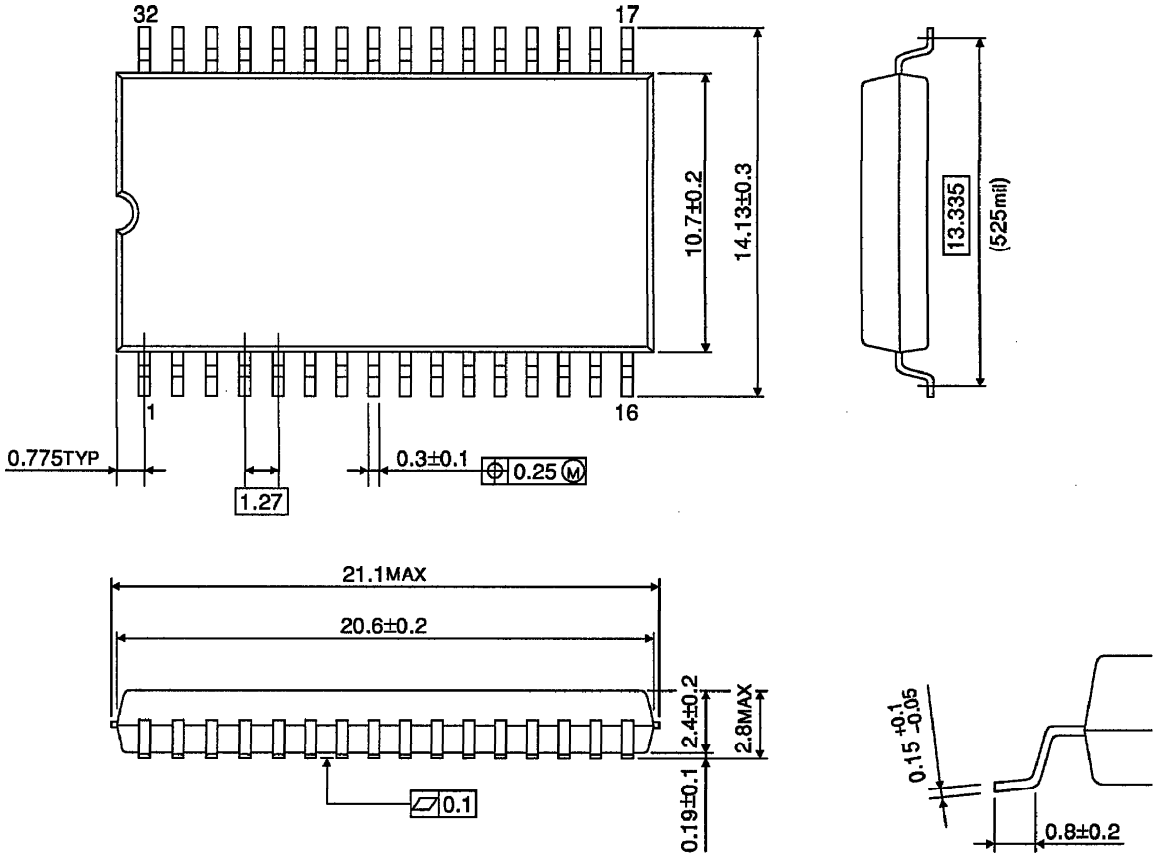
OUTLINE DRAWING

SOP32-P-525-1.27

Unit : mm

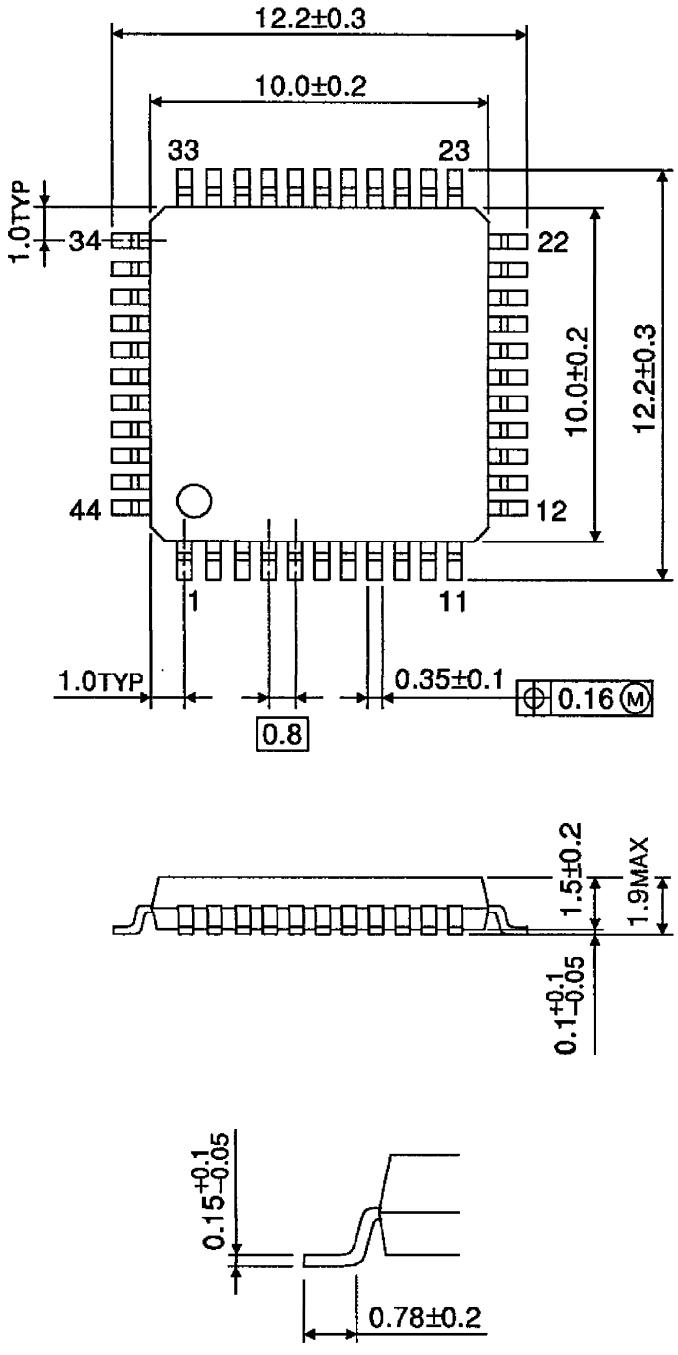


Weight : 1.1g (Typ.)

OUTLINE DRAWING

QFP44-P-1010-0.80

Unit : mm



Weight : 0.6g (Typ.)