**N**ational **Semiconductor**

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# TP3070, TP3071, TP3070-X
# COMBO® II Programmable PCM CODEC/Filter

## General Description

The TP3070 and TP3071 are second-generation combined PCM CODEC and Filter devices optimized for digital switching applications on subscriber line and trunk cards. Using advanced switched capacitor techniques, COMBO II combines transmit bandpass and receive lowpass channel filters with a companding PCM encoder and decoder. The devices are A-law and $\mu$-law selectable and employ a conventional serial PCM interface capable of being clocked up to 4.096 MHz. A number of programmable functions may be controlled via a serial control port.

Channel gains are programmable over a 25.4 dB range in each direction, and a programmable filter is included to enable Hybrid Balancing to be adjusted to suit a wide range of loop impedance conditions. Both transformer and active SLIC interface circuits with real or complex termination impedances can be balanced by this filter, with cancellation in excess of 30 dB being readily achievable when measured across the passband against standard test termination networks.

To enable COMBO II to interface to the SLIC control leads, a number of programmable latches are included; each may be configured as either an input or an output. The TP3070 provides 6 latches and the TP3071 5 latches.

See also AN-614, COMBO II application guide.

## Features

■ Complete CODEC and FILTER system including:
— Transmit and receive PCM channel filters
— $\mu$-law or A-law companding encoder and decoder
— Receive power amplifier drives 300$\Omega$
— 4.096 MHz serial PCM data (max)
■ Programmable Functions:
— Transmit gain: 25.4 dB range, 0.1 dB steps
— Receive gain: 25.4 dB range, 0.1 dB steps
— Hybrid balance cancellation filter
— Time-slot assignment; up to 64 slots/frame
— 2 port assignment (TP3070)
— 6 interface latches (TP3070)
— A or $\mu$-law
— Analog loopback
— Digital loopback
■ Direct interface to solid-state SLICs
■ Simplifies transformer SLIC; single winding secondary
■ Standard serial control interface
■ 80 mW operating power (typ)
■ 1.5 mW standby power (typ)
■ Designed for CCITT and LSSGR applications
■ TTL and CMOS compatible digital interfaces
■ Extended temperature versions available for −40°C to +85°C (TP3070V-X)

## Block Diagram



**FIGURE 1**

TL/H/8635−1

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## Connection Diagrams

TP3070

| | | | |
|---|---|---|---|
| N/C | 4 | | |
| V_BB | 3 | | |
| VF_R0 | 2 | | |
| GND | 1 | | |
| VF_X1 | 28 | | |
| V_CC | 27 | | |
| IL0 | 26 | | |

N/C — 5          25 — IL1
IL3 — 6          24 — IL4
IL2 — 7          23 — IL5
FS_R — 8   TP3070   22 — FS_X
D_R1 — 9          21 — $\overline{TS}_X1$
D_R0 — 10         20 — $\overline{TS}_X0$
CO — 11          19 — D_X1

12 13 14 15 16 17 18
CI CCLK $\overline{CS}$ MR BCLK MCLK D_X0

TL/H/8635–4

**Order Number TP3070V**
**(0°C to +70°C)**
**Order Number TP3070V-X**
**(−40°C to +85°C)**
**See NS Package Number V28A**

GND — 1          20 — VF_X1
VF_R0 — 2         19 — V_CC
V_BB — 3          18 — IL0
IL3 — 4           17 — IL1
IL2 — 5   TP3071   16 — IL4
FS_R — 6          15 — FS_X
D_R0 — 7          14 — $\overline{TS}_X0$
CI/O — 8          13 — D_X0
CCLK — 9          12 — BCLK/MCLK
$\overline{CS}$ — 10          11 — MR
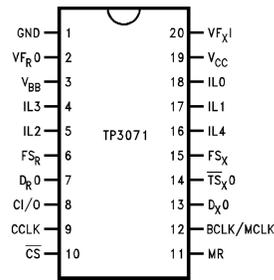
TL/H/8635–2

**Order Number TP3071J**
**See NS Package Number J20A**

**Order Number TP3071N**
**See NS Package Number N20A**

## Pin Descriptions

| Pin | Description |
|---|---|
| $V_{CC}$ | +5V ±5% power supply. |
| $V_{BB}$ | −5V ±5% power supply. |
| GND | Ground. All analog and digital signals are referenced to this pin. |
| $FS_X$ | Transmit Frame Sync input. Normally a pulse or squarewave with an 8 kHz repetition rate is applied to this input to define the start of the transmit time slot assigned to this device (non-delayed data timing mode), or the start of the transmit frame (delayed data timing mode using the internal time-slot assignment counter). |
| $FS_R$ | Receive Frame Sync input. Normally a pulse or squarewave with an 8 kHz repetition rate is applied to this input to define the start of the receive time slot assigned to this device (non-delayed data timing mode), or the start of the receive frame (delayed data timing mode using the internal time-slot assignment counter). |
| BCLK | Bit clock input used to shift PCM data into and out of the $D_R$ and $D_X$ pins. BCLK may vary from 64 kHz to 4.096 MHz in 8 kHz increments, and must be synchronous with MCLK. |
| MCLK | Master clock input used by the switched capacitor filters and the encoder and decoder sequencing logic. Must be 512 kHz, 1.536 MHz, 1.544 MHz, 2.048 MHz or 4.096 MHz and synchronous with BCLK. |
| $VF_XI$ | The Transmit analog high-impedance input. Voice frequency signals present on this input are encoded as an A-law or $\mu$-law PCM bit stream and shifted out on the selected $D_X$ pin. |
| $VF_RO$ | The Receive analog power amplifier output, capable of driving load impedances as low as $300\Omega$ (depending on the peak overload level required). PCM data received on the assigned $D_R$ pin is decoded and appears at this output as voice frequency signals. |
| $D_X0$ | $D_X1$ is available on the TP3070 only; $D_X0$ is available on all devices. These Transmit Data TRI-STATE® outputs remain in the high impedance state except during the assigned transmit time slot on the assigned port, during which the transmit PCM data byte is shifted out on the rising edges of BCLK. |
| $D_X1$ | |
| $\overline{TS}_X0$ | $\overline{TS}_X1$ is available on the TP3070 only; $\overline{TS}_X0$ is available on all devices. Normally these open-drain outputs are floating in a high impedance state except when a time-slot is active on one of the $D_X$ outputs, when the appropriate $\overline{TS}_X$ output pulls low to enable a backplane line-driver. |
| $\overline{TS}_X1$ | |
| $D_R0$ | $D_R1$ is available on the TP3070 only; $D_R0$ is available on all devices. These receive data inputs are inactive except during the assigned receive time slot of the assigned port when the receive PCM data is shifted in on the falling edges of BCLK. |
| $D_R1$ | |
| CCLK | Control Clock input. This clock shifts serial control information into or out from CI/O or CI and CO when the $\overline{CS}$ input is low, depending on the current instruction. CCLK may be asynchronous with the other system clocks. |
| CI/O | This is the Control Data I/O pin which is provided on the TP3071. Serial control information is shifted to or read from COMBO II on this pin when $\overline{CS}$ is low. The direction of the data is determined by the current instruction as defined in Table I. |
| CI | This is a separate Control Input, available only on the TP3070. It can be connected to CO if required. |
| CO | This is a separate Control Output, available only on the TP3070. It can be connected to CI if required. |
| $\overline{CS}$ | Chip Select input. When this pin is low, control information can be written to or read from COMBO II via the CI/O pin (or CI and CO). |
| IL5–IL0 | IL5 through IL0 are available on the TP3070. IL4 through IL0 are available on the TP3071. |

## Pin Descriptions (Continued)

| Pin | Description |
|---|---|
| | Each Interface Latch I/O pin may be individually programmed as an input or an output determined by the state of the corresponding bit in the Latch Direction Register (LDR). For pins configured as inputs, the logic state sensed on each input is latched into the Interface Latch Register (ILR) whenever control data is written to COMBO II, while $\overline{CS}$ is low, and the information is shifted out on the CO (or CI/O) pin. When configured as outputs, control data written into the ILR appears at the corresponding IL pins. |
| MR | This logic input must be pulled low for normal operation of COMBO II. When pulled momentarily high (at least 1 $\mu$sec.), all programmable registers in the device are reset to the states specified under "Power-On Initialization". |
| NC | No Connection. Do not connect to this pin. Do not route traces through this pin. |

## Functional Description

### POWER-ON INITIALIZATION

When power is first applied, power-on reset circuitry initializes the COMBO II and puts it into the power-down state. The gain control registers for the transmit and receive gain sections are programmed to OFF (00000000), the hybrid balance circuit is turned off, the power amp is disabled and the device is in the non-delayed timing mode. The Latch Direction Register (LDR) is pre-set with all IL pins programmed as inputs, placing the SLIC interface pins in a high impedance state. The CI/O pin is set as an input ready for the first control byte of the initialization sequence. Other initial states in the Control Register are indicated in Section 2.0.

A reset to these same initial conditions may also be forced by driving the MR pin momentarily high. This may be done either when powered-up or down. For normal operation this pin must be pulled low. If not used, MR should be hardwired to ground.

The desired modes for all programmable functions may be initialized via the control port prior to a Power-up command.

### POWER-DOWN STATE

Following a period of activity in the powered-up state the power-down state may be re-entered by writing any of the control instructions into the serial control port with the "P" bit set to "1" as indicated in Table I. It is recommended that the chip be powered down before writing any additional instructions. In the power-down state, all non-essential circuitry is de-activated and the $D_X0$ (and $D_X1$) outputs are in the high impedance TRI-STATE condition.

The coefficients stored in the Hybrid Balance circuit and the Gain Control registers, the data in the LDR and ILR, and all control bits remain unchanged in the power-down state unless changed by writing new data via the serial control port, which remains active. The outputs of the Interface Latches also remain active, maintaining the ability to monitor and control the SLIC.

### TRANSMIT FILTER AND ENCODER

The Transmit section input, $VF_X I$, is a high impedance summing input which is used as the differencing point for the internal hybrid balance cancellation signal. No external components are necessary to set the gain. Following this circuit is a programmable gain/attenuation amplifier which is controlled by the contents of the Transmit Gain Register (see Programmable Functions section). An active pre-filter then precedes the 3rd order high-pass and 5th order low-pass switched capacitor filters. The A/D converter has a compressing characteristic according to the standard CCITT A or $\mu255$ coding laws, which must be selected by a control instruction during initialization (see Tables I and II). A precision on-chip voltage reference ensures accurate and highly stable transmission levels. Any offset voltage arising in the gain-set amplifier, the filters or the comparator is canceled by an internal auto-zero circuit.

Each encode cycle begins immediately following the assigned Transmit time-slot. The total signal delay referenced to the start of the time-slot is approximately 165 $\mu$s (due to the Transmit Filter) plus 125 $\mu$s (due to encoding delay), which totals 290 $\mu$s. Data is shifted out on $D_X0$ or $D_X1$ during the selected time slot on eight rising edges of BCLK.

### DECODER AND RECEIVE FILTER

PCM data is shifted into the Decoder's Receive PCM Register via the $D_R0$ or $D_R1$ pin during the selected time-slot on the 8 falling edges of BCLK. The Decoder consists of an expanding DAC with either A or $\mu255$ law decoding characteristic, which is selected by the same control instruction used to select the Encode law during initialization. Following the Decoder is a 5th order low-pass switched capacitor filter with integral Sin x/x correction for the 8 kHz sample and hold. A programmable gain amplifier, which must be set by writing to the Receive Gain Register, is included, and finally a Power Amplifier capable of driving a 300$\Omega$ load to $\pm3.5$V, a 600$\Omega$ load to $\pm3.8$V or a 15 k$\Omega$ load to $\pm4.0$V at peak overload.

A decode cycle begins immediately after the assigned receive time-slot, and 10 $\mu$s later the Decoder DAC output is updated. The total signal delay is 10 $\mu$s plus 120 $\mu$s (filter delay) plus 62.5 $\mu$s ($\frac{1}{2}$ frame) which gives approximately 190 $\mu$s.

### PCM INTERFACE

The $FS_X$ and $FS_R$ frame sync inputs determine the beginning of the 8-bit transmit and receive time-slots respectively. They may have any duration from a single cycle of BCLK HIGH to one MCLK period LOW. Two different relationships may be established between the frame sync inputs and the actual time-slots on the PCM busses by setting bit 3 in the Control Register (see Table II). Non-delayed data mode is similar to long-frame timing on the TP3050/60 series of devices (COMBO); time-slots begin nominally coincident with the rising edge of the appropriate FS input. The alternative is to use Delayed Data mode, which is similar to short-frame sync timing on COMBO, in which each FS input must be high at least a half-cycle of BCLK earlier than the time-slot. The Time-Slot Assignment circuit on the device can only be used with Delayed Data timing.

When using Time-Slot Assignment, the beginning of the first time-slot in a frame is identified by the appropriate FS input. The actual transmit and receive time-slots are then determined by the internal Time-Slot Assignment counters.

Transmit and Receive frames and time-slots may be skewed from each other by any number of BCLK cycles. During each assigned Transmit time-slot, the selected $D_X0/1$ output shifts data out from the PCM register on the rising edges of BCLK. $\overline{TS}_X0$ (or $\overline{TS}_X1$ as appropriate) also pulls low for the first 7$\frac{1}{2}$ bit times of the time-slot to control the TRI-STATE Enable of a backplane line-driver. Serial PCM data is shifted into the selected $D_R0/1$ input during each assigned Receive time-slot on the falling edges of BCLK. $D_X0$ or $D_X1$ and $D_R0$ or $D_R1$ are selectable on the TP3070 only, see Section 6.

## Functional Description (Continued)

**TABLE I. Programmable Register Instructions**

| Function | Byte 1 (Note 1) 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Byte 2 (Note 1) 7  6  5  4  3  2  1  0 |
|---|---|---|---|---|---|---|---|---|---|
| Single Byte Power-Up/Down | P | X | X | X | X | X | 0 | X | None |
| Write Control Register | P | 0 | 0 | 0 | 0 | 0 | 1 | X | See Table II |
| Read-Back Control Register | P | 0 | 0 | 0 | 0 | 1 | 1 | X | See Table II |
| Write to Interface Latch Register | P | 0 | 0 | 0 | 1 | 0 | 1 | X | See Table V |
| Read Interface Latch Register | P | 0 | 0 | 0 | 1 | 1 | 1 | X | See Table V |
| Write Latch Direction Register | P | 0 | 0 | 1 | 0 | 0 | 1 | X | See Table IV |
| Read Latch Direction Register | P | 0 | 0 | 1 | 0 | 1 | 1 | X | See Table IV |
| Write Receive Gain Register | P | 0 | 1 | 0 | 0 | 0 | 1 | X | See Table VIII |
| Read Receive Gain Register | P | 0 | 1 | 0 | 0 | 1 | 1 | X | See Table VIII |
| Write Transmit Gain Register | P | 0 | 1 | 0 | 1 | 0 | 1 | X | See Table VII |
| Read Transmit Gain Register | P | 0 | 1 | 0 | 1 | 1 | 1 | X | See Table VII |
| Write Receive Time-Slot/Port | P | 1 | 0 | 0 | 0 | 0 | 1 | X | See Table VI |
| Read-Back Receive Time-Slot/Port | P | 1 | 0 | 0 | 0 | 1 | 1 | X | See Table VI |
| Write Transmit Time-Slot/Port | P | 1 | 0 | 1 | 0 | 0 | 1 | X | See Table VI |
| Read-Back Transmit Time-Slot/Port | P | 1 | 0 | 1 | 0 | 1 | 1 | X | See Table VI |
| Write Hybrid Balance Register 1 | P | 0 | 1 | 1 | 0 | 0 | 1 | X | Derive from Optimization Routine in TP3077SW Program |
| Read Hybrid Balance Register 1 | P | 0 | 1 | 1 | 0 | 1 | 1 | X | |
| Write Hybrid Balance Register 2 | P | 0 | 1 | 1 | 1 | 0 | 1 | X | |
| Read Hybrid Balance Register 2 | P | 0 | 1 | 1 | 1 | 1 | 1 | X | |
| Write Hybrid Balance Register 3 | P | 1 | 0 | 0 | 0 | 0 | 1 | X | |
| Read Hybrid Balance Register 3 | P | 1 | 0 | 0 | 0 | 1 | 1 | X | |

**Note 1:** Bit 7 of bytes 1 and 2 is always the first bit clocked into or out from the CI, CO or CI/O pin. X = don't care.

**Note 2:** "P" is the power-up/down control bit, see "Power-Up/Down Control" section. ("0" = Power Up, "1" = Power Down)

**Note 3:** Other register address codes are invalid and should not be used.

### SERIAL CONTROL PORT

Control information and data are written into or read-back from COMBO II via the serial control port consisting of the control clock CCLK, the serial data input/output CI/O, (or separate input, CI, and output, CO, on the TP3070 only), and the Chip Select input, CS. All control instructions require 2 bytes, as listed in Table I, with the exception of a single byte power-up/down command. The byte 1 bits are used as follows: bit 7 specifies power up or power down; bits 6, 5, 4 and 3 specify the register address; bit 2 specifies whether the instruction is read or write; bit 1 specifies a one or two byte instruction; and bit 0 is not used.

To shift control data into COMBO II, CCLK must be pulsed 8 times while CS is low. Data on the CI/O (or CI) input is shifted into the serial input register on the falling edge of each CCLK pulse. After all data is shifted in, the contents of the input shift register are decoded, and may indicate that a 2nd byte of control data will follow. This second byte may either be defined by a second byte-wide CS pulse or may follow the first contiguously, i.e. it is not mandatory for CS to return high between the first and second control bytes. At the end of CCLK8 in the 2nd control byte the data is loaded into the appropriate programmable register. CS may remain low continuously when programming successive registers, if desired. However, CS should be set high when no data transfers are in progress.

To readback Interface Latch data or status information from COMBO II, the first byte of the appropriate instruction is strobed in while CS is low, as defined in Table I. CS must be kept low, or be taken low again for a further 8 CCLK cycles, during which the data is shifted onto the CO or CI/O pin on the rising edges of CCLK. When CS is high the CO or CI/O pin is in the high-impedance TRI-STATE, enabling the CI/O pins of many devices to be multiplexed together.

If CS returns high during either byte 1 or byte 2 before all eight CCLK pulses of that byte occur, both the bit count and byte count are reset and register contents are not affected. This prevents loss of synchronization in the control interface as well as corruption of register data due to processor interrupt or other problem. When CS returns low again, the device will be ready to accept bit 1 of byte 1 of a new instruction.

## Programmable Functions

### 1.0 POWER-UP/DOWN CONTROL

Following power-on initialization, power-up and power-down control may be accomplished by writing any of the control instructions listed in Table I into COMBO II with the "P" bit set to "0" for power-up or "1" for power-down. Normally it is recommended that all programmable functions be initially programmed while the device is powered down. Power state control can then be included with the last programming instruction or the separate single-byte instruction. Any of the programmable registers may also be modified while the device is powered-up or down by setting the "P" bit as indicated. When the power-up or down control is entered as a single byte instruction, bit one (1) must be reset to a 0.

When a power-up command is given, all de-activated circuits are activated, but the TRI-STATE PCM output(s), $D_X0$ (and $D_X1$), will remain in the high impedance state until the second $FS_X$ pulse after power-up.

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## Programmable Functions (Continued)

### 2.0 CONTROL REGISTER INSTRUCTION

The first byte of a READ or WRITE instruction to the Control Register is as shown in Table I. The second byte has the following bit functions:

#### TABLE II. Control Register Byte 2 Functions

| Bit Number and Name | | | | | | | | Function |
|---|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| $F_1$ | $F_0$ | MA | IA | DN | DL | AL | PP | |
| 0 | 0 | | | | | | | MCLK = 512 kHz |
| 0 | 1 | | | | | | | MCLK = 1.536 or 1.544 MHz |
| 1 | 0 | | | | | | | MCLK = 2.048 MHz* |
| 1 | 1 | | | | | | | MCLK = 4.096 MHz |
| | | 0 | X | | | | | Select $\mu$-255 law* |
| | | 1 | 0 | | | | | A-law, Including Even Bit Inversion |
| | | 1 | 1 | | | | | A-law, No Even Bit Inversion |
| | | | | 0 | | | | Delayed Data Timing |
| | | | | 1 | | | | Non-Delayed Data Timing* |
| | | | | | 0 | 0 | | Normal Operation* |
| | | | | | 1 | X | | Digital Loopback |
| | | | | | 0 | 1 | | Analog Loopback |
| | | | | | | | 0 | Power Amp Enabled in PDN |
| | | | | | | | 1 | Power Amp Disabled in PDN* |

* = State at power-on initialization. (Bit 4 = 0)

#### 2.1 Master Clock Frequency Selection

A Master clock must be provided to COMBO II for operation of the filter and coding/decoding functions. The MCLK frequency must be either 512 kHz, 1.536 MHz, 1.544 MHz, 2.048 MHz, or 4.096 MHz and must be synchronous with BCLK. Bits $F_1$ and $F_0$ (see Table II) must be set during initialization to select the correct internal divider.

#### 2.2 Coding Law Selection

Bits "MA" and "IA" in Table II permit the selection of $\mu$255 coding or A-law coding, with or without even bit inversion.

#### 2.3 Analog Loopback

Analog Loopback mode is entered by setting the "AL" and "DL" bits in the Control Register as shown in Table II. In the analog loopback mode, the Transmit input $VF_XI$ is isolated from the input pin and internally connected to the $VF_RO$ output, forming a loop from the Receive PCM Register back to the Transmit PCM Register. The $VF_RO$ pin remains active, and the programmed settings of the Transmit and Receive gains remain unchanged, thus care must be taken to ensure that overload levels are not exceeded anywhere in the loop. Hybrid balance must be disabled for meaningful analog loopback function.

#### 2.4 Digital Loopback

Digital Loopback mode is entered by setting the "AL" and "DL" bits in the Control Register as shown in Table II. This mode provides another stage of path verification by enabling data written into the Receive PCM Register to be read back from that register in any Transmit time-slot at $D_X0/1$. In digital loopback, the decoder will remain functional and output a signal at $VF_RO$. If this is undesirable, the receive output can be turned off by programming the receive gain register to all zeros.

#### 3.0 INTERFACE LATCH DIRECTIONS

Immediately following power-on, all Interface Latches assume they are inputs, and therefore all IL pins are in a high impedance state. Each IL pin may be individually programmed as a logic input or output by writing the appropriate instruction to the LDR, see Tables I and IV. For minimum power dissipation, unconnected latch pins should be programmed as outputs. For the TP3071, L5 should always be programmed as an output.

Bits $L_5$–$L_0$ must be set by writing the specified instruction to the LDR with the L bits in the second byte set as follows:

#### TABLE IV. Byte 2 Functions of Latch Direction Register

| Byte 2 Bit Number | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $L_0$ | $L_1$ | $L_2$ | $L_3$ | $L_4$ | $L_5$ | X | X |

| $L_n$ Bit | IL Direction |
|---|---|
| 0 | Input |
| 1 | Output |

X = don't care

#### 4.0 INTERFACE LATCH STATES

Interface Latches configured as outputs assume the state determined by the appropriate data bit in the 2-byte instruction written to the Interface Latch Register (ILR) as shown in Tables I and V. Latches configured as inputs will sense the state applied by an external source, such as the Off-Hook detect output of a SLIC. All bits of the ILR, i.e. sensed inputs and the programmed state of outputs, can be read back in the 2nd byte of a READ from the ILR.

It is recommended that during initialization, the state of IL pins to be configured as outputs should be programmed first, followed immediately by the Latch Direction Register.

#### TABLE V. Interface Latch Data Bit Order

| Bit Number | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_4$ | $D_5$ | X | X |

#### TABLE III. Coding Law Conventions

| | $\mu$255 law | | True A-law with even bit inversion | | A-law without even bit inversion | |
|---|---|---|---|---|---|---|
| | MSB | LSB | MSB | LSB | MSB | LSB |
| $V_{IN}$ = +Full Scale | 1000 | 0000 | 1010 | 1010 | 1111 | 1111 |
| $V_{IN}$ = 0V | 1111 | 1111 | 1101 | 0101 | 1000 | 0000 |
| | 0111 | 1111 | 0101 | 0101 | 0000 | 0000 |
| $V_{IN}$ = −Full Scale | 0000 | 0000 | 0010 | 1010 | 0111 | 1111 |

Note 1: The MSB is always the first PCM bit shifted in or out of COMBO II.

## Programmable Functions (Continued)

**TABLE VI. Time-Slot and Port Assignment Instruction**

| Bit Number and Name | | | | | | | | Function |
|---|---|---|---|---|---|---|---|---|
| **7**<br>**EN** | **6**<br>**PS**<br>**(Note 1)** | **5**<br>**T5**<br>**(Note 2)** | **4**<br>**T4** | **3**<br>**T3** | **2**<br>**T2** | **1**<br>**T1** | **0**<br>**T0** | |
| 0 | 0 | X | X | X | X | X | X | Disable $D_X0$ Output (Transmit Instruction)<br>Disable $D_R0$ Input (Receive Instruction) |
| 0 | 1 | X | X | X | X | X | X | Disable $D_X1$ Output (Transmit Instruction)<br>Disable $D_R1$ Input (Receive Instruction) |
| 1 | 0 | Assign One Binary Coded Time-Slot from 0–63 | | | | | | Enable $D_X0$ Output (Transmit Instruction)<br>Enable $D_R0$ Input (Receive Instruction) |
|  |  | Assign One Binary Coded Time-Slot from 0–63 | | | | | |  |
| 1 | 1 | Assign One Binary Coded Time-Slot from 0–63 | | | | | | Enable $D_X1$ Output (Transmit Instruction)<br>Enable $D_R1$ Input (Receive Instruction) |
|  |  | Assign One Binary Coded Time-Slot from 0–63 | | | | | |  |

**Note 1:** The ''PS'' bit MUST always be set to 0 for the TP3071.

**Note 2:** T5 is the MSB of the Time-slot assignment bit field. Time slot bits should be set to ''000000'' for both transmit and receive when operating in non-delayed data timing mode.

### 5.0 TIME-SLOT ASSIGNMENT

COMBO II can operate in either fixed time-slot or time-slot assignment mode for selecting the Transmit and Receive PCM time-slots. Following power-on, the device is automatically in Non-Delayed Timing mode, in which the time-slot always begins with the leading (rising) edge of frame sync inputs $FS_X$ and $FS_R$. Time-Slot Assignment may only be used with Delayed Data timing; see *Figure 6*. $FS_X$ and $FS_R$ may have any phase relationship with each other in BCLK period increments.

Alternatively, the internal time-slot assignment counters and comparators can be used to access any time-slot in a frame, using the frame sync inputs as marker pulses for the beginning of transmit and receive time-slot 0. In this mode, a frame may consist of up to 64 time-slots of 8 bits each. A time-slot is assigned by a 2-byte instruction as shown in Tables I and VI. The last 6 bits of the second byte indicate the selected time-slot from 0–63 using straight binary notation. When writing a timeslot and port assignment register, if the PCM interface is currently active, it is immediately deactivated to prevent possible bus clashes. A new assignment becomes active on the second frame following the end of the Chip-Select for the second control byte. Rewriting of register contents should not be performed during the talking period of a connection to prevent waveform distortion caused by loss of a sample which will occur with each register write. The ''EN'' bit allows the PCM inputs, $D_R0/1$, or outputs, $D_X0/1$, as appropriate, to be enabled or disabled.

Time-Slot Assignment mode requires that the $FS_X$ and $FS_R$ pulses must conform to the delayed data timing format shown in *Figure 6*.

### 6.0 PORT SELECTION

On the TP3070 only, an additional capability is available; 2 Transmit serial PCM ports, $D_X0$ and $D_X1$, and 2 Receive serial PCM ports, $D_R0$ and $D_R1$, are provided to enable two-way space switching to be implemented. Port selections for transmit and receive are made within the appropriate time-slot assignment instruction using the ''PS'' bit in the second byte. The PS bit selects either Port 0 or Port 1. Both ports cannot be active at the same time.

On the TP3071, only ports $D_X0$ and $D_R0$ are available, therefore the ''PS'' bit MUST always be set to 0 for these devices.

Table VI shows the format for the second byte of both transmit and receive time-slot and port assignment instructions.

### 7.0 TRANSMIT GAIN INSTRUCTION BYTE 2

The transmit gain can be programmed in 0.1 dB steps by writing to the Transmit Gain Register as defined in Tables I and VII. This corresponds to a range of 0 dBm0 levels at $VF_XI$ between 1.619 Vrms and 0.087 Vrms (equivalent to $+6.4$ dBm to $-19.0$ dBm in 600Ω).

To calculate the binary code for byte 2 of this instruction for any desired input 0 dBm0 level in Vrms, take the nearest integer to the decimal number given by:

$$200 \times \log_{10} (V/0.08595)$$

and convert to the binary equivalent. Some examples are given in Table VII and a complete tabulation is given in Appendix I of AN-614.

It should be noted that the Transmit (idle channel) Noise and Transmit Signal to Total Distortion are both specified with transmit gain set to 0 dB (Gain Register set to all ones). At high transmit gains there will be some degradation in noise performance for these parameters. See Application Note AN-614 for more information on this subject.

**TABLE VII. Byte 2 of Transmit Gain Instruction**

| Bit Number<br>7 6 5 4 3 2 1 0 | 0 dBm0 Test Level (Vrms)<br>at $VF_XI$ |
|---|---|
| 0 0 0 0 0 0 0 0 | No Output* |
| 0 0 0 0 0 0 0 1 | 0.087 |
| 0 0 0 0 0 0 1 0 | 0.088 |
| — | — |
| 1 1 1 1 1 1 1 0 | 1.600 |
| 1 1 1 1 1 1 1 1 | 1.619 |

*Analog signal path is cut off, but $D_X$ remains active and will output codes representing idle noise.

### 8.0 RECEIVE GAIN INSTRUCTION BYTE 2

The receive gain can be programmed in 0.1 dB steps by writing to the Receive Gain Register as defined in Tables I and VIII. Note the following restrictions on output drive capability:

## Programmable Functions (Continued)

a) 0 dBm0 levels $\leq$ 1.96 Vrms at $VF_RO$ may be driven into a load of $\geq$ 15 k$\Omega$ to GND; receive gain set to 0 dB (Gain Register set to all ones)

b) 0 dBm0 levels $\leq$ 1.85 Vrms at $VF_RO$ may be driven into a load of $\geq$ 600$\Omega$ to GND; receive gain set to $-0.5$ dB

c) 0 dBm0 levels $\leq$ 1.71 Vrms at $VF_RO$ may be driven into a load of $\geq$ 300$\Omega$ to GND; receive gain set to $-1.2$ dB

To calculate the binary code for byte 2 of this instruction for any desired output 0 dBm0 level in Vrms, take the nearest integer to the decimal number given by:

$$200 \times \log_{10} (V/0.1043)$$

and convert to the binary equivalent. Some examples are given in Table VIII and a complete tabulation is given in Appendix I of AN-614.

**TABLE VIII. Byte 2 of Receive Gain Instruction**

| Bit Number<br>7 6 5 4 3 2 1 0 | 0 dBm0 Test Level (Vrms)<br>at $VF_RO$ |
|---|---|
| 0 0 0 0 0 0 0 0 | No Output (Low Z to GND) |
| 0 0 0 0 0 0 0 1 | 0.105 |
| 0 0 0 0 0 0 1 0 | 0.107 |
| — | — |
| 1 1 1 1 1 1 1 0 | 1.941 |
| 1 1 1 1 1 1 1 1 | 1.964 |

### 9.0 HYBRID BALANCE FILTER

The Hybrid Balance Filter on COMBO II is a programmable filter consisting of a second-order section, Hybal1, followed by a first-order section, Hybal2, and a programmable attenuator. Either of the filter sections can be bypassed if only one is required to achieve good cancellation. A selectable 180 degree inverting stage is included to compensate for interface circuits which also invert the transmit input relative to the receive output signal. The 2nd order section is intended mainly to balance low frequency signals across a transformer SLIC, and the first order section to balance midrange to higher audio frequency signals.

As a 2nd order section, Hybal1 has a pair of low frequency zeroes and a pair of complex conjugate poles. When configuring Hybal1, matching the phase of the hybrid at low to mid-band frequencies is most critical. Once the echo path is correctly balanced in phase, the magnitude of the cancella-

tion signal can be corrected by the programmable attenuator.

The 2nd order mode of Hybal1 is most suitable for balancing interfaces with transformers having high inductance of 1.5 Henries or more. An alternative configuration for smaller transformers is available by converting Hybal1 to a simple first-order section with a single real low-frequency pole and zero. In this mode, the pole/zero frequency may be programmed.

Many line interfaces can be adequately balanced by use of the Hybal1 section only, in which case the Hybal2 filter should be de-selected to bypass it.

Hybal2, the higher frequency first-order section, is provided for balancing an electronic SLIC, and is also helpful with a transformer SLIC in providing additional phase correction for mid and high-band frequencies, typically 1 kHz to 3.4 kHz. Such a correction is particularly useful if the test balance impedance includes a capacitor of 100 nF or less, such as the loaded and non-loaded loop test networks in the United States. Independent placement of the pole and zero location is provided.

*Figure 2* shows a simplified diagram of the local echo path for a typical application with a transformer interface. The magnitude and phase of the local echo signal, measured at $VF_XI$, are a function of the termination impedance $Z_T$, the line transformer and the impedance of the 2W loop, $Z_L$. If the impedance reflected back into the transformer primary is expressed as $Z_L'$ then the echo path transfer function from $VF_RO$ to $VF_XI$ is:

$$H(w) = Z_L'/(Z_T + Z_L') \qquad (1)$$

### 9.1 PROGRAMMING THE FILTER

On initial power-up, the Hybrid Balance filter is disabled. Before the hybrid balance filter can be programmed it is necessary to design the transformer and termination impedance in order to meet system 2W input return loss specifications, which are normally measured against a fixed test impedance (600 or 900$\Omega$ in most countries). Only then can the echo path be modeled and the hybrid balance filter programmed. Hybrid balancing is also measured against a fixed test impedance, specified by each national Telecom administration to provide adequate control of talker and listener
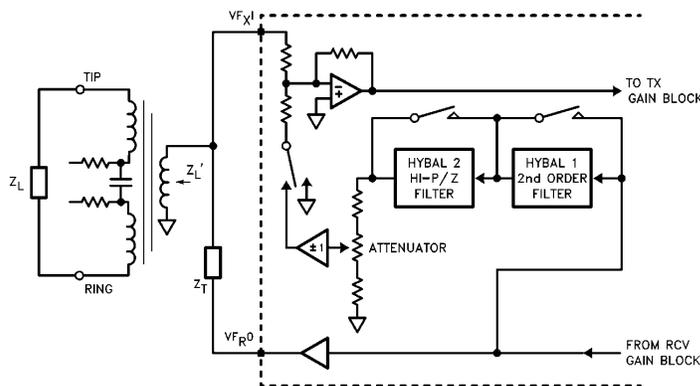


FIGURE 2. Simplified Diagram of Hybrid Balance Circuit

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## Programmable Functions (Continued)

echo over the majority of their network connections. This test impedance is $Z_L$ in *Figure 2*. The echo signal and the degree of transhybrid loss obtained by the programmable filter must be measured from the PCM digital input, $D_R0$, to the PCM digital output, $D_X0$, either by digital test signal analysis or by conversion back to analog by a PCM CODEC/Filter.

Three registers must be programmed in COMBO II to fully configure the Hybrid Balance Filter as follows:

Register 1:  select/de-select Hybrid Balance Filter;

invert/non-invert cancellation signal;

select/de-select Hybal2 filter section;

attenuator setting.

Register 2:  select/de-select Hybal1 filter;

set Hybal1 to 2nd order or 1st order;

pole and zero frequency selection.

Register 3:  program pole frequency in Hybal2 filter;

program zero frequency in Hybal2 filter.

Standard filter design techniques may be used to model the echo path (see Equation 1) and design a matching hybrid balance filter configuration. Alternatively, the frequency response of the echo path can be measured and the hybrid balance filter designed to replicate it.

A Hybrid Balance filter design guide and software optimization program are available under license from National Semiconductor Corporation; order TP3077SW.

## Applications Information

*Figure 3* shows a typical application of the TP3071 together with a typical monolithic SLIC. Four of the IL latches are configured as outputs to control the relay drivers on the SLIC, while IL4 is an input for the Supervision signal.

### POWER SUPPLIES

While the pins of the TP3070 COMBO II devices are well protected against electrical misuse, it is recommended that the standard CMOS practice of applying GND to the device before any other connections are made should always be followed. In applications where the printed circuit card may be plugged into a hot socket with power and clocks already present, extra long pins on the connector should be used for ground and $V_{BB}$. In addition, a Schottky diode should be connected between $V_{BB}$ and ground.

To minimize noise sources, all ground connections to each device should meet at a common point as close as possible to the device GND pin in order to prevent the interaction of ground return currents flowing through a common bus impedance. Power supply decoupling capacitors of 0.1 $\mu$F should be connected from this common device ground point to $V_{CC}$ and $V_{BB}$ as close to the device pins as possible. $V_{CC}$ and $V_{BB}$ should also be decoupled with Low Effective Series Resistance Capacitors of at least 10 $\mu$F located near the card edge connector.

Further guidelines on PCB layout techniques are provided in Application Note AN-614, "COMBO II™ Programmable PCM CODEC/Filter Family Application Guide".
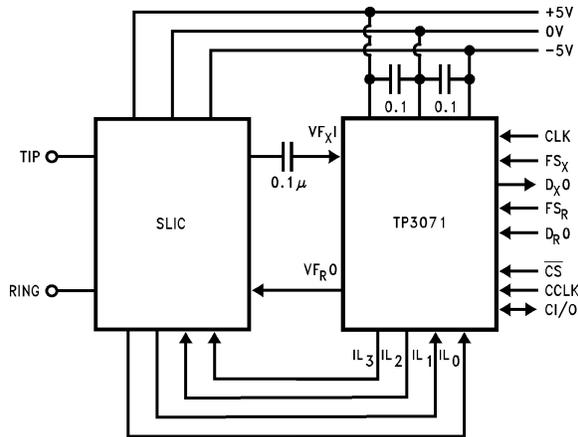


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**FIGURE 3. Typical Application with Monolithic SLIC**

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# Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| $V_{CC}$ to GND | 7V |
| Voltage at $VF_Xl$ | $V_{CC}$ + 0.5V to $V_{BB}$ − 0.5V |
| Voltage at any Digital Input | $V_{CC}$ + 0.5V to GND − 0.5V |
| Storage Temperature Range | −65°C to + 150°C |
| $V_{BB}$ to GND | −7V |
| Current at $VF_R0$ | ±100 mA |
| Current at any Digital Output | ±50 mA |
| Lead Temperature (Soldering, 10 sec.) | 300°C |

# Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for $V_{CC}$ = +5V ±5%, $V_{BB}$ = −5V ±5%; $T_A$ = 0°C to +70°C (−40°C to +85°C for TP3070-X) by correlation with 100% electrical testing at $T_A$ = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at $V_{CC}$ = +5V, $V_{BB}$ = −5V, $T_A$ = 25°C.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **DIGITAL INTERFACES** | | | | | | |
| $V_{IL}$ | Input Low Voltage | All Digital Inputs (DC Meas.)* | | | **0.7** | V |
| $V_{IH}$ | Input High Voltage | All Digital Inputs (DC Meas.)* | **2.0** | | | V |
| $V_{OL}$ | Output Low Voltage | $D_X0$, $D_X1$, $\overline{TS}_X0$, $\overline{TS}_X1$ and CO, $I_L$ = 3.2 mA, All Other Digital Outputs, $I_L$ = 1 mA | | | **0.4** | V |
| $V_{OH}$ | Output High Voltage | $D_X0$, $D_X1$ and CO, $I_L$ = −3.2 mA, All Other Digital Outputs (except $\overline{TS}_X$), $I_L$ = −1 mA | **2.4** | | | V |
| | | All Digital Outputs, $I_L$ = −100 μA | $V_{CC}$ − 0.5 | | | V |
| $I_{IL}$ | Input Low Current | Any Digital Input, GND < $V_{IN}$ < $V_{IL}$ | **−10** | | **10** | μA |
| $I_{IH}$ | Input High Current | Any Digital Input except MR, $V_{IH}$ < $V_{IN}$ < $V_{CC}$ | **−10** | | **10** | μA |
| | | MR Only | **−10** | | **100** | μA |
| $I_{OZ}$ | Output Current in High Impedance State (TRI-STATE) | $D_X0$, $D_X1$, $\overline{TS}_X0$, $\overline{TS}_X1$, CO and CI/O (as an Output) IL5–IL0 When Selected as Inputs GND < $V_{OUT}$ < $V_{CC}$ | **−10** | | **10** | μA |
| | | −40°C to +85°C (TP3070-X) | −30 | | 30 | μA |
| **ANALOG INTERFACES** | | | | | | |
| $I_{VFXI}$ | Input Current, $VF_Xl$ | −3.3V < $VF_Xl$ < 3.3V | **−10.0** | | **10.0** | μA |
| $R_{VFXI}$ | Input Resistance | −3.3V < $VF_Xl$ < 3.3V | **390** | 620 | | kΩ |
| $VOS_X$ | Input Offset Voltage Applied at $VF_Xl$ | Transmit Gain = 0 dB Transmit Gain = 25.4 dB | | | 200 10 | mV mV |
| $RL_{VFRO}$ | Load Resistance | Receive Gain = 0 dB Receive Gain = −0.5 dB Receive Gain = −1.2 dB | 15k 600 **300** | | | Ω |
| $CL_{VFRO}$ | Load Capacitance | $RL_{VFRO}$ ≥ 300Ω $CL_{VFRO}$ from $VF_R$O to GND | | | **200** | pF |
| $RO_{VFRO}$ | Output Resistance | Steady Zero PCM Code Applied to $D_R0$ or $D_R1$ | | 1.0 | 3.0 | Ω |
| $VOS_R$ | Output Offset Voltage at $V_{FRO}$ | Alternating ± Zero PCM Code Applied to $D_R0$ or $D_R1$, Maximum Receive Gain | **−200** | | **200** | mV |
| **POWER DISSIPATION** | | | | | | |
| $I_{CC}0$ | Power Down Current | CCLK, CI/O, CI, CO, = 0.4V, $\overline{CS}$ = 2.4V Interface Latches Set as Outputs with No Load, All Other Inputs Active, Power Amp Disabled | | 0.1 | **0.6** | mA |
| $I_{BB}0$ | Power Down Current | As Above −40°C to +85°C (TP3070-X) | | −0.1 | **−0.3** −0.4 | mA mA |
| $I_{CC}1$ | Power Up Current | CCLK, CI/O, CI, CO = 0.4V, $\overline{CS}$ = 2.4V No Load on Power Amp Interface Latches Set as Outputs with No Load −40°C to +85°C (TP3070-X) | | 8.0 | **11.0** 13.0 | mA mA |
| $I_{BB}1$ | Power Up Current | As Above −40°C to +85°C (TP3070-X) | | −8.0 | **−11.0** −13.0 | mA mA |
| $I_{CC}2$ | Power Down Current | Power Amp Enabled −40°C to +85°C (TP3070-X) | | 2.0 | **3.0** 4.0 | mA mA |
| $I_{BB}2$ | Power Down Current | Power Amp Enabled −40°C to +85°C (TP3070-X) | | −2.0 | **−3.0** −4.0 | mA mA |

**Note** *: See definitions and timing conventions section.

## Timing Specifications

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for $V_{CC} = +5V \pm 5\%$; $V_{BB} = -5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ ($-40°C$ to $+85°C$ for TP3070-X) by correlation with 100% electrical testing at $T_A = 25°C$. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at $V_{CC} = +5V$, $V_{BB} = -5V$, $T_A = 25°C$.

All timing parameters are measured at $V_{OH} = 2.0V$ and $V_{OL} = 0.7V$.

See Definitions and Timing Conventions section for test methods information.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **MASTER CLOCK TIMING** | | | | | | |
| $f_{MCLK}$ | Frequency of MCLK | Selection of Frequency is Programmable (See Table III) | | 512<br>1536<br>1544<br>2048<br>**4096** | | kHz<br>kHz<br>kHz<br>kHz<br>kHz |
| $t_{WMH}$ | Period of MCLK High | Measured from $V_{IH}$ to $V_{IH}$ (See Note) | **80** | | | ns |
| $t_{WML}$ | Period of MCLK Low | Measured from $V_{IL}$ to $V_{IL}$ (See Note) | **80** | | | ns |
| $t_{RM}$ | Rise Time of MCLK | Measured from $V_{IL}$ to $V_{IH}$ | | | 30 | ns |
| $t_{FM}$ | Fall Time of MCLK | Measured from $V_{IH}$ to $V_{IL}$ | | | 30 | ns |
| $t_{HBM}$ | HOLD Time, BCLK LOW to MCLK HIGH | TP3070 Only | **50** | | | ns |
| $t_{WFL}$ | Period of $F_{SX}$ or $F_{SR}$ Low | Measured from $V_{IL}$ to $V_{IL}$ | 1 | | | MCLK Period |
| **PCM INTERFACE TIMING** | | | | | | |
| $f_{BCLK}$ | Frequency of BCLK | May Vary from 64 kHz to 4096 kHz in 8 kHz Increments | **64** | | **4096** | kHz |
| $t_{WBH}$ | Period of BCLK High | Measured from $V_{IH}$ to $V_{IH}$ | **80** | | | ns |
| $t_{WBL}$ | Period of BCLK Low | Measured from $V_{IL}$ to $V_{IL}$ | **80** | | | ns |
| $t_{RB}$ | Rise Time of BCLK | Measured from $V_{IL}$ to $V_{IH}$ | | | 30 | ns |
| $t_{FB}$ | Fall Time of BCLK | Measured from $V_{IH}$ to $V_{IL}$ | | | 30 | ns |
| $t_{HBF}$ | Hold Time, BCLK Low to $FS_{X/R}$ High or Low | | **30** | | | ns |
| $t_{SFB}$ | Setup Time, $FS_{X/R}$ High to BCLK Low | | **30** | | | ns |
| $t_{DBD}$ | Delay Time, BCLK High to Data Valid | Load = 100 pF Plus 2 LSTTL Loads<br>$-40°C$ to $+85°C$ (TP3070-X) | | | **80**<br>90 | ns<br>ns |
| $t_{DBZ}$ | Delay Time, BCLK Low to $D_X0/1$ Disabled if $FS_X$ Low, $FS_X$ Low to $D_X0/1$ disabled if 8th BCLK Low, or BCLK High to $D_X0/1$ Disabled if $FS_X$ High | $D_X0/1$ Disabled is measured at $V_{OL}$ or $V_{OH}$ according to *Figure 5* or *Figure 6*<br><br>$-40°C$ to $+85°C$ (TP3070-X) | **15**<br><br>15 | | **80**<br><br>100 | ns<br><br>ns |
| $t_{DBT}$ | Delay Time, BCLK High to $\overline{TS_X}$ Low if $FS_X$ High, or $FS_X$ High to $\overline{TS_X}$ Low if BCLK High (Non Delayed Mode); BCLK High to $\overline{TS_X}$ Low (Delayed Data Mode) | Load = 100 pF Plus 2 LSTTL Loads | | | 60 | ns |
| $t_{ZBT}$ | TRI-STATE Time, BCLK Low to $\overline{TS_X}$ High if $FS_X$ Low, $FS_X$ Low to $\overline{TS_X}$ High if 8th BCLK Low, or BCLK High to $\overline{TS_X}$ High if $FS_X$ High | | 15 | | 60 | ns |
| $t_{DFD}$ | Delay Time, $FS_{X/R}$ High to Data Valid | Load = 100 pF Plus 2 LSTTL Loads, Applies if $FS_{X/R}$ Rises Later than BCLK Rising Edge in Non-Delayed Data Mode Only<br>$-40°C$ to $+85°C$ (TP3070-X) | | | **80**<br><br>90 | ns<br><br>ns |
| $t_{SDB}$ | Setup Time, $D_R0/1$ Valid to BCLK Low | | **30** | | | ns |
| $t_{HBD}$ | Hold Time, BCLK Low to $D_R0/1$ Invalid | $-40°C$ to $+85°C$ (TP3070-X) | **15**<br>15 | | | ns<br>ns |

**Note:** Applies only to MCLK Frequencies $\geq$ 1.536 MHz. At 512 kHz a 50:50 $\pm 2\%$ Duty Cycle must be used.
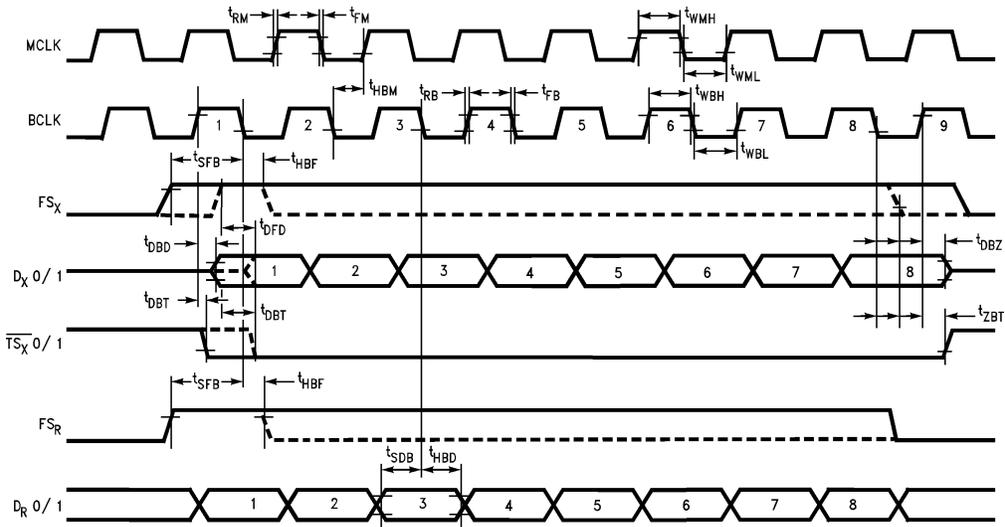
## Timing Specifications (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ ($-40°C$ to $+85°C$ for TP3070-X) by correlation with 100% electrical testing at $T_A = 25°C$. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at $V_{CC} = +5V$, $V_{BB} = -5V$, $T_A = 25°C$.

All timing parameters are measured at $V_{OH} = 2.0V$ and $V_{OL} = 0.7V$.

See Definitions and Timing Conventions section for test methods information.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **SERIAL CONTROL PORT TIMING** | | | | | | |
| $f_{CCLK}$ | Frequency of CCLK | | | | **2048** | kHz |
| $t_{WCH}$ | Period of CCLK High | Measured from $V_{IH}$ to $V_{IH}$ | **160** | | | ns |
| $t_{WCL}$ | Period of CCLK Low | Measured from $V_{IL}$ to $V_{IL}$ | **160** | | | ns |
| $t_{RC}$ | Rise Time of CCLK | Measured from $V_{IL}$ to $V_{IH}$ | | | 50 | ns |
| $t_{FC}$ | Fall Time of CCLK | Measured from $V_{IH}$ to $V_{IL}$ | | | 50 | ns |
| $t_{HCS}$ | Hold Time, CCLK Low to $\overline{CS}$ Low | CCLK1 | **10** | | | ns |
| $t_{HSC}$ | Hold Time, CCLK Low to $\overline{CS}$ High | CCLK 8 | **100** | | | ns |
| $t_{SSC}$ | Setup Time, $\overline{CS}$ Transition to CCLK Low | | **60** | | | ns |
| $t_{SSCO}$ | Setup Time, $\overline{CS}$ Transition to CCLK High | | 50 | | | ns |
| $t_{SDC}$ | Setup Time, CI (CI/O) Data In to CCLK Low | | **50** | | | ns |
| $t_{HCD}$ | Hold Time, CCLK Low to CI/O Invalid | | 50 | | | ns |
| $t_{DCD}$ | Delay Time, CCLK High to CI/O Data Out Valid | Load = 100 pF plus 2 LSTTL Loads<br>$-40°C$ to $+85°C$ (TP3070-X) | | | **80**<br>100 | ns<br>ns |
| $t_{DSD}$ | Delay Time, $\overline{CS}$ Low to CO (CI/O) Valid | Applies Only if Separate $\overline{CS}$ used for Byte 2<br>$-40°C$ to $+85°C$ (TP3070-X) | | | **80**<br><br>100 | ns<br><br>ns |
| $t_{DDZ}$ | Delay Time, $\overline{CS}$ or 9th CCLK High to CO (CI/O) High Impedance | Applies to Earlier of $\overline{CS}$ High or 9th CCLK High | 15 | | 80 | ns |
| **INTERFACE LATCH TIMING** | | | | | | |
| $t_{SLC}$ | Setup Time, IL to CCLK 8 of Byte 1 | Interface Latch Inputs Only | **100** | | | ns |
| $t_{HCL}$ | Hold Time, IL Valid from 8th CCLK Low (Byte 1) | | 50 | | | ns |
| $t_{DCL}$ | Delay Time CCLK 8 of Byte 2 to IL | Interface Latch Outputs Only<br>$C_L = 50$ pF | | | 200 | ns |
| **MASTER RESET PIN** | | | | | | |
| $t_{WMR}$ | Duration of Master Reset High | | 1 | | | $\mu s$ |

## Timing Diagrams



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**FIGURE 5. Non Delayed Data Timing Mode**
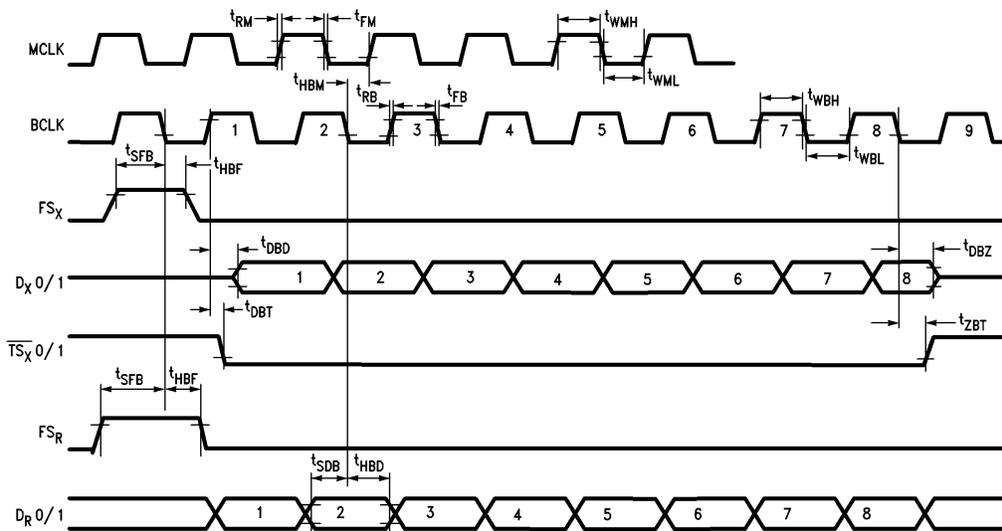


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**FIGURE 6. Delayed Data Timing Mode**
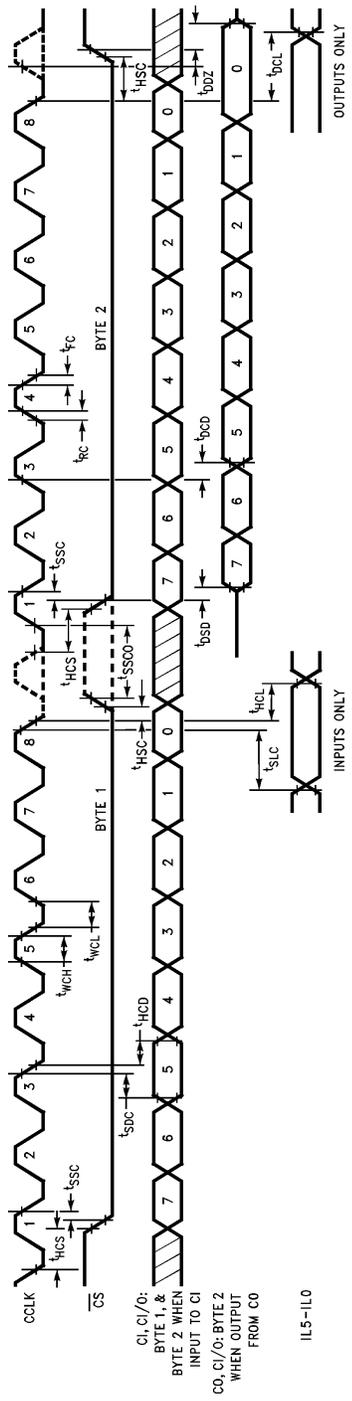**(Time Slot Zero Only)**

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# Timing Diagrams (Continued)



FIGURE 7. Control Port Timing

## Transmission Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for $V_{CC}$ = +5V ±5%, $V_{BB}$ = −5V ±5%; $T_A$ = 0°C to +70°C (−40°C to +85°C for TP3070-X) by correlation with 100% electrical testing at $T_A$ = 25°C. f = 1015.625 Hz, $VF_XI$ = 0 dBm0, $D_R0$ or $D_R1$ = 0 dBm0 PCM code. Transmit and receive gains programmed for maximum 0 dBm0 test levels (0 dB gain), hybrid balance filter disabled. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at $V_{CC}$ = +5V, $V_{BB}$ = −5V, $T_A$ = 25°C.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **AMPLITUDE RESPONSE** | | | | | | |
| | Absolute Levels | The Maximum 0 dBm0 Levels are: | | | | |
| | | $VF_XI$ | | 1.619 | | Vrms |
| | | $VF_RO$ (15 kΩ Load) | | 1.964 | | Vrms |
| | | The Minimum 0 dBm0 Levels are: | | | | |
| | | $VF_XI$ | | 87.0 | | mVrms |
| | | $VF_RO$ (Any Load ≥ 300Ω) | | 105.0 | | mVrms |
| | | Overload Levels are 3.17 dBm0 (μLaw) and 3.14 dBm0 (A-Law) | | | | |
| $G_{XA}$ | Transmit Gain Absolute Accuracy | Transmit Gain Programmed for Maximum 0 dBm0 Test Level. (All 1's in gain register) Measure Deviation of Digital Code from Ideal 0 dBm0 PCM Code at $D_X0/1$. $T_A$ = 25°C | **−0.15** | | **0.15** | dB |
| $G_{XAG}$ | Transmit Gain Variation with Programmed Gain | $T_A$ = 25°C, $V_{CC}$ = 5V, $V_{BB}$ = 5V Programmed Gain from 0 dB to 19 dB (0 dBm0 Levels of 1.619 Vrms to 0.182 Vrms) | **−0.1** | | **0.1** | dB |
| | | Programmed Gain from 19.1 dB to 25.4 dB (0 dBm0 Levels of 0.180 Vrms to 0.087 Vrms) | **−0.3** | | **0.3** | dB |
| | | **Note:** ±0.1 dB min/max is available as a selected part. | | | | |
| $G_{XAF}$ | Transmit Gain Variation with Frequency | Relative to 1015.625 Hz, (Note 4) Minimum Gain < $G_X$ < Maximum Gain | | | | |
| | | f = 60 Hz | | | −26 | dB |
| | | f = 200 Hz | −1.8 | | −0.1 | dB |
| | | f = 300 Hz to 3000 Hz | −0.15 | | 0.15 | dB |
| | | f = 3400 Hz | −0.7 | | 0.0 | dB |
| | | f = 4000 Hz | | | −14 | dB |
| | | f ≥ 4600 Hz. Measure Response at Alias Frequency from 0 kHz to 4 kHz. $G_X$ = 0 dB, $VF_XI$ = 1.619 Vrms | | | −32 | dB |
| | | Relative to 1015.625 Hz | | | | |
| | | f = 62.5 Hz | | | **−24.9** | dB |
| | | f = 203.125 Hz | **−1.7** | | **−0.1** | dB |
| | | f = 343.75 Hz | **−0.15** | | **0.15** | dB |
| | | f = 515.625 Hz | **−0.15** | | **0.15** | dB |
| | | f = 2140.625 Hz | **−0.15** | | **0.15** | dB |
| | | f = 3156.25 Hz | **−0.15** | | **0.15** | dB |
| | | f = 3406.250 Hz | **−0.74** | | **0.0** | dB |
| | | f = 3984.375 Hz | | | **−13.5** | dB |
| | | Relative to 1062.5 Hz (Note 4) | | | | |
| | | f = 5250 Hz, Measure 2750 Hz | | | **−32** | dB |
| | | f = 11750 Hz, Measure 3750 Hz | | | **−32** | dB |
| | | f = 49750 Hz, Measure 1750 Hz | | | **−32** | dB |

## Transmission Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ ($-40°C$ to $+85°C$ for TP3070-X) by correlation with 100% electrical testing at $T_A = 25°C$. $f = 1015.625$ Hz, $VF_X I = 0$ dBm0, $D_R 0$ or $D_R 1 = 0$ dBm0 PCM code. Transmit and receive gains programmed for maximum 0 dBm0 test levels (0 dB gain), hybrid balance filter disabled. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at $V_{CC} = +5V$, $V_{BB} = -5V$, $T_A = 25°C$.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--------|-----------|------------|-----|-----|-----|-------|
| **AMPLITUDE RESPONSE** (Continued) | | | | | | |
| $G_{XAT}$ | Transmit Gain Variation with Temperature | Measured Relative to $G_{XA}$, $V_{CC} = 5V$, $V_{BB} = -5V$, Minimum gain $< G_X <$ Maximum Gain | −0.1 | | 0.1 | dB |
| | | −40°C to +85°C (TP3070-X) | −0.15 | | 0.15 | dB |
| $G_{XAL}$ | Transmit Gain Variation with Signal Level | Sinusoidal Test Method. Reference Level = 0 dBm0. | | | | |
| | | $VF_X I = -40$ dBm0 to +3 dBm0 | **−0.2** | | **0.2** | dB |
| | | $VF_X I = -50$ dBm0 to −40 dBm0 | **−0.4** | | **0.4** | dB |
| | | $VF_X I = -55$ dBm0 to −50 dBm0 | **−1.2** | | **1.2** | dB |
| $G_{RA}$ | Receive Gain Absolute Accuracy | Receive Gain Programmed for Maximum 0 dBm0 Test Level (All 1's in Gain Register). Apply 0 dBm0 PCM Code to $D_R 0$ or $D_R 1$. Measure $VF_R O$. | | | | |
| | | $T_A = 25°C$ | **−0.15** | | **0.15** | dB |
| $G_{RAG}$ | Receive Gain Variation with Programmed Gain | $T_A = 25°C$, $V_{CC} = 5V$, $V_{BB} = -5V$ Programmed Gain from 0 dB to 19 dB (0 dBm0 Levels of 1.964 Vrms to 0.220 Vrms) | **−0.1** | | **0.1** | dB |
| | | Programmed Gain from 19.1 dB to 25.4 dB (0 dBm0 Levels of 0.218 Vrms to 0.105 Vrms) | **−0.3** | | **0.3** | dB |
| | | Note: ±0.1 dB min/max is available as a selected part. | | | | |
| $G_{RAT}$ | Receive Gain Variation with Temperature | Measured Relative to $G_{RA}$. $V_{CC} = 5V$, $V_{BB} = -5V$. Minimum Gain $< G_R <$ Maximum Gain | −0.1 | | 0.1 | dB |
| | | −40°C to +85°C (TP3070-X) | −0.15 | | 0.15 | dB |
| $G_{RAF}$ | Receive Gain Variation with Frequency | Relative to 1015.625 Hz, (Note 4) $D_R 0$ or $D_R 1 = 0$ dBm0 code. Minimum Gain $< G_R <$ Maximum Gain | | | | |
| | | f = 200 Hz | −0.25 | | 0.15 | dB |
| | | f = 300 Hz to 3000 Hz | −0.15 | | 0.15 | dB |
| | | f = 3400 Hz | −0.7 | | 0.0 | dB |
| | | f = 4000 Hz | | | −14 | dB |
| | | $G_R = 0$ dB, $D_R 0 = 0$ dBm0 Code, $G_X = 0$ dB (Note 4) | | | | |
| | | f = 296.875 Hz | **−0.15** | | **0.15** | dB |
| | | f = 1875.00 Hz | **−0.15** | | **0.15** | dB |
| | | f = 2906.25 Hz | **−0.15** | | **0.15** | dB |
| | | f = 2984.375 Hz | **−0.15** | | **0.15** | dB |
| | | f = 3406.250 Hz | **−0.74** | | **0.0** | dB |
| | | f = 3984.375 Hz | | | **−13.5** | dB |

## Transmission Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ ($-40°C$ to $+85°C$ for TP3070-X) by correlation with 100% electrical testing at $T_A = 25°C$. $f = 1015.625$ Hz, $VF_X I = 0$ dBm0, $D_R 0$ or $D_R 1 = 0$ dBm0 PCM code. Transmit and receive gains programmed for maximum 0 dBm0 test levels (0 dB gain), hybrid balance filter disabled. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at $V_{CC} = +5V$, $V_{BB} = -5V$, $T_A = 25°C$.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **AMPLITUDE RESPONSE** (Continued) | | | | | | |
| $G_{RAL}$ | Receive Gain Variation with Signal Level | Sinusoidal Test Method. Reference Level = 0 dBm0. | | | | |
| | | $D_R 0 = -40$ dBm0 to $+3$ dBm0 | **−0.2** | | **0.2** | dB |
| | | $D_R 0 = -50$ dBm0 to $-40$ dBm0 | **−0.4** | | **0.4** | dB |
| | | $D_R 0 = -55$ dBm0 to $-50$ dBm0 | **−1.2** | | **1.2** | dB |
| | | $D_R 0 = 3.1$ dBm0 | | | | |
| | | $R_L = 600\Omega$, $G_R = -0.5$ dB | −0.2 | | 0.2 | dB |
| | | $R_L = 300\Omega$, $G_R = -1.2$ dB | **−0.2** | | **0.2** | dB |
| **ENVELOPE DELAY DISTORTION WITH FREQUENCY** | | | | | | |
| $D_{XA}$ | Tx Delay, Absolute | $f = 1600$ Hz | | | 315 | $\mu s$ |
| $D_{XR}$ | Tx Delay, Relative to $D_{XA}$ | $f = 500-600$ Hz | | | 220 | $\mu s$ |
| | | $f = 600-800$ Hz | | | 145 | $\mu s$ |
| | | $f = 800-1000$ Hz | | | 75 | $\mu s$ |
| | | $f = 1000-1600$ Hz | | | 40 | $\mu s$ |
| | | $f = 1600-2600$ Hz | | | 75 | $\mu s$ |
| | | $f = 2600-2800$ Hz | | | 105 | $\mu s$ |
| | | $f = 2800-3000$ Hz | | | 155 | $\mu s$ |
| $D_{RA}$ | Rx Delay, Absolute | $f = 1600$ Hz | | | 200 | $\mu s$ |
| $D_{RR}$ | Rx Delay, Relative to $D_{RA}$ | $f = 500-1000$ Hz | −40 | | | $\mu s$ |
| | | $f = 1000-1600$ Hz | −30 | | | $\mu s$ |
| | | $f = 1600-2600$ Hz | | | 90 | $\mu s$ |
| | | $f = 2600-2800$ Hz | | | 125 | $\mu s$ |
| | | $f = 2800-3000$ Hz | | | 175 | $\mu s$ |
| **NOISE** | | | | | | |
| $N_{XC}$ | Transmit Noise, C Message Weighted, $\mu$-law Selected | (Note 1) All '1's in Gain Register | | 12 | **15** | dBrnC0 |
| $N_{XP}$ | Transmit Noise, P Message Weighted, A-law Selected | (Note 1) All '1's in Gain Register | | −74 | **−67** | dBm0p |
| $N_{RC}$ | Receive Noise, C Message Weighted, $\mu$-law Selected | PCM Code is Alternating Positive and Negative Zero | | 8 | **11** | dBrnC0 |
| $N_{RP}$ | Receive Noise, P Message Weighted, A-law Selected | PCM Code Equals Positive Zero | | −82 | **−79** | dBm0p |
| $N_{RS}$ | Noise, Single Frequency | $f = 0$ kHz to 100 kHz, Loop Around Measurement, $VF_X I = 0$ Vrms | | | −53 | dBm0 |
| $PPSR_X$ | Positive Power Supply Rejection, Transmit | $V_{CC} = 5.0$ $V_{DC} + 100$ mVrms | | | | |
| | | $f = 0$ kHz–4 kHz (Note 2) | **36** | | | dBC |
| | | $f = 4$ kHz–50 kHz | 30 | | | dBC |
| $NPSR_X$ | Negative Power Supply Rejection, Transmit | $V_{BB} = -5.0$ $V_{DC} + 100$ mVrms | | | | |
| | | $f = 0$ kHz–4 kHz (Note 2) | **36** | | | dBC |
| | | $f = 4$ kHz–50 kHz | 30 | | | dBC |
| $PPSR_R$ | Positive Power Supply Rejection, Receive | PCM Code Equals Positive Zero $V_{CC} = 5.0$ $V_{DC} + 100$ mVrms Measure $VF_R O$ | | | | |
| | | $f = 0$ Hz–4000 Hz | **36** | | | dBC |
| | | $f = 4$ kHz–25 kHz | 40 | | | dB |
| | | $f = 25$ kHz–50 kHz | 36 | | | dB |

## Transmission Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ ($-40°C$ to $+85°C$ for TP3070-X) by correlation with 100% electrical testing at $T_A = 25°C$. $f = 1015.625$ Hz, $VF_X I = 0$ dBm0, $D_R 0$ or $D_R 1 = 0$ dBm0 PCM code. Transmit and receive gains programmed for maximum 0 dBm0 test levels (0 dB gain), hybrid balance filter disabled. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at $V_{CC} = +5V$, $V_{BB} = -5V$, $T_A = 25°C$.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **NOISE** (Continued) | | | | | | |
| $NPSR_R$ | Negative Power Supply Rejection, Receive | PCM Code Equals Positive Zero $V_{BB} = -5.0$ $V_{DC} + 100$ mVrms Measure $VF_R O$ | | | | |
| | | f = 0 Hz–4000 Hz | **36** | | | dBC |
| | | f = 4 kHz–25kHz | 40 | | | dB |
| | | f = 25 kHz–50 kHz | 36 | | | dB |
| SOS | Spurious Out-of-Band Signals at the Channel Output | 0 dBm0, 300 Hz to 3400 Hz Input PCM Code Applied at $D_R 0$ (or $D_R 1$) | | | | |
| | | 4600 Hz–7600 Hz | | | **−30** | dB |
| | | 7600 Hz–8400 Hz | | | **−40** | dB |
| | | 8400 Hz–50,000 Hz | | | **−30** | dB |
| **DISTORTION** | | | | | | |
| $STD_X$ $STD_R$ | Signal to Total Distortion Transmit or Receive Half-Channel, μ-law Selected | Sinusoidal Test Method Level = 3.0 dBm0 | **33** | | | dBC |
| | | = 0 dBm0 to − 30 dBm0 | **36** | | | dBC |
| | | = −40 dBm0 | **30** | | | dBC |
| | | = −45 dBm0 | **25** | | | dBC |
| $STD_{RL}$ | Signal to Total Distortion Receive with Resistive Load | Sinusoidal Test Method Level = +3.1 dBm0 | | | | |
| | | $R_L = 600Ω$, $G_R = -0.5$ dB | 33 | | | dBC |
| | | $R_L = 300Ω$, $G_R = -1.2$ dB | **33** | | | dBC |
| $SFD_X$ | Single Frequency Distortion, Transmit | | | | **−46** | dB |
| $SFD_R$ | Single Frequency Distortion, Receive | | | | **−46** | dB |
| IMD | Intermodulation Distortion | Transmit or Receive Two Frequencies in the Range 300 Hz–3400 Hz | | | **−41** | dB |
| **CROSSTALK** | | | | | | |
| $CT_{X-R}$ | Transmit to Receive Crosstalk, 0 dBm0 Transmit Level | f = 300 Hz–3400 Hz $D_R$ = Idle Code | | −90 | **−75** | dB |
| $CT_{R-X}$ | Receive to Transmit Crosstalk, 0 dBm0 Receive Level | f = 300 Hz–3400 Hz (Note 2) | | −90 | **−70** | dB |

**Note 1:** Measured by grounded input at $VF_X I$.

**Note 2:** $PPSR_X$, $NPSR_X$, and $CT_{R-X}$ are measured with a −50 dBm0 activation signal applied to $VF_X I$.

**Note 3:** A signal is Valid if it is above $V_{IH}$ or below $V_{IL}$ and Invalid if it is between $V_{IL}$ and $V_{IH}$. For the purposes of this specification the following conditions apply:

    a) All input signals are defined as: $V_{IL} = 0.4V$, $V_{IH} = 2.7V$, $t_R < 10$ ns, $t_F < 10$ ns.

    b) $t_R$ is measured from $V_{IL}$ to $V_{IH}$. $t_F$ is measured from $V_{IH}$ to $V_{IL}$.

    c) Delay Times are measured from the input signal Valid to the output signal Valid.

    d) Setup Times are measured from the data input Valid to the clock input Invalid.

    e) Hold Times are measured from the clock signal Valid to the data input Invalid.

    f) Pulse widths are measured from $V_{IL}$ to $V_{IL}$ or from $V_{IH}$ to $V_{IH}$.

**Note 4:** A multi-tone test technique is used.

# Definitions and Timing Conventions

## DEFINITIONS

$V_{IH}$ — $V_{IH}$ is the D.C. input level above which an input level is guaranteed to appear as a logical one. This parameter is to be measured by performing a functional test at reduced clock speeds and nominal timing, (i.e., not minimum setup and hold times or output strobes), with the high level of all driving signals set to $V_{IH}$ and maximum supply voltages applied to the device.

$V_{IL}$ — $V_{IL}$ is the D.C. input level below which an input level is guaranteed to appear as a logical zero to the device. This parameter is measured in the same manner as $V_{IH}$ but with all driving signal low levels set to $V_{IL}$ and minimum supply voltages applied to the device.

$V_{OH}$ — $V_{OH}$ is the minimum D.C. output level to which an output placed in a logical one state will converge when loaded at the maximum specified load current.

$V_{OL}$ — $V_{OL}$ is the maximum D.C. output level to which an output placed in a logical zero state will converge when loaded at the maximum specified load current.

Threshold Region — The threshold region is the range of input voltages between $V_{IL}$ and $V_{IH}$.

Valid Signal — A signal is Valid if it is in one of the valid logic states. (i.e., above $V_{IH}$ or below $V_{IL}$). In timing specifications, a signal is deemed valid at the instant it enters a valid state.

Invalid signal — A signal is invalid if it is not in a valid logic state, i.e., when it is in the threshold region between $V_{IL}$ and $V_{IH}$. In timing specifications, a signal is deemed Invalid at the instant it enters the threshold region.

## TIMING CONVENTIONS

For the purposes of this timing specification the following conventions apply.

Input Signals — All input signals may be characterized as: $V_L = 0.4V$, $V_H = 2.4V$, $t_R < 10$ ns, $t_F < 10$ ns.

Period — The period of the clock signal is designated as $t_{Pxx}$ where $_{xx}$ represents the mnemonic of the clock signal being specified.

Rise Time — Rise times are designated as $t_{Ryy}$, where yy represents a mnemonic of the signal whose rise time is being specified. $t_{Ryy}$ is measured from $V_{IL}$ to $V_{IH}$.

Fall Time — Fall times are designated as $t_{Fyy}$, where yy represents a mnemonic of the signal whose fall time is being specified. $t_{Fyy}$ is measured from $V_{IH}$ to $V_{IL}$.

Pulse Width High — The high pulse width is designated as $t_{WzzH}$, where zz represents the mnemonic of the input or output signal whose pulse width is being specified. High pulse widths are measured from $V_{IH}$ to $V_{IH}$.

Pulse Width Low — The low pulse width is designated as $t_{WzzL}$, where zz represents the mnemonic of the input or output signal whose pulse width is being specified. Low pulse widths are measured from $V_{IL}$ to $V_{IL}$.

Setup Time — Setup times are designated as $t_{Swwxx}$, where ww represents the mnemonic of the input signal whose setup time is being specified relative to a clock or strobe input represented by mnemonic xx. Setup times are measured from the ww Valid to xx Invalid.

Hold Time — Hold times are designated as $T_{Hwwxx}$, where ww represents the mnemonic of the input signal whose hold time is being specified relative to a clock or strobe input represented by the mnemonic xx. Hold times are measured from xx Valid to ww Invalid.

Delay Time — Delay times are designated as $T_{Dxxyy}$[ IHIL], where xx represents the mnemonic of the input reference signal and yy represents the mnemonic of the output signal whose timing is being specified relative to xx. The mnemonic may optionally be terminated by an H or L to specify the high going or low going transition of the output signal. Maximum delay times are measured from xx Valid to yy Valid. Minimum delay times are measured from xx Valid to yy Invalid. This parameter is tested under the load conditions specified in the Conditions column of the Timing Specifications section of this datasheet.

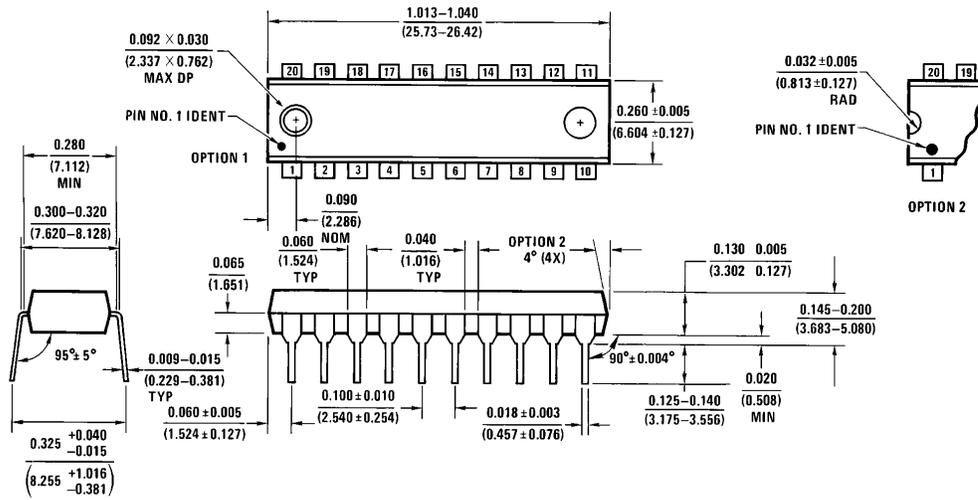# Physical Dimensions inches (millimeters)
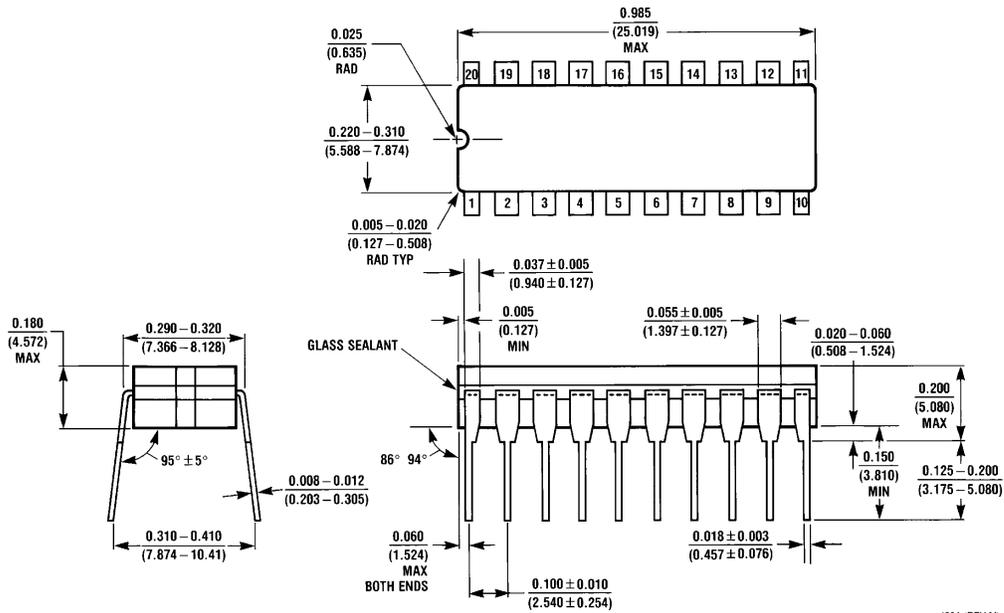
Ceramic Dual-In-Line Package (J)
Order Number TP3071J
NS Package Number J20A
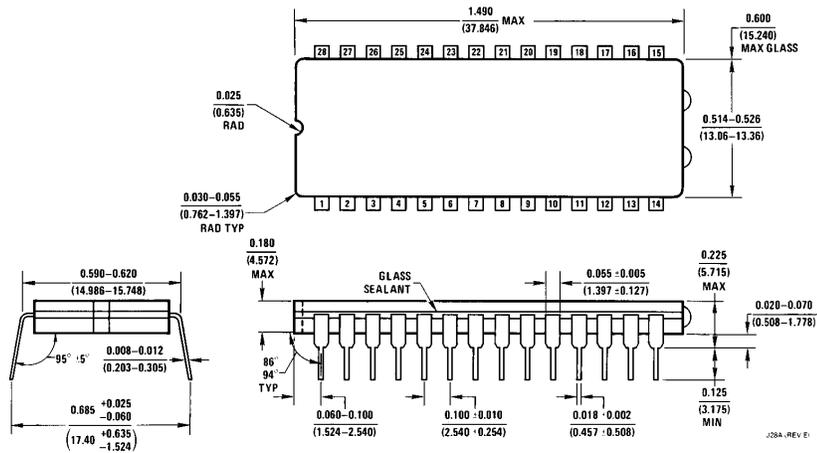
Ceramic Dual-In-Line Package (J)
Order Number TP3070J
NS Package Number J28A

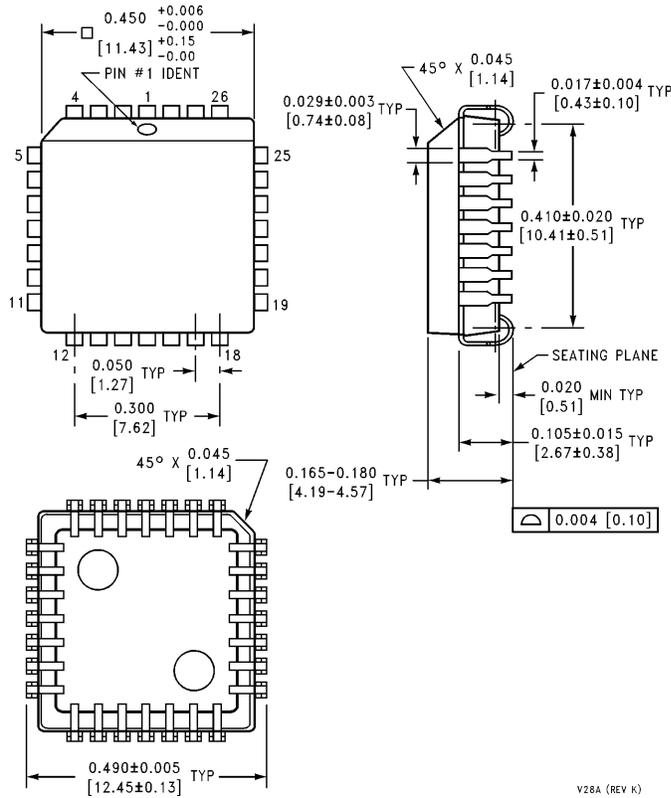## Physical Dimensions inches (millimeters) (Continued)



**Molded Dual-In-Line (N)**
**Order Number TP3071N**
**NS Package Number N20A**

N20A (REV G)

**Physical Dimensions** inches (millimeters) (Continued)

0.450 +0.006 / −0.000
[11.43] +0.15 / −0.00

PIN #1 IDENT

4    1    26

5    25

11    19

12    18

0.050 TYP
[1.27]

0.300 TYP
[7.62]

45° X 0.045
[1.14]

0.490±0.005 TYP
[12.45±0.13]

0.029±0.003 TYP
[0.74±0.08]

45° X 0.045
[1.14]

0.017±0.004 TYP
[0.43±0.10]

0.410±0.020 TYP
[10.41±0.51]

SEATING PLANE

0.020 MIN TYP
[0.51]

0.105±0.015 TYP
[2.67±0.38]

0.165−0.180 TYP
[4.19−4.57]

0.004 [0.10]

V28A (REV K)

**Plastic Leaded Chip Carrier (V)**
**Order Number TP3070V or TP3070V-X**
**NS Package Number V28A**

**LIFE SUPPORT POLICY**

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.