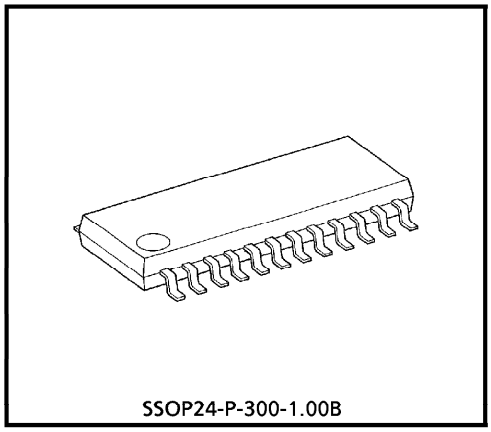
TOSHIBA INTELLIGENT POWER DEVICE SILICON MONOLITHIC POWER MOS INTEGRATED CIRCUIT

TPD2007F

LOW-SIDE POWER SWITCH ARRAY (8 CHANNELS) for MOTORS, SOLENOIDS, and LAMP DRIVES

The TPD2007F is an 8-channel low-side switch array for vertical power MOS FET output. A monolithic power IC, it can directly drive a power load from a CMOS or TTL logic circuit (such as an MPU). It offers overcurrent and overtemperature protection functions.



SSOP24-P-300-1.00B

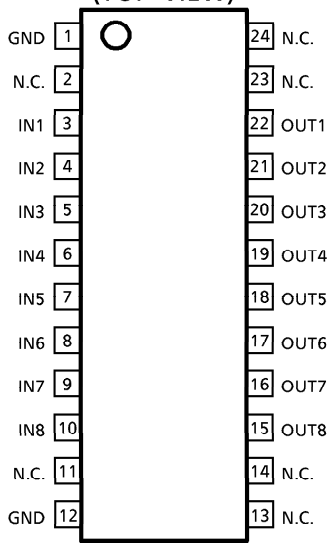
Weight : 0.29 g (typ.)

FEATURES

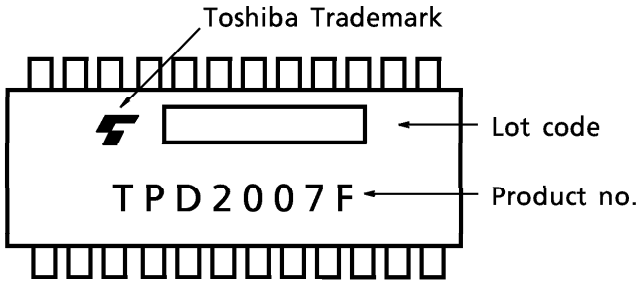
- A low-side switch array incorporating an N-channel power MOS FET. (1.4 Ω max.)
- Can directly drive a power load from a microprocessor.
- Built-in protection against overtemperature protection and overcurrent protection.
- 8-channel access enables space-saving design.
- High operating voltage : 40 V
- Low on-resistance : 1.4 Ω max. @V_{DD} = 12 V, I_O = 0.5 A (per channel)
- Supports parallel operation.
- Built-in an active clamp circuit
- Supplied in an SSOP-24 package (300 mil) in embossed taping.

PIN ASSIGNMENT

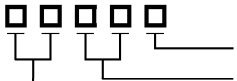
(TOP VIEW)



MARKING



Lot code naming system



Toshiba house no.
Manufactured week (52 weeks or 53 weeks indicating system starting from the first Thursday of January)
Manufactured year (last two digits of the year)

This device uses MOS structure, it is sensitive to electrostatics. Please take this into account.

980910EBA2

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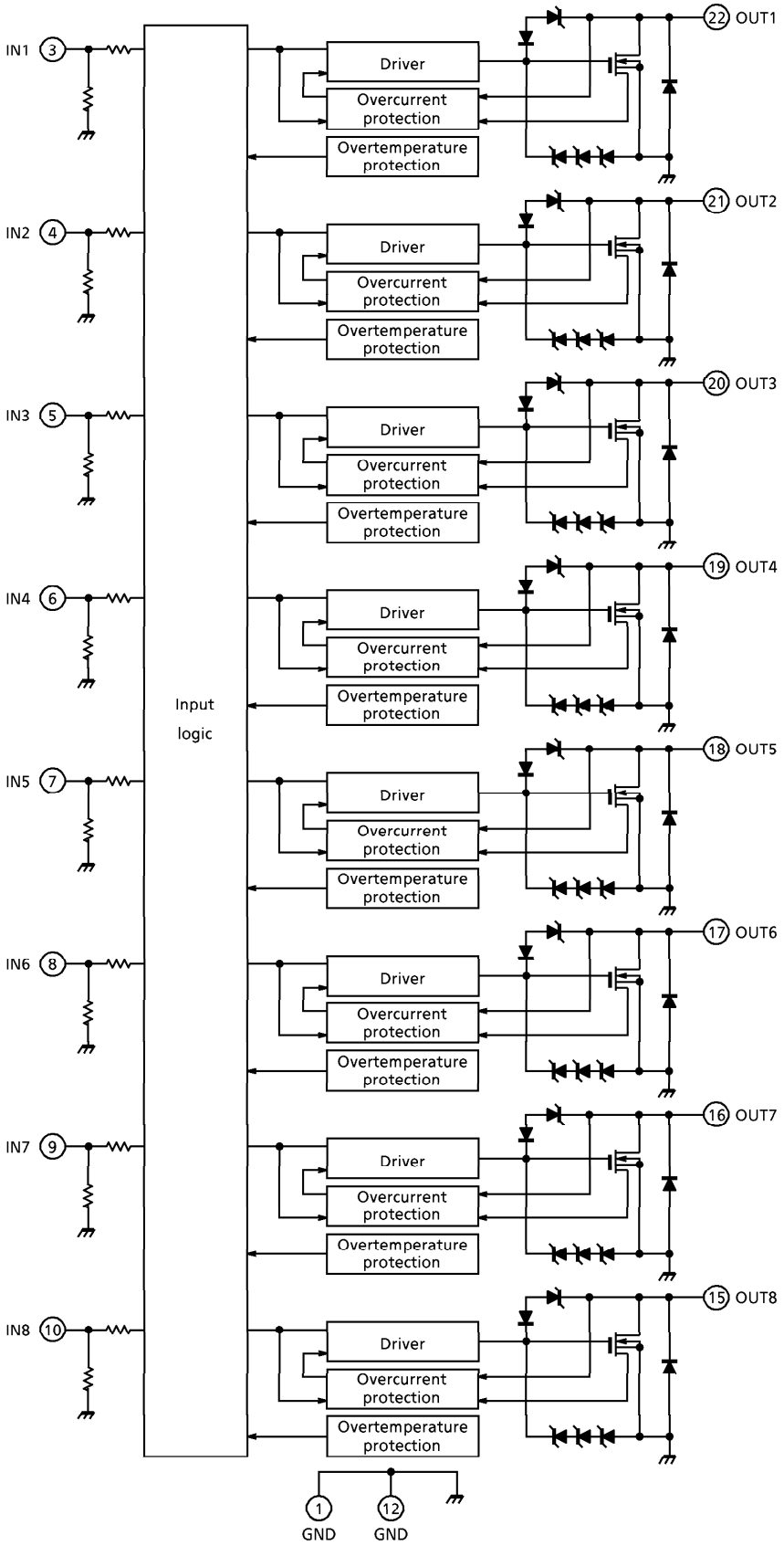
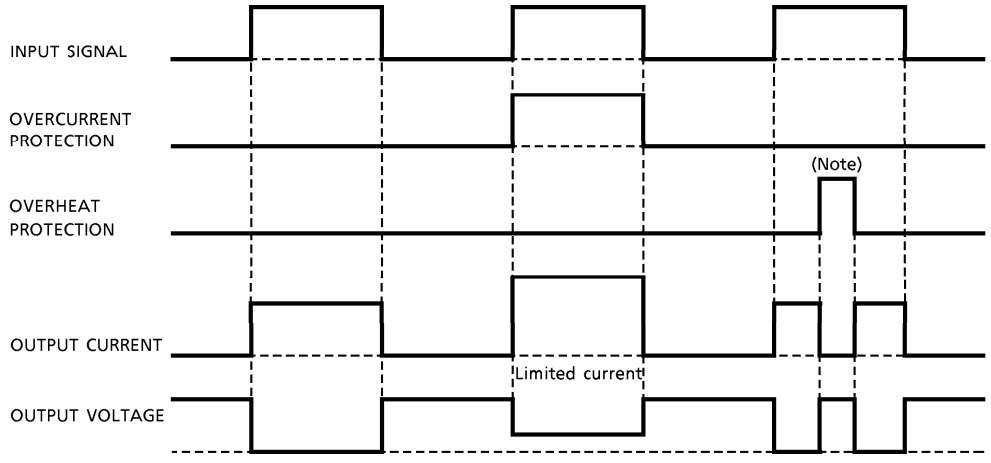
BLOCK DIAGRAM



PIN DESCRIPTION

PIN No.	SYMBOL	DESCRIPTION
1	GND	GND pin; in common with the pin no.12 internally.
2	N.C.	—
3	IN1	Control input pin for channel 1 and built-in pull-down resistor (300 kΩ typ.)
4	IN2	Control input pin for channel 2 and built-in pull-down resistor (300 kΩ typ.)
5	IN3	Control input pin for channel 3 and built-in pull-down resistor (300 kΩ typ.)
6	IN4	Control input pin for channel 4 and built-in pull-down resistor (300 kΩ typ.)
7	IN5	Control input pin for channel 5 and built-in pull-down resistor (300 kΩ typ.)
8	IN6	Control input pin for channel 6 and built-in pull-down resistor (300 kΩ typ.)
9	IN7	Control input pin for channel 7 and built-in pull-down resistor (300 kΩ typ.)
10	IN8	Control input pin for channel 8 and built-in pull-down resistor (300 kΩ typ.)
11	N.C.	—
12	GND	GND pin; in common with the pin no.1 internally.
13	N.C.	—
14	N.C.	—
15	OUT8	Output pin for channel 8
16	OUT7	Output pin for channel 7
17	OUT6	Output pin for channel 6
18	OUT5	Output pin for channel 5
19	OUT4	Output pin for channel 4
20	OUT3	Output pin for channel 3
21	OUT2	Output pin for channel 2
22	OUT1	Output pin for channel 1
23	N.C.	—
24	N.C.	—

TIMING CHART



(Note) : The overheating detector circuits feature hysteresis. After overheating is detected, normal operation is restored only when the junction temperature falls by the hysteresis amount (10°C typ.) in relation to the overheating detection temperature.

TRUTH TABLE

INPUT SIGNAL	OUTPUT SIGNAL	STATE
L	H	Normal
H	L	
L	H	Overcurrent protection
H	Internally limited	
L	H	Overtemperature protection
H	H	

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Input Voltage	V_{IN}	−0.5~7	V
Drain-source Voltage	V_{DSS}	40	V
Output Current	I_D	Internally Limited	A
Power Dissipation (Operating All Channels, Ta = 25°C)	P_T	0.8	W
		1.5 (Note)	
Single Pulse Avalanche Energy	E_{AS}	10	mJ
Operating Temperature	T_{opr}	−40~85	°C
Junction Temperature	T_j	150	°C
Storage Temperature	T_{stg}	−55~150	°C

THERMAL CHARACTERISTIC

CHARACTERISTIC	SYMBOL	RATING	UNIT
Thermal Resistance Junction to Ambient (Operating All Channels, Ta = 25°C)	$\Sigma R_{th\ (j\text{-}a)}$	156.3	°C / W
		83.4 (Note)	

(Note) : 60 mm × 60 mm × 1.6 t when a device is mounted on a glass epoxy PCB. (DC)

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Drain-Source Clamp Voltage		$V_{(BR)\ DSS}$	—	I_D = 10 mA, V_{IN} = 0 V	40	—	—	
Input Voltage		V_{th}	—	V_{DS} = 24 V, I_{DS} = 1 mA	0.8	—	2.0	V
Input Current		I_{IL}	—	V_{IN} = 0 V	− 10	—	10	μA
		I_{IH}	—	V_{IN} = 5 V	—	140	300	
On Resistance		$R_{DS\ (ON)}$	—	V_{IN} = 5 V, I_O = 0.5 A	—	1.0	1.4	Ω
Off Current		I_{DSS}	—	V_{DS} = 40V	—	—	100	μA
Overcurrent Protection		$I_{S\ (1)}$	—	V_{DS} = 12 V, V_{IN} = 5 V, R_L = 3 Ω	1	2	3	A
		$I_{S\ (2)}$	—	V_{DS} = 30 V, V_{IN} = 5 V, R_L = 3 Ω	0.7	—	2	
Overtemperature Protection	Temperature	TSD	—	V_{IN} = 5 V	—	160	—	°C
	Hysteresis	ΔTSD	—	—	—	10	—	
Switching Time		t_{ON}	1	V_{DD} = 12 V, R_L = 24 Ω, V_{IN} = 0 V / 5 V	—	10	50	μs
		t_{OFF}	1		—	10	50	
Operating Input Voltage Protection Circuit		$V_{IN\ (P)}$	—	—	4.5	—	6.0	V
Drain-Source Diode Forward Voltage		V_{DSF}	—	IF = 1 A, V_{IN} = 0 V	—	—	1.6	V

DESCRIPTION OF PROTECTOR CIRCUIT

(1) Overtemperature Protection

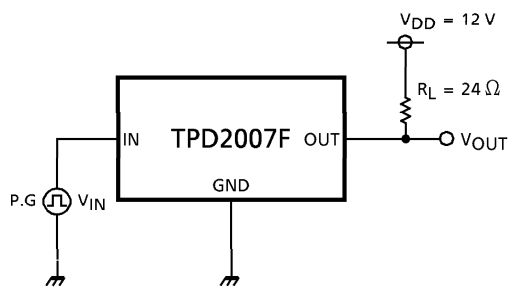
- The overheating detector circuits feature hysteresis. After overheating is detected, normal operation is restored only when the junction temperature falls by the hysteresis amount (10°C typ.) in relation to the overheating detection temperature.

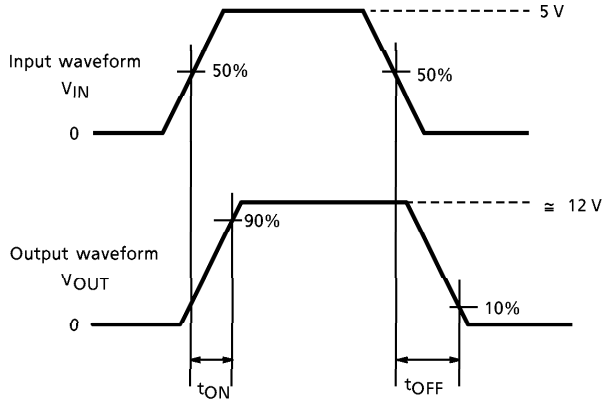
(2) Overcurrent Protection

- When overcurrent is detected, the overcurrent limiter function limits the output current. Normal operation is restored when the load current drops below the overcurrent detection value.

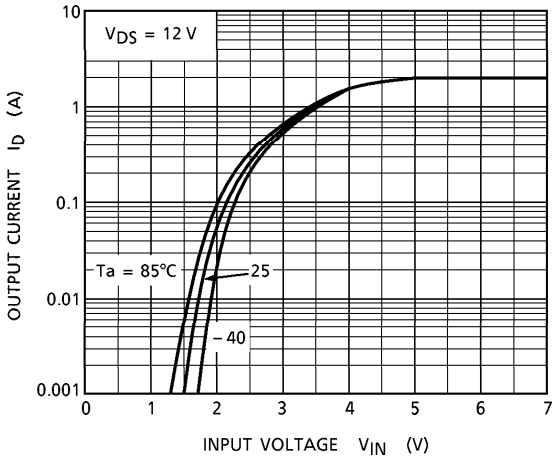
TEST CIRCUIT

Switching Time

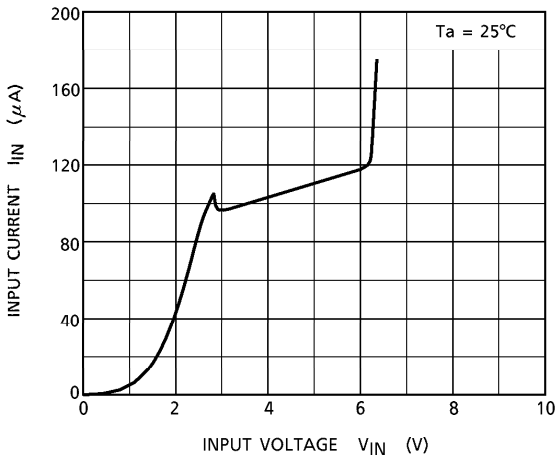




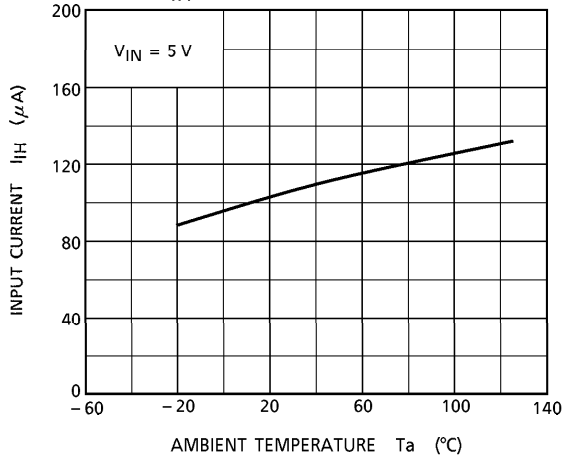
I_D – V_{IN} (FOR EACH CHANNEL)



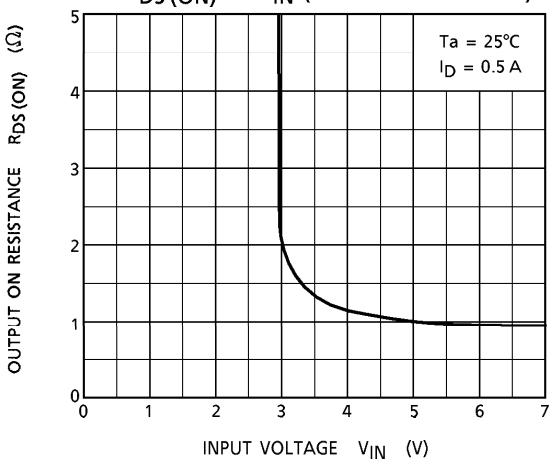
I_{IN} – V_{IN} (FOR EACH CHANNEL)



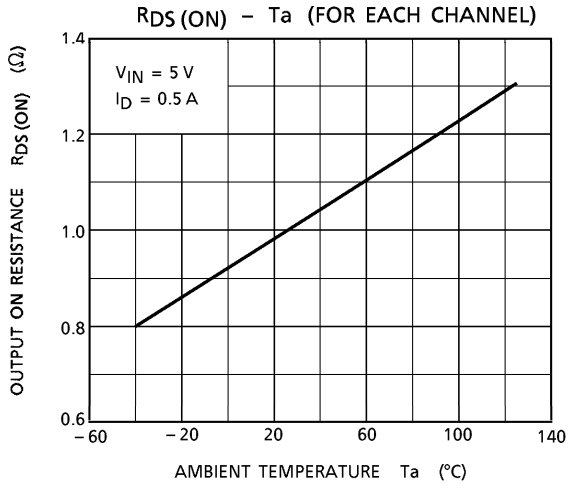
I_{IH} – Ta (FOR EACH CHANNEL)



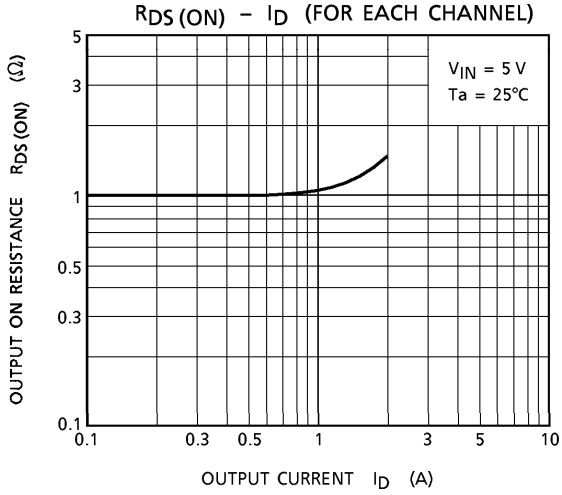
$R_{DS\,(ON)}$ – V_{IN} (FOR EACH CHANNEL)



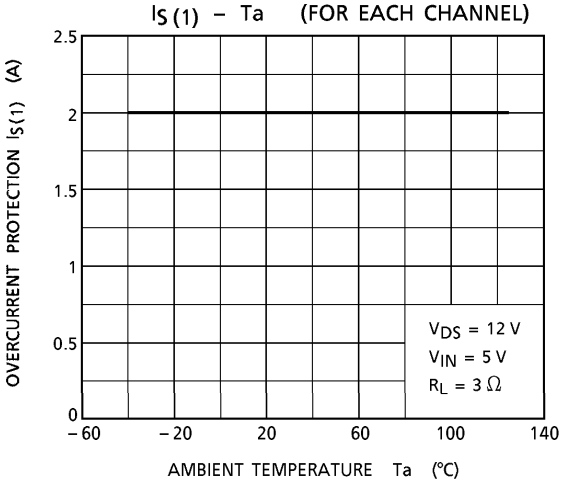
$R_{DS\,(ON)}$ – Ta (FOR EACH CHANNEL)



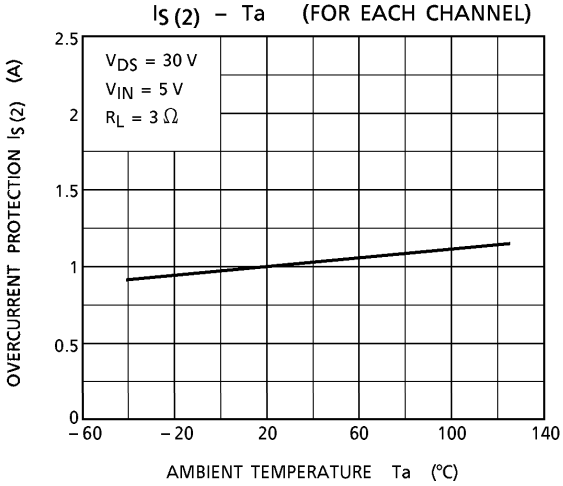
$R_{DS\,(ON)}$ – I_D (FOR EACH CHANNEL)



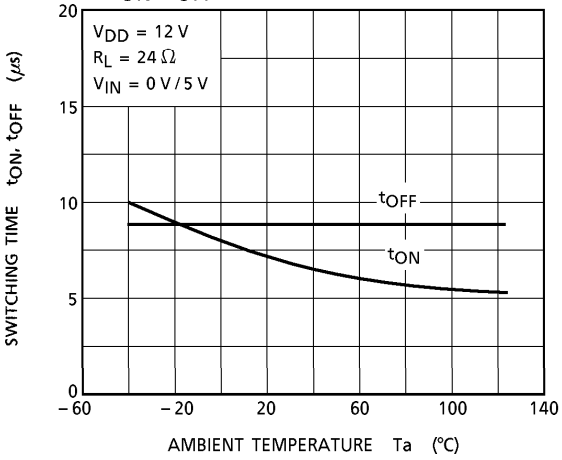
$I_{S(1)}$ – Ta (FOR EACH CHANNEL)



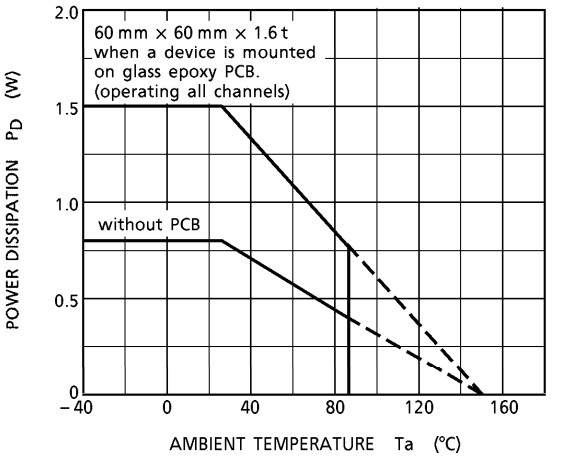
$I_{S(2)}$ – Ta (FOR EACH CHANNEL)



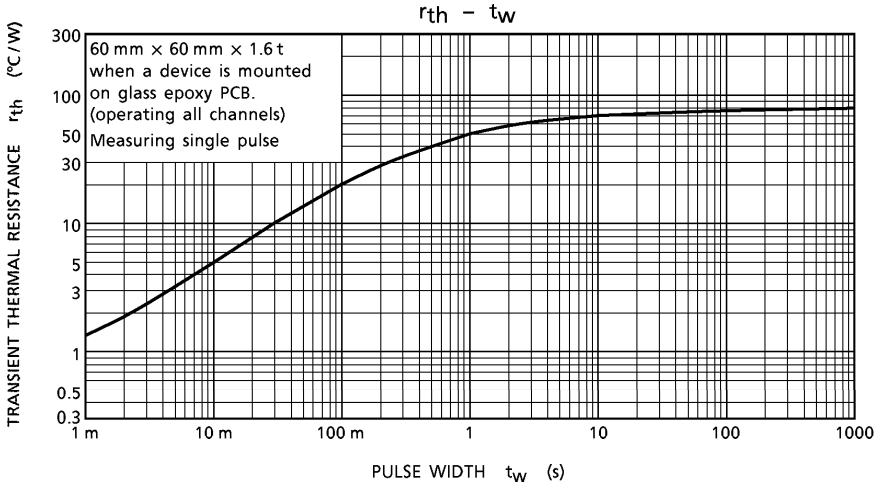
t_{ON}, t_{OFF} – Ta (FOR EACH CHANNEL)



P_D – Ta



r_{th} – t_W

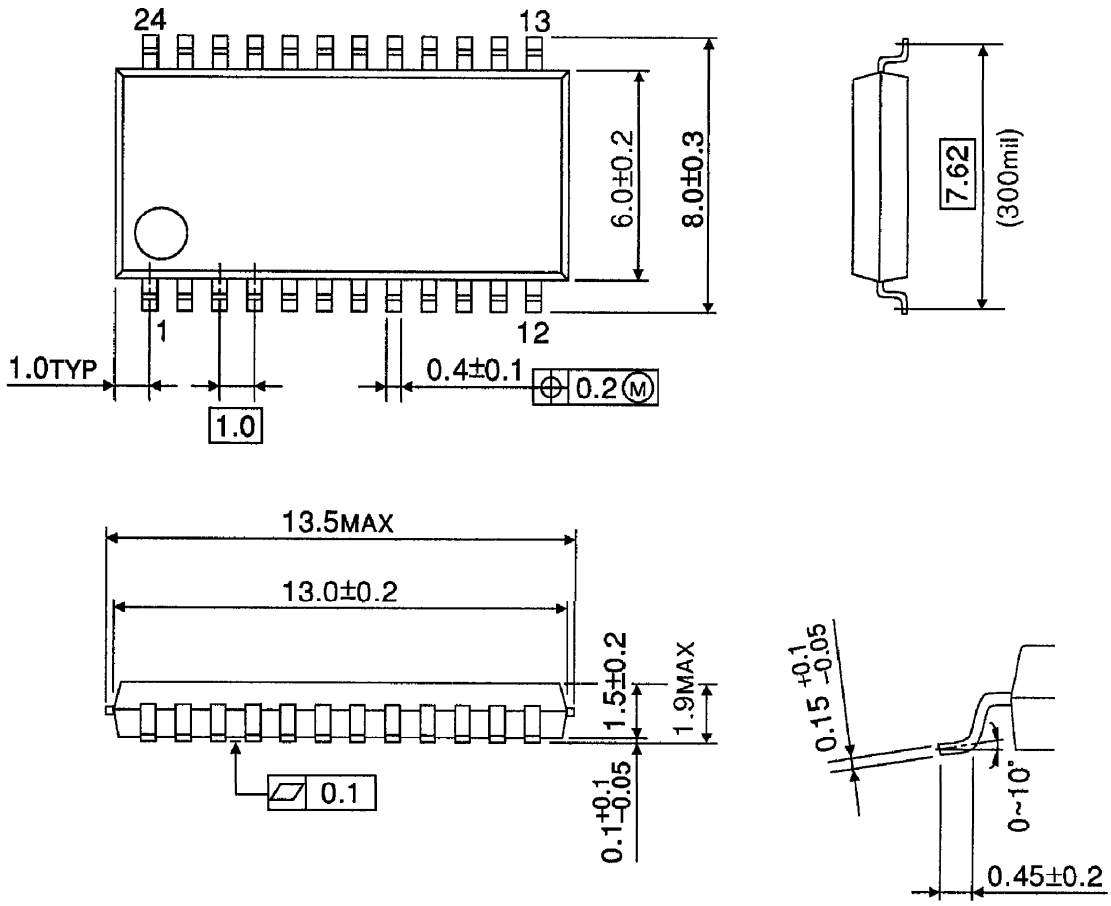


MOISTURE-PROOF PACKING

After the pack is opened, use the devices in a 30°C, 60% RH environment, and within the 48 hours. Embossed-tape packing cannot be baked. Devices so packed must be within their allowable time limits after unpacking, as specified on the packing.
Tape packing quantity: 500 devices / reel (EL) or 2000 devices / reel (EL1)

PACKAGE DIMENSIONS

SSOP24-P-300-1.00B Unit : mm



Weight : 0.29 g (typ.)