UltraLow Supply-Current/Supply-Voltage Supervisory Circuits

FEATURES

- **Precision Supply Voltage Supervision Range: 0.9 V, 1.2 V, 1.5 V, 1.6 V, 2 V, and 3.3 V**
- **High Trip-Point Accuracy: 0.75%**
- **Supply Current of 1.2 µA (typical)**
- **$\overline{\text{RESET}}$ Defined With Input Voltages as Low as 0.4 V**
- **Power-On Reset Generator With a Delay Time of 130 ms**
- **Push/Pull or Open-Drain $\overline{\text{RESET}}$ Outputs**
- **SOT23-6 Package**
- **Package Temperature Range: –40°C to +85°C**

APPLICATIONS

- **Applications Using Low-Power DSPs, Microcontrollers, or Microprocessors**
- **Portable- and Battery-Powered Equipment**
- **Intelligent Instruments**
- **Wireless Communication Systems**
- **Industrial Equipment**
- **Notebook/Desktop Computers**

DESCRIPTION

The TPS310x and TPS311x families of supervisory circuits provide circuit initialization and timing supervision, primarily for DSP and processor-based systems.

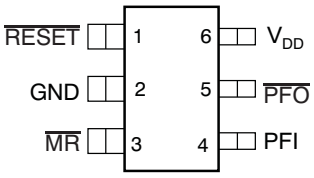
During power-on, $\overline{\text{RESET}}$ is asserted when the supply voltage (V_{DD}) becomes higher than 0.4 V. Thereafter, the supervisory circuit monitors V_{DD} and keeps the $\overline{\text{RESET}}$ output active as long as V_{DD} remains below the threshold voltage (V_{IT}). An internal timer delays the return of the output to the inactive state to ensure proper system reset. The delay time starts after V_{DD} has risen above V_{IT}. When V_{DD} drops below V_{IT}, the output becomes active again.

All the devices of this family have a fixed-sense threshold voltage (V_{IT}) set by an internal voltage divider.

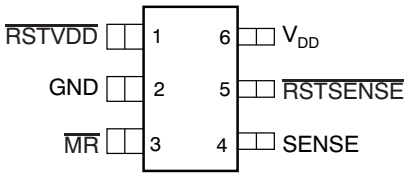
The TPS3103 and TPS3106 have an active-low, open-drain $\overline{\text{RESET}}$ output. The TPS3110 has an active-low push/pull $\overline{\text{RESET}}$.

The product spectrum is designed for supply voltages of 0.9 V up to 3.3 V. The circuits are available in SOT23-6 packages. The TPS31xx family is characterized for operation over a temperature range of –40°C to +85°C.

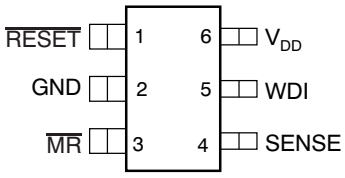
TPS3103
DBV PACKAGE
(TOP VIEW)

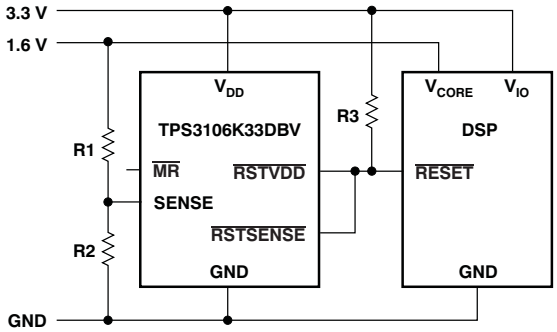


TPS3106
DBV PACKAGE
(TOP VIEW)



TPS3110
DBV PACKAGE
(TOP VIEW)





Typical Application Circuit

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	NOMINAL SUPPLY VOLTAGE	THRESHOLD VOLTAGE, V_{IT}(2)
TPS3103E12DBVR	1.2 V	1.142 V
TPS3103E15DBVR	1.5 V	1.434 V
TPS3103H20DBVR	2.0 V	1.84 V
TPS3103K33DBVR	3.3 V	2.941 V
TPS3106E09DBVR	0.9 V	0.86 V
TPS3106E16DBVR	1.6 V	1.521 V
TPS3106K33DBVR	3.3 V	2.941 V
TPS3110E09DBVR	0.9 V	0.86 V
TPS3110E12DBVR	1.2 V	1.142 V
TPS3110E15DBVR	1.5 V	1.434 V
TPS3110K33DBVR	3.3 V	2.941 V

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Custom threshold voltages are available. Minimum order quantities apply. Contact factory for details and availability.

AVAILABLE OPTIONS

DEVICE	$\overline{\text{RESET}}$ OUTPUT	$\overline{\text{RSTSENSE}}$, $\overline{\text{RSTVDD}}$ OUTPUT	SENSE INPUT	WDI INPUT	$\overline{\text{PFO}}$ OUTPUT
TPS3103	Open-drain				Open-drain
TPS3106		Open-drain	✓		
TPS3110	Push-pull		✓	✓	

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

	VALUE	UNIT
Supply voltage, V_{DD}(2)	–0.3 to +3.6	V
$\overline{\text{MR}}$ Pin, $V_{\overline{MR}}$	–0.3 to V_{DD} + 0.3	V
All other pins(2)	–0.3 to +3.6	V
Maximum low output current, I_{OL}	5	mA
Maximum high output current, I_{OH}	–5	mA
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD})	±10	mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD})(3)	±10	mA
Continuous total power dissipation	See Dissipation Rating Table	
Operating temperature range, T_A	–40 to +85	°C
Storage temperature range, T_{STG}	–65 to +150	°C
Soldering temperature	+260	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND. For reliable operation, the device must not be operated at 3.6 V for more than t = 1000h continuously.
(3) Output is clamped for push-pull outputs by the back gate diodes internal to the IC. No clamp exists for the open-drain outputs.

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DISSIPATION RATINGS

PACKAGE	$T_A \le +25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = +25°C$	$T_A = +70°C$ POWER RATING	$T_A = +85°C$ POWER RATING
DBV	437 mW	3.5 mW/°C	280 mW	227 mW

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range, unless otherwise noted.

	MIN	MAX	UNIT
Supply voltage, V_{DD} (1)	0.4	3.3	V
Input voltage, V_I	0	V_{DD} + 0.3	V
High-level input voltage, V_{IH} at $\overline{MR}$, WDI	$0.7 \times V_{DD}$		V
Low-level input voltage, V_{IL} at $\overline{MR}$, WDI		$0.3 \times V_{DD}$	V
Input transition rise and fall rate at Δt/ΔV at $\overline{MR}$, WDI		100	ns/V
Operating temperature range, T_A	–40	+85	°C

(1) For proper operation of SENSE, PFI, and WDI functions: $V_{DD} \ge 0.8$ V.

ELECTRICAL CHARACTERISTICS

Over operating free-air temperature range (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = 3.3 V, I_{OH} = –3 mA	$0.8 \times V_{DD}$			V
			V_{DD} = 1.8 V, I_{OH} = –2 mA				
			V_{DD} = 1.5 V, I_{OH} = –1 mA				
			V_{DD} = 0.9 V, I_{OH} = –0.4 mA				
			V_{DD} = 0.5 V, I_{OH} = –5 µA	$0.7 \times V_{DD}$			V
V_{OL}	Low-level output voltage		V_{DD} = 3.3 V, I_{OL} = 3 mA			0.3	V
			V_{DD} = 1.5 V, I_{OL} = 2 mA				
			V_{DD} = 1.2 V, I_{OL} = 1 mA				
			V_{DD} = 0.9 V, I_{OL} = 500 µA				
V_{OL}	Low-level output voltage	$\overline{RESET}$ only	V_{DD} = 0.4 V, I_{OL} = 5 µA			0.1	V
$V_{IT–}$	Negative-going input threshold voltage (1)	TPS31xxE09	T_A = +25°C	0.854	0.860	0.866	V
		TPS31xxE12		1.133	1.142	1.151	
		TPS31xxE15		1.423	1.434	1.445	
		TPS31xxE16		1.512	1.523	1.534	
		TPS31xxH20		1.829	1.843	1.857	
		TPS31xxK33		2.919	2.941	2.963	
$V_{IT – (S)}$	Negative-going input threshold voltage (1)	SENSE, PFI	$V_{DD} \ge 0.8$ V, T_A = +25°C	0.542	0.551	0.559	V
V_{HYS}	Hysteresis at V_{DD} input		0.8 V ≤ V_{IT} < 1.5 V		20		mV
			1.6 V ≤ V_{IT} < 2.4 V		30		
			2.5 V ≤ V_{IT} < 3.3 V		50		
$T_{(K)}$	Temperature coefficient of $V_{IT–}$, PFI, SENSE		T_A = –40°C to +85°C		–0.012	–0.019	%/K
V_{HYS}	Hysteresis at SENSE, PFI input		$V_{DD} \ge 0.8$ V		15		mV
I_{IH}	High-level input current	$\overline{MR}$	$\overline{MR}$ = V_{DD}, V_{DD} = 3.3 V	–25		25	nA
		SENSE, PFI, WDI	SENSE, PFI, WDI = V_{DD}, V_{DD} = 3.3 V	–25		25	

(1) To ensure the best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be placed close to the supply terminals.

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ELECTRICAL CHARACTERISTICS (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IL}	Low-level input current	$\overline{MR}$	$\overline{MR}$ = 0 V, V_{DD} = 3.3 V	–47	–33	–25	µA
		SENSE, PFI, WDI	SENSE, PFI, WDI = 0 V, V_{DD} = 3.3 V	–25		25	nA
I_{OH}	High-level output current at $\overline{RESET}$ (2)	Open-drain	$V_{DD} = V_{IT} + 0.2$ V, V_{OH} = 3.3 V			200	nA
I_{DD}	Supply current		$V_{DD} > V_{IT}$ (average current), $V_{DD} < 1.8$ V		1.2	3	µA
			$V_{DD} > V_{IT}$ (average current), $V_{DD} > 1.8$ V		2	4.5	
			$V_{DD} < V_{IT}$, $V_{DD} < 1.8$ V			22	
			$V_{DD} < V_{IT}$, $V_{DD} > 1.8$ V			27	
	Internal pull-up resistor at $\overline{MR}$			70	100	130	kΩ
C_I	Input capacitance at $\overline{MR}$, SENSE, PFI, WDI		V_I = 0 V to V_{DD}		1		pF

(2) Also refers to $\overline{RSTVDD}$ and $\overline{RSTSENSE}$.

SWITCHING CHARACTERISTICS

At R_L = 1 MΩ, C_L = 50 pF, and T_A = –40°C to +85°C, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_D	Delay time		$V_{DD} \geq 1.1 \times V_{IT}$, $\overline{MR} = 0.7 \times V_{DD}$, See Timing Diagrams	65	130	195	ms
t_{PHL}	Propagation delay time, high-to-low level output	V_{DD} to $\overline{RESET}$ or $\overline{RSTVDD}$ delay	$V_{IH} = 1.1 \times V_{IT}$, $V_{IL} = 0.9 \times V_{IT}$			40	µs
t_{PLH}	Propagation delay time, low-to-high level output	V_{DD} to $\overline{RESET}$ or $\overline{RSTVDD}$ delay	$V_{IH} = 1.1 \times V_{IT}$, $V_{IL} = 0.9 \times V_{IT}$			40	µs
t_{PHL}	Propagation delay time, high-to-low level output	SENSE to $\overline{RESET}$ or $\overline{RSTSENSE}$ delay	$V_{DD} \geq 0.8$ V, $V_{IH} = 1.1 \times V_{IT}$, $V_{IL} = 0.9 \times V_{IT}$			40	µs
t_{PLH}	Propagation delay time, high-to-low level output	SENSE to $\overline{RESET}$ or $\overline{RSTSENSE}$ delay	$V_{DD} \geq 0.8$ V, $V_{IH} = 1.1 \times V_{IT}$, $V_{IL} = 0.9 \times V_{IT}$			40	µs
t_{PHL}	Propagation delay time, high-to-low level output	PFI to $\overline{PFO}$ delay	$V_{DD} \geq 0.8$ V, $V_{IH} = 1.1 \times V_{IT}$, $V_{IL} = 0.9 \times V_{IT}$			40	µs
t_{PLH}	Propagation delay time, low-to-high level output	PFI to $\overline{PFO}$ delay	$V_{DD} \geq 0.8$ V, $V_{IH} = 1.1 \times V_{IT}$, $V_{IL} = 0.9 \times V_{IT}$			300	µs
t_{PHL}	Propagation delay time, low-to-high level output	$\overline{MR}$ to $\overline{RESET}$. $\overline{RSTVDD}$, $\overline{RSTSENSE}$ delay	$V_{DD} \geq 1.1 \times V_{IT}$, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$		1	5	µs
t_{PLH}	Propagation delay time, low-to-high level output	$\overline{MR}$ to $\overline{RESET}$. $\overline{RSTVDD}$, $\overline{RSTSENSE}$ delay	$V_{DD} \geq 1.1 \times V_{IT}$, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$		1	5	µs

TIMING REQUIREMENTS

At R_L = 1 MΩ, C_L = 50 pF, and T_A = –40°C to +85°C, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{T(OUT)}$	Time-out period	at WDI	$V_{DD} \geq 0.85$ V	0.55	1.1	1.65	s
t_W	Pulse width	at V_{DD}	$V_{IH} = 1.1 \times V_{IT}$, $V_{IL} = 0.9 \times V_{IT–}$, $V_{IT–} = 0.86$ V	20			µs
		at $\overline{MR}$	$V_{DD} \geq V_{IT} + 0.2$ V, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$	0.1			
		at SENSE	$V_{DD} \geq V_{IT}$, $V_{IH} = 1.1 \times V_{IT\,–\,(S)}$, $V_{IL} = 0.9 \times V_{IT\,–\,(S)}$	20			
		at PFI	$V_{DD} \geq 0.85$ V, $V_{IH} = 1.1 \times V_{IT\,–\,(S)}$, $V_{IL} = 0.9 \times V_{IT\,–\,(S)}$	20			
		at WDI	$V_{DD} \geq V_{IT}$, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$	0.3			

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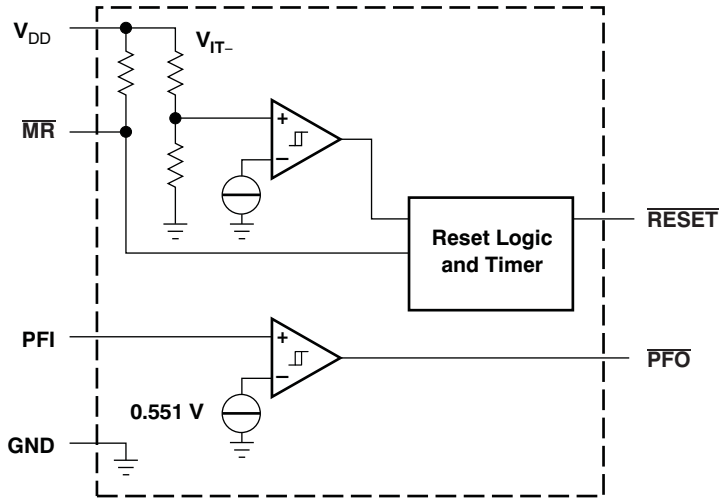
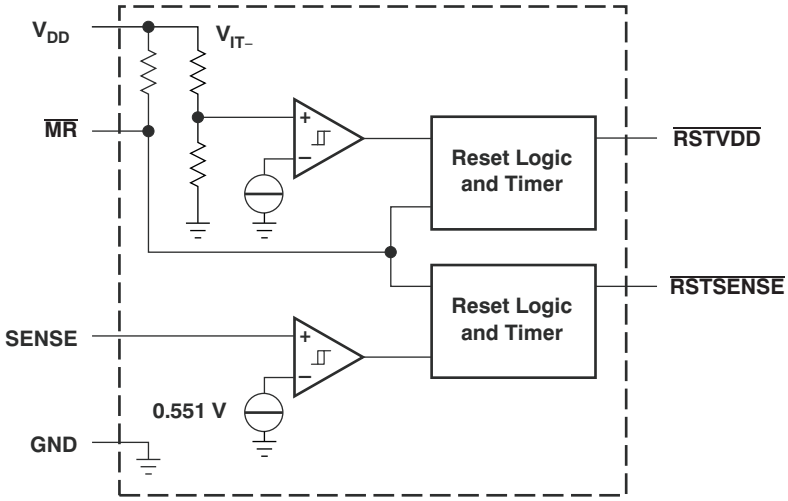
FUNCTIONAL BLOCK DIAGRAMS

TPS3103



TPS3106



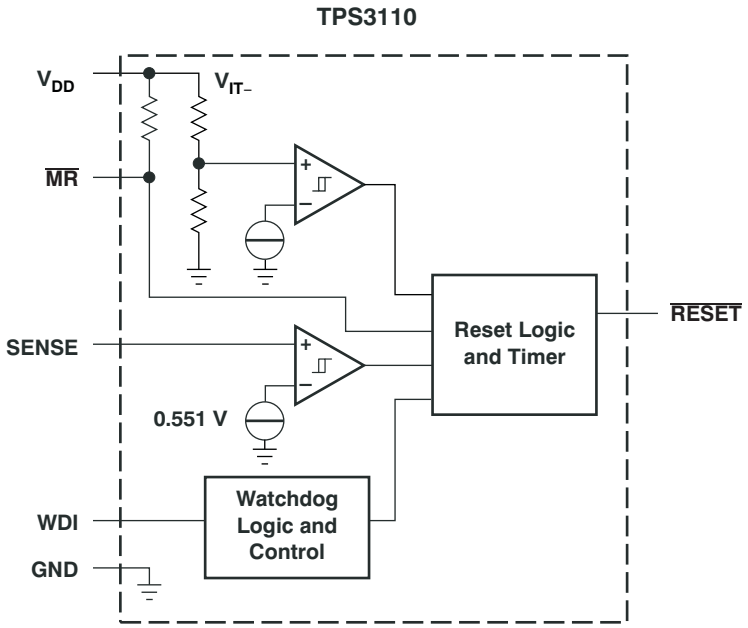


Table 1. TPS3103 FUNCTION TABLE

$\overline{MR}$	$V_{(PFI)}$ > 0.551 V	$V_{DD} > V_{IT}$	$\overline{RESET}$	$\overline{PFO}$
L	0	X(1)	L	L
L	1	X	L	H
H	0	0	L	L
H	0	1	H	L
H	1	0	L	H
H	1	1	H	H

(1) X = Don't care.

Table 2. TPS3106 FUNCTION TABLE

$\overline{MR}$	$V_{(SENSE)}$ > 0.551 V	$V_{DD} > V_{IT}$	$\overline{RSTVDD}$	$\overline{RSTSENSE}$
L	X(1)	X	L	L
H	0	0	L	L
H	0	1	H	L
H	1	0	L	H
H	1	1	H	H

(1) X = Don't care.

Table 3. TPS3110 FUNCTION TABLE(1)

$\overline{MR}$	$V_{(SENSE)}$ > 0.551 V	$V_{DD} > V_{IT}$	$\overline{RESET}$
L	X(2)	X	L
H	0	0	L
H	0	1	L
H	1	0	L
H	1	1	H

(1) Function of watchdog-timer not shown.
(2) X = Don't care.

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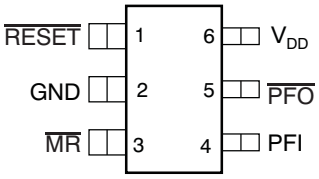
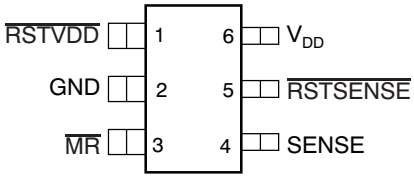
PIN DESCRIPTIONS

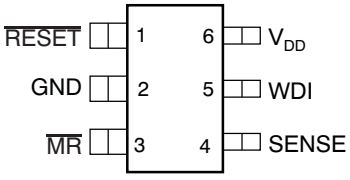
TPS3103
DBV PACKAGE
(TOP VIEW)



TPS3106
DBV PACKAGE
(TOP VIEW)



TPS3110
DBV PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
NAME	DEVICE	NO.	
GND	ALL	2	GND
$\overline{MR}$	ALL	3	Manual-reset input. Pull low to force a reset. $\overline{RESET}$ remains low as long as $\overline{MR}$ is low and for the timeout period after $\overline{MR}$ goes high. Leave unconnected or connect to V_{DD} when unused.
PFI	TPS3103	4	Power-fail input compares to 0.551 V with no additional delay. Connect to V_{DD} if not used.
$\overline{PFO}$	TPS3103	5	Power-fail output. Goes high when voltage at PFI rises above 0.551 V.
$\overline{RESET}$	TPS3103, TPS3110	1	Active-low reset output. Either push-pull or open-drain output stage.
$\overline{RSTSENSE}$	TPS3106	5	Active-low reset output. Logic level at $\overline{RSTSENSE}$ only depends on the voltage at SENSE and the status of $\overline{MR}$.
$\overline{RSTVDD}$	TPS3106	1	Active-low reset output. Logic level at $\overline{RSTVDD}$ only depends on the voltage at V_{DD} and the status of $\overline{MR}$.
SENSE	TPS3106, TPS3110	4	A reset will be asserted if the voltage at SENSE is lower than 0.551 V. Connect to V_{DD} if unused.
V_{DD}	ALL	6	Supply voltage. Powers the device and monitors its own voltage.
WDI	TPS3110	5	Watchdog timer input. If WDI remains high or low longer than the time-out period, then reset is triggered. The timer clears when reset is asserted or when WDI sees a rising edge or a falling edge.

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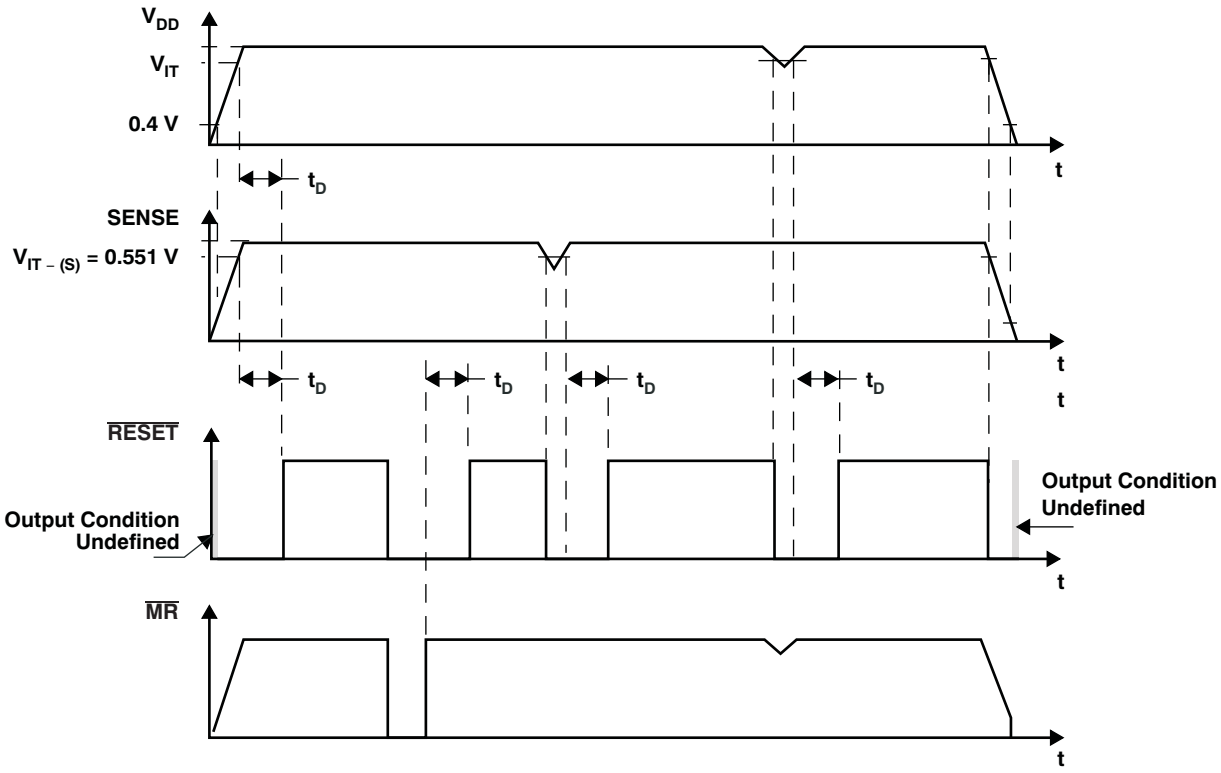
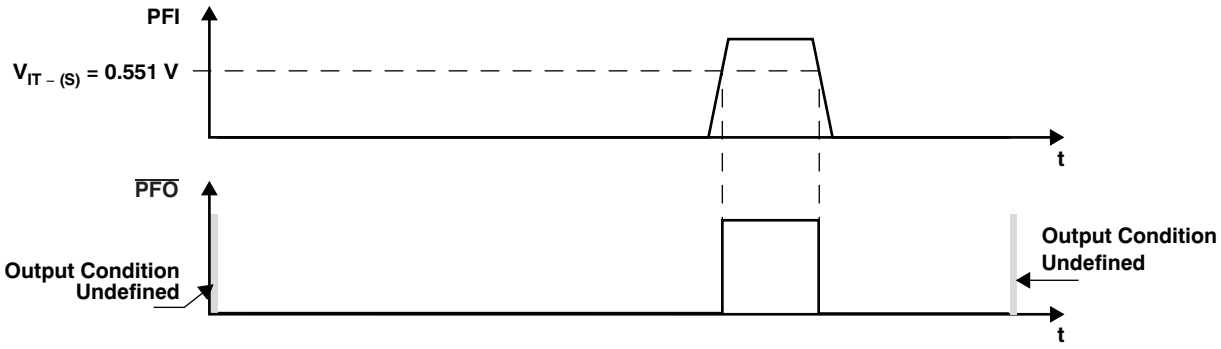
TIMING DIAGRAMS

Timing Diagrams for TPS3103





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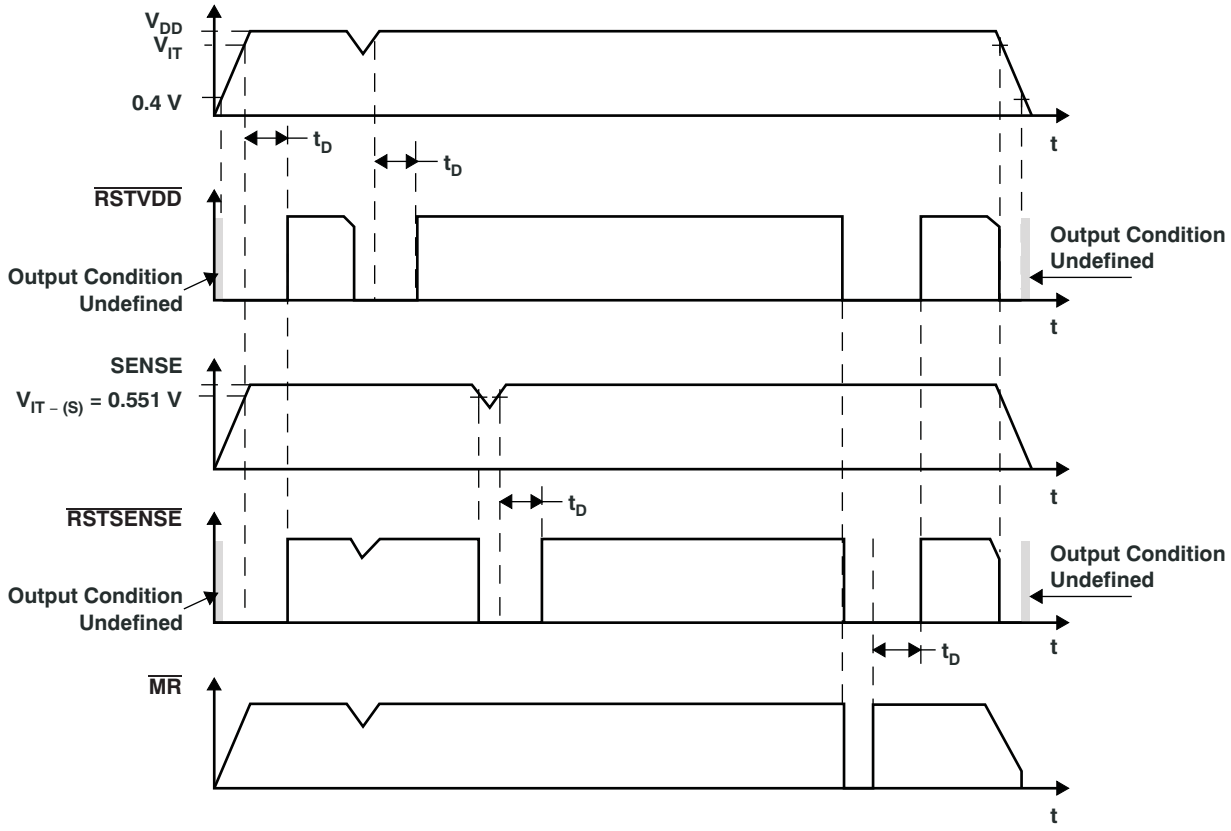
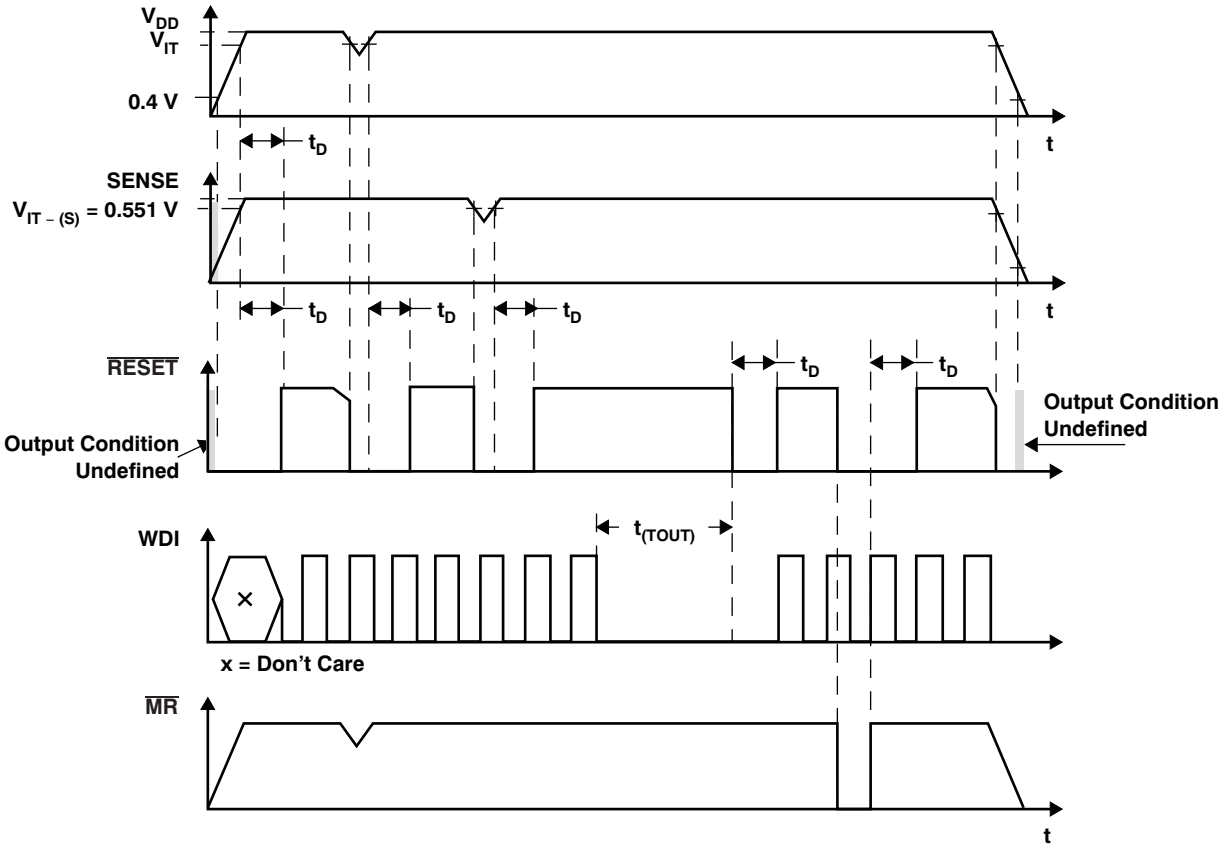
Timing Diagram for TPS3106



Timing Diagram for TPS3110



TYPICAL CHARACTERISTICS

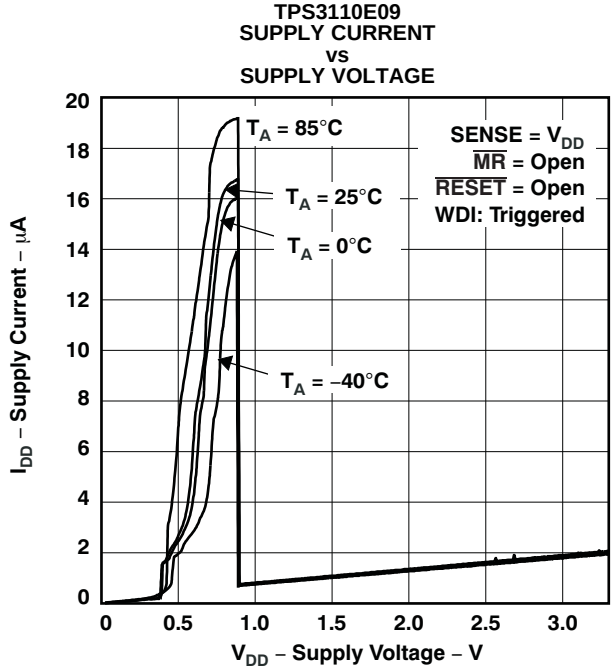


Figure 1.

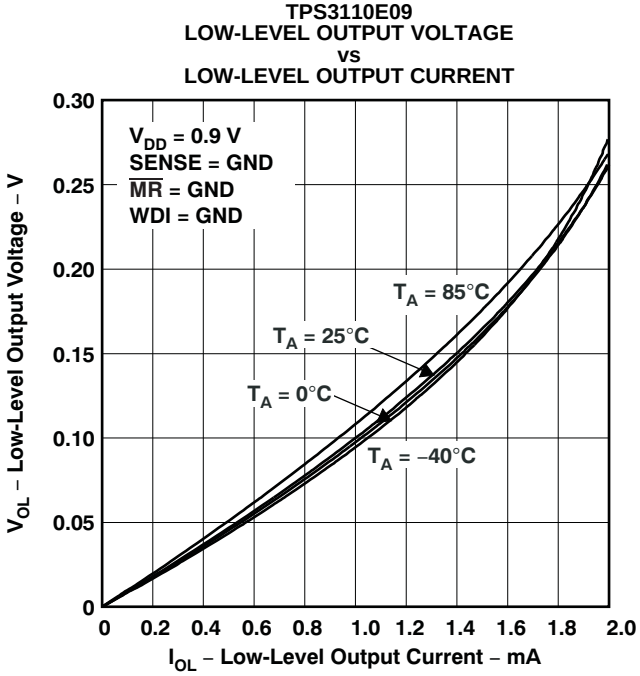


Figure 2.

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TYPICAL CHARACTERISTICS (continued)

TPS3110E09
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

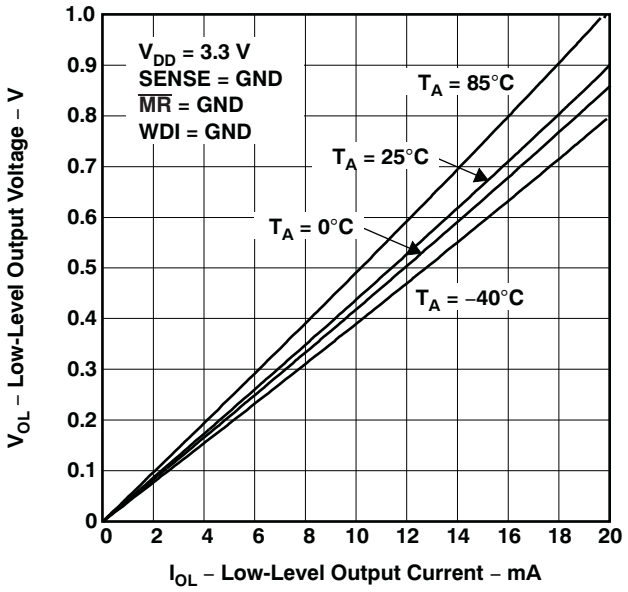

Figure 3.

TPS3110E09
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

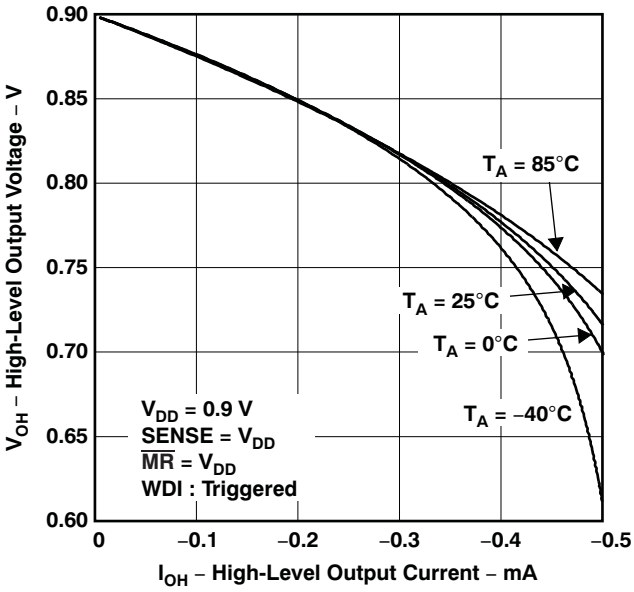

Figure 4.

TPS3110K33
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

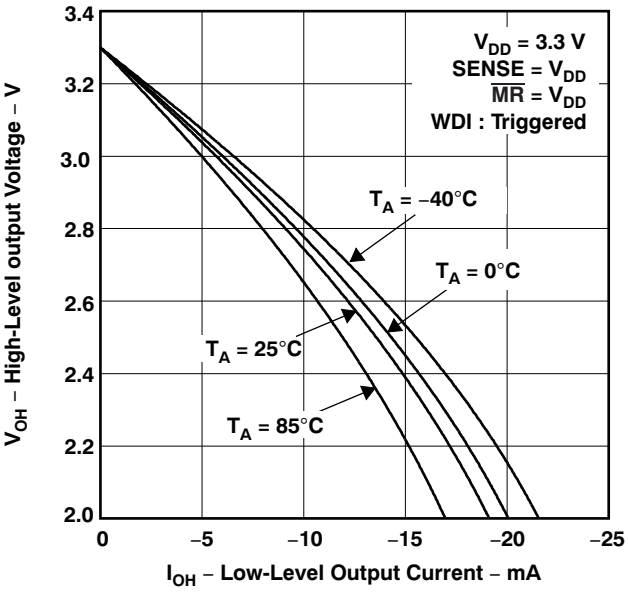

Figure 5.

MINIMUM PULSE DURATION AT V_{DD}
vs
THRESHOLD OVERDRIVE VOLTAGE

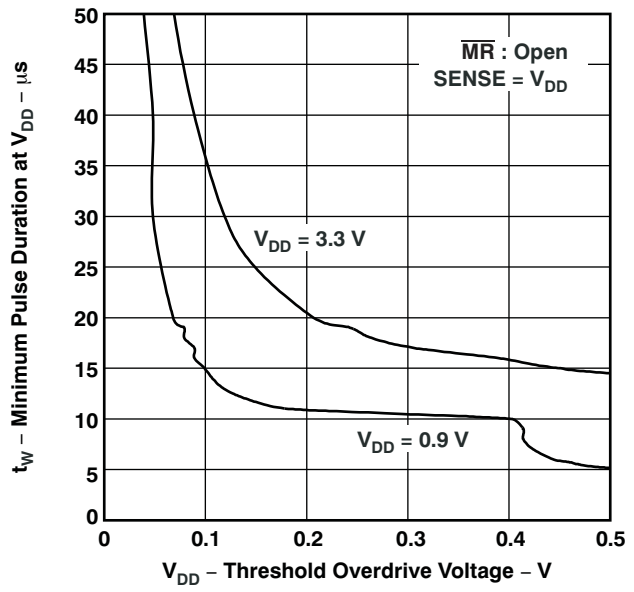

Figure 6.

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TYPICAL CHARACTERISTICS (continued)

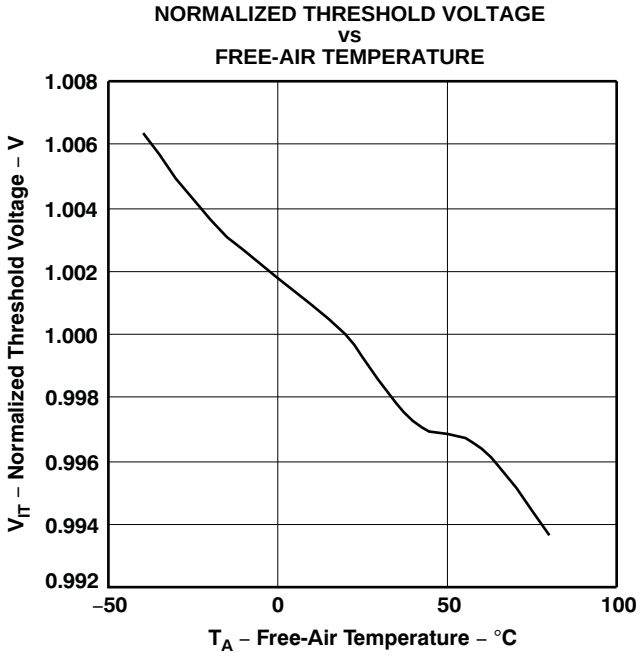

Figure 7.

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APPLICATION INFORMATION

The TPS31xx family has a quiescent current in the 1-µA to 2-µA range. When $\overline{\text{RESET}}$ is active, triggered by the voltage monitored at V_{DD}, the quiescent current increases to about 20 µA (see the Electrical Characteristics).

In some applications it is necessary to minimize the quiescent current even during the reset period. This is especially true when the voltage of a battery is supervised and the $\overline{\text{RESET}}$ is used to shut down the system or for an early warning. In this case the reset condition will last for a longer period of time. The current drawn from the battery should almost be zero, especially when the battery is discharged.

For this kind of application, either the TPS3103 or TPS3106 is a good fit. To minimize current consumption, select a version where the threshold voltage is lower than the voltage monitored at V_{DD}. The TPS3106 has two reset outputs. One output ($\overline{\text{RSTVDD}}$) is triggered from the voltage monitored at V_{DD}. The other output ($\overline{\text{RSTSENSE}}$) is triggered from the voltage monitored at SENSE. In the application shown in Figure 8, the TPS3106E09 is used to monitor the input voltage of two NiCd or NiMH cells. The threshold voltage ($V_{(TH)}$ = 0.86 V) was chosen as low as possible to ensure that the supply voltage is always higher than the threshold voltage at V_{DD}. The voltage of the battery is monitored using the SENSE input. The voltage divider was calculated to assert a reset using the $\overline{\text{RSTSENSE}}$ output at 2 × 0.8 V = 1.6 V.

$$R1 = R2 \times \left(\frac{V_{TRIP}}{V_{IT(S)}} - 1 \right) \quad (1)$$

where:

V_{TRIP} is the voltage of the battery at which a reset is asserted and

$V_{IT(S)}$ is the threshold voltage at SENSE = 0.551 V.

R1 was chosen for a resistor current in the 1-µA range.

With V_{TRIP} = 1.6 V:

R1 ≡ 1.9 × R2

R1 = 820 kΩ, R2 = 430 kΩ

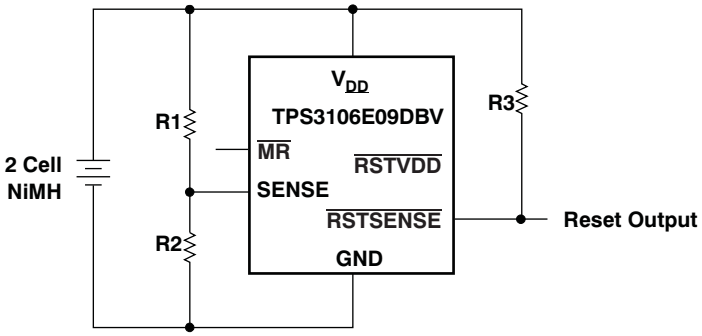

Figure 8. Battery Monitoring with 3-µA Supply Current for Device and Resistor Divider

WATCHDOG

The TPS3110 device integrates a watchdog timer that must be periodically triggered by a positive or negative transition of WDI. When the supervising system fails to retrigger the watchdog circuit within the time-out interval, $\overline{\text{RESET}}$ becomes active for the time period (t_D). This event also reinitializes the watchdog timer.

MANUAL RESET ($\overline{\text{MR}}$)

Many µC-based products require manual-reset capability, allowing an operator or logic circuitry to initiate a reset. Logic low at $\overline{\text{MR}}$ asserts reset. Reset remains asserted while $\overline{\text{MR}}$ is low and for a time period (t_D) after $\overline{\text{MR}}$ returns high. The input has an internal 100-kΩ pull-up resistor, so it can be left open if it is unused.

Connect a normally open momentary switch from $\overline{\text{MR}}$ to GND to create a manual reset function. External debounce is not required. If $\overline{\text{MR}}$ is driven from long cables or if the device is used in noisy environments, connecting a 0.1-µF capacitor from $\overline{\text{MR}}$ to GND provides additional noise immunity.

If there is a possibility of transient or DC conditions causing $\overline{\text{MR}}$ to rise above V_{DD}, a diode should be used to limit $\overline{\text{MR}}$ to a diode drop above V_{DD}.

PFI, $\overline{\text{PFO}}$

The TPS3103 has an integrated power-fail (PFI) comparator with a separate open-drain ($\overline{\text{PFO}}$) output. The PFI and $\overline{\text{PFO}}$ can be used for low-battery detection, power-fail warning, or for monitoring a power supply other than the main supply, and has no effect on $\overline{\text{RESET}}$.

An additional comparator is provided to monitor voltages other than the nominal supply voltage. The power-fail input (PFI) will be compared with an internal voltage reference of 0.551 V. If the input voltage falls below the power-fail threshold ($V_{IT\ -\ (S)}$), the power-fail output ($\overline{\text{PFO}}$) goes low. If it goes above 0.551 V plus approximately 15-mV hysteresis, the output returns to high. By connecting two external resistors, it is possible to supervise any voltage above 0.551 V. The sum of both resistors should be approximately 1 MΩ, to minimize power consumption and to assure that the current into the PFI pin can be neglected, compared with the current through the resistor network. The tolerance of the external resistors should be not more than 1% to ensure minimal variation of sensed voltage. If the power-fail comparator is unused, connect PFI to GND and leave $\overline{\text{PFO}}$ unconnected. For proper operation of the PFI-comparator, the supply voltage (V_{DD}) must be higher than 0.8 V.

SENSE

The voltage at the SENSE input is compared with a reference voltage of 0.551 V. If the voltage at SENSE falls below the sense-threshold ($V_{IT\ -\ (S)}$), reset is asserted. On the TPS3106, a dedicated $\overline{\text{RSTSENSE}}$ output is available. On the TPS3110, the logic signal from SENSE is OR-wired with the logic signal from V_{DD} or $\overline{\text{MR}}$. An internal timer delays the return of the output to the inactive state, once the voltage at SENSE goes above 0.551 V plus about 15 mV of hysteresis. For proper operation of the SENSE-comparator, the supply voltage must be higher than 0.8 V.

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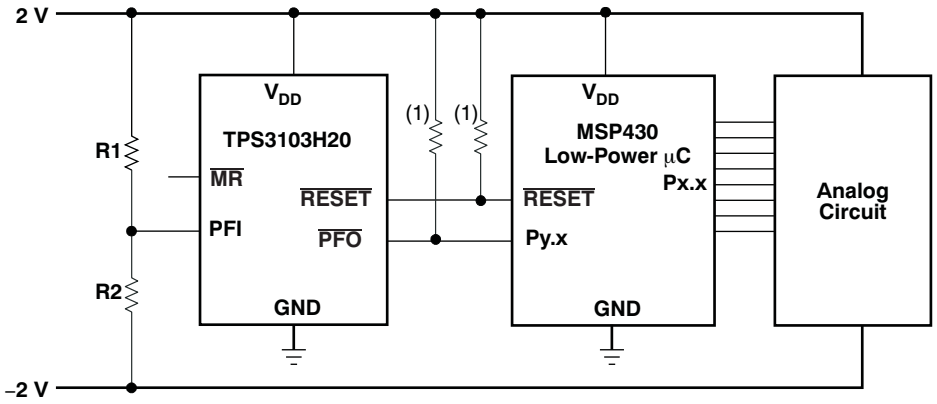
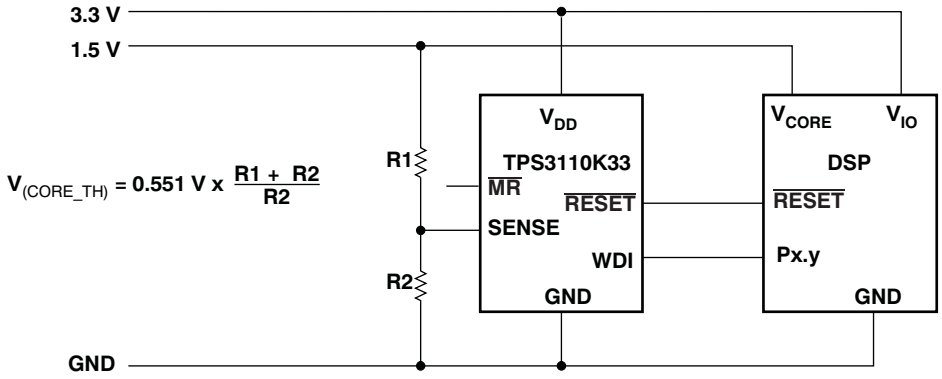


$$V_{(NEG_TH)} = 0.551\ V - \frac{R2}{R1}(V_{DD} - 0.551\ V)$$

(1) Resistor may be integrated in μC.

Figure 9. TPS3103 Monitoring a Negative Voltage



$$V_{(CORE_TH)} = 0.551\ V \times \frac{R1 + R2}{R2}$$

Figure 10. TPS3110 in a DSP-System Monitoring Both Supply Voltages

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN0402002DBVR	ACTIVE	SOT-23	DBV	6		TBD	Call TI	Call TI	-40 to 85		Samples
TPS3103E12DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFWI	Samples
TPS3103E12DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFWI	Samples
TPS3103E12DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFWI	Samples
TPS3103E12DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFWI	Samples
TPS3103E15DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFXI	Samples
TPS3103E15DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFXI	Samples
TPS3103E15DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFXI	Samples
TPS3103E15DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFXI	Samples
TPS3103H20DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFYI	Samples
TPS3103H20DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFYI	Samples
TPS3103H20DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFYI	Samples
TPS3103H20DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFYI	Samples
TPS3103K33DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGRI	Samples
TPS3103K33DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGRI	Samples
TPS3103K33DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGRI	Samples
TPS3103K33DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGRI	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS3106E09DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFZI	Samples
TPS3106E09DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFZI	Samples
TPS3106E09DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFZI	Samples
TPS3106E09DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFZI	Samples
TPS3106E16DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGSI	Samples
TPS3106E16DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGSI	Samples
TPS3106E16DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGSI	Samples
TPS3106E16DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGSI	Samples
TPS3106K33DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGBI	Samples
TPS3106K33DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGBI	Samples
TPS3106K33DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGBI	Samples
TPS3106K33DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGBI	Samples
TPS3110E09DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGII	Samples
TPS3110E09DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGII	Samples
TPS3110E09DBVT	OBSOLETE	SOT-23	DBV	6		TBD	Call TI	Call TI	-40 to 85	PGII	
TPS3110E09DBVTG4	OBSOLETE	SOT-23	DBV	6		TBD	Call TI	Call TI	-40 to 85	PGII	
TPS3110E12DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGJI	Samples
TPS3110E12DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGJI	Samples
TPS3110E12DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGJI	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS3110E12DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGJI	Samples
TPS3110E15DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGKI	Samples
TPS3110E15DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGKI	Samples
TPS3110E15DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGKI	Samples
TPS3110E15DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGKI	Samples
TPS3110K33DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGLI	Samples
TPS3110K33DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGLI	Samples
TPS3110K33DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGLI	Samples
TPS3110K33DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGLI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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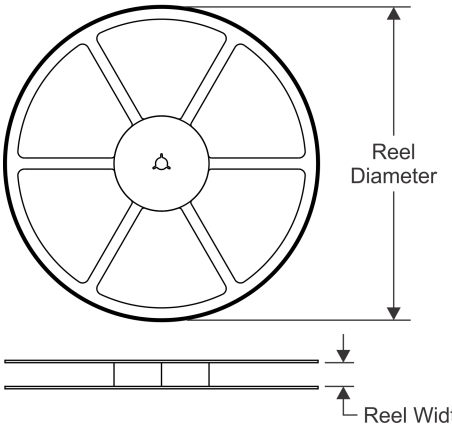
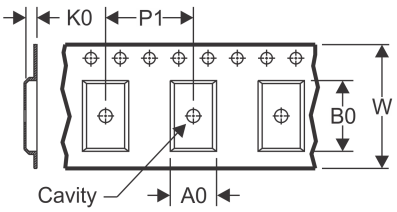
TAPE AND REEL INFORMATION

REEL DIMENSIONS

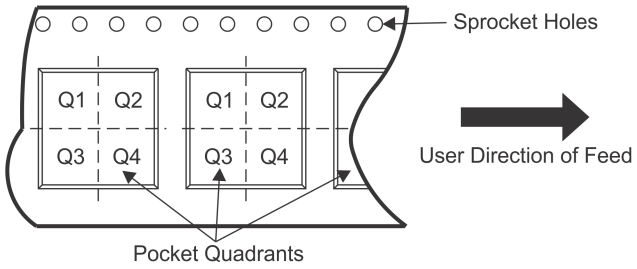


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

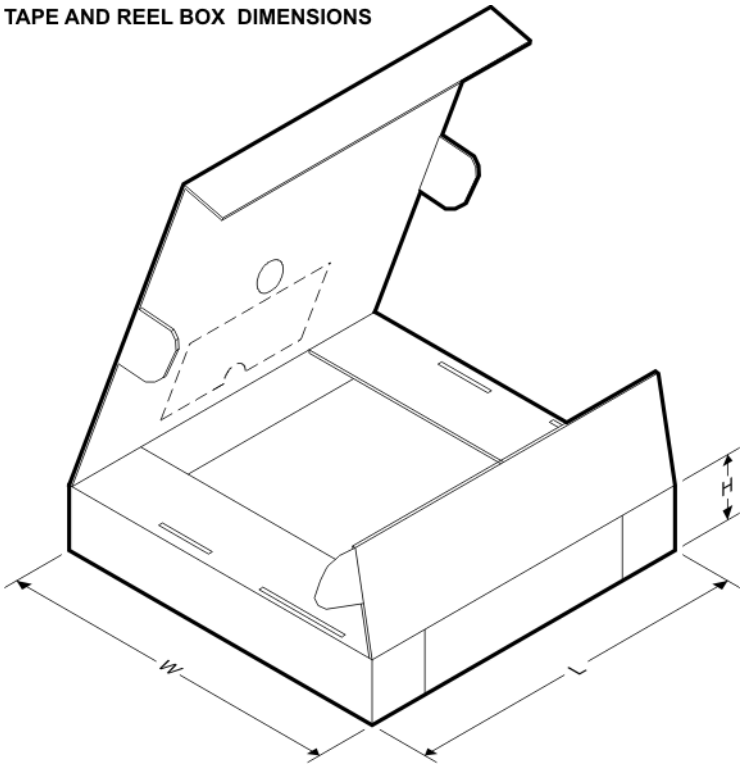


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3103E12DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3103E12DBVT	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3103E15DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3103E15DBVT	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3103H20DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3103H20DBVT	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3103K33DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3103K33DBVR	SOT-23	DBV	6	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3103K33DBVT	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3103K33DBVT	SOT-23	DBV	6	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3106E09DBVR	SOT-23	DBV	6	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3106E09DBVT	SOT-23	DBV	6	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3106E16DBVR	SOT-23	DBV	6	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3106E16DBVT	SOT-23	DBV	6	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3106K33DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3106K33DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3110E09DBVR	SOT-23	DBV	6	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3110E12DBVR	SOT-23	DBV	6	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3110E12DBVT	SOT-23	DBV	6	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3110E15DBVR	SOT-23	DBV	6	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3110E15DBVT	SOT-23	DBV	6	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3110K33DBVR	SOT-23	DBV	6	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3110K33DBVT	SOT-23	DBV	6	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

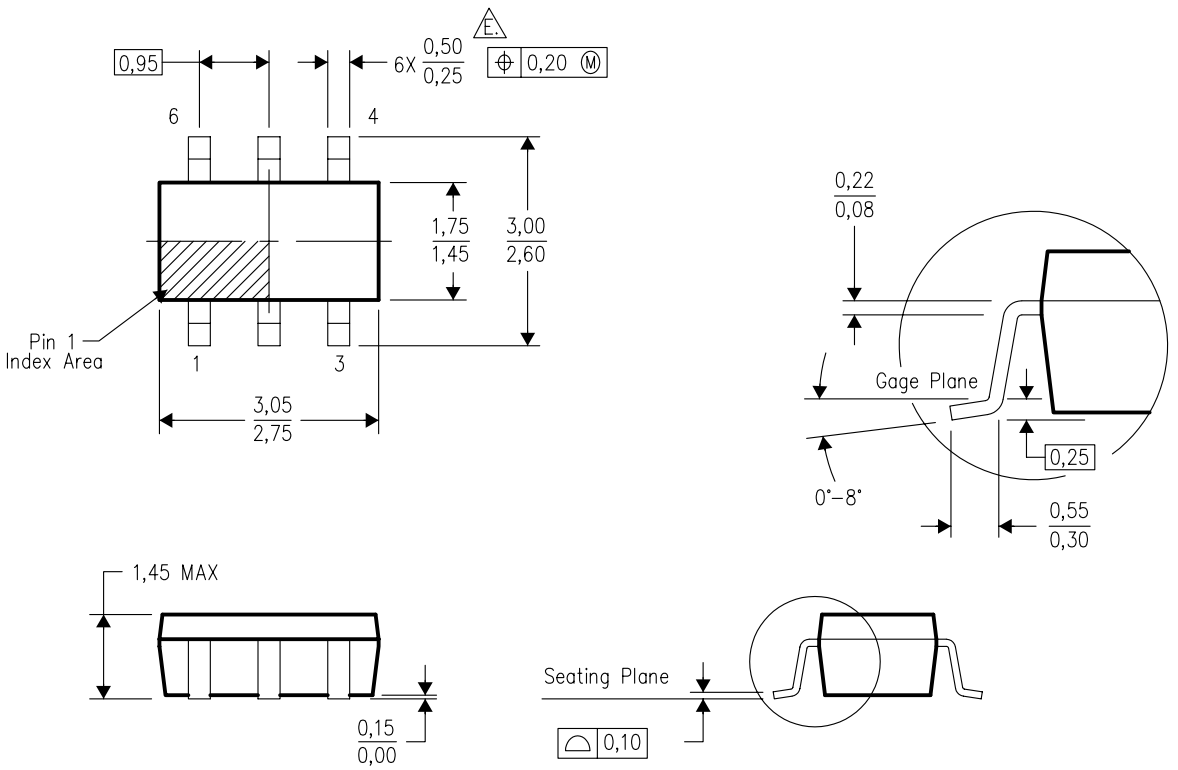


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3103E12DBVR	SOT-23	DBV	6	3000	203.0	203.0	35.0
TPS3103E12DBVT	SOT-23	DBV	6	250	203.0	203.0	35.0
TPS3103E15DBVR	SOT-23	DBV	6	3000	203.0	203.0	35.0
TPS3103E15DBVT	SOT-23	DBV	6	250	203.0	203.0	35.0
TPS3103H20DBVR	SOT-23	DBV	6	3000	203.0	203.0	35.0
TPS3103H20DBVT	SOT-23	DBV	6	250	203.0	203.0	35.0
TPS3103K33DBVR	SOT-23	DBV	6	3000	203.0	203.0	35.0
TPS3103K33DBVR	SOT-23	DBV	6	3000	182.0	182.0	20.0
TPS3103K33DBVT	SOT-23	DBV	6	250	203.0	203.0	35.0
TPS3103K33DBVT	SOT-23	DBV	6	250	182.0	182.0	20.0
TPS3106E09DBVR	SOT-23	DBV	6	3000	182.0	182.0	20.0
TPS3106E09DBVT	SOT-23	DBV	6	250	182.0	182.0	20.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3106E16DBVR	SOT-23	DBV	6	3000	182.0	182.0	20.0
TPS3106E16DBVT	SOT-23	DBV	6	250	182.0	182.0	20.0
TPS3106K33DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3106K33DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
TPS3110E09DBVR	SOT-23	DBV	6	3000	182.0	182.0	20.0
TPS3110E12DBVR	SOT-23	DBV	6	3000	182.0	182.0	20.0
TPS3110E12DBVT	SOT-23	DBV	6	250	182.0	182.0	20.0
TPS3110E15DBVR	SOT-23	DBV	6	3000	182.0	182.0	20.0
TPS3110E15DBVT	SOT-23	DBV	6	250	182.0	182.0	20.0
TPS3110K33DBVR	SOT-23	DBV	6	3000	182.0	182.0	20.0
TPS3110K33DBVT	SOT-23	DBV	6	250	182.0	182.0	20.0

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



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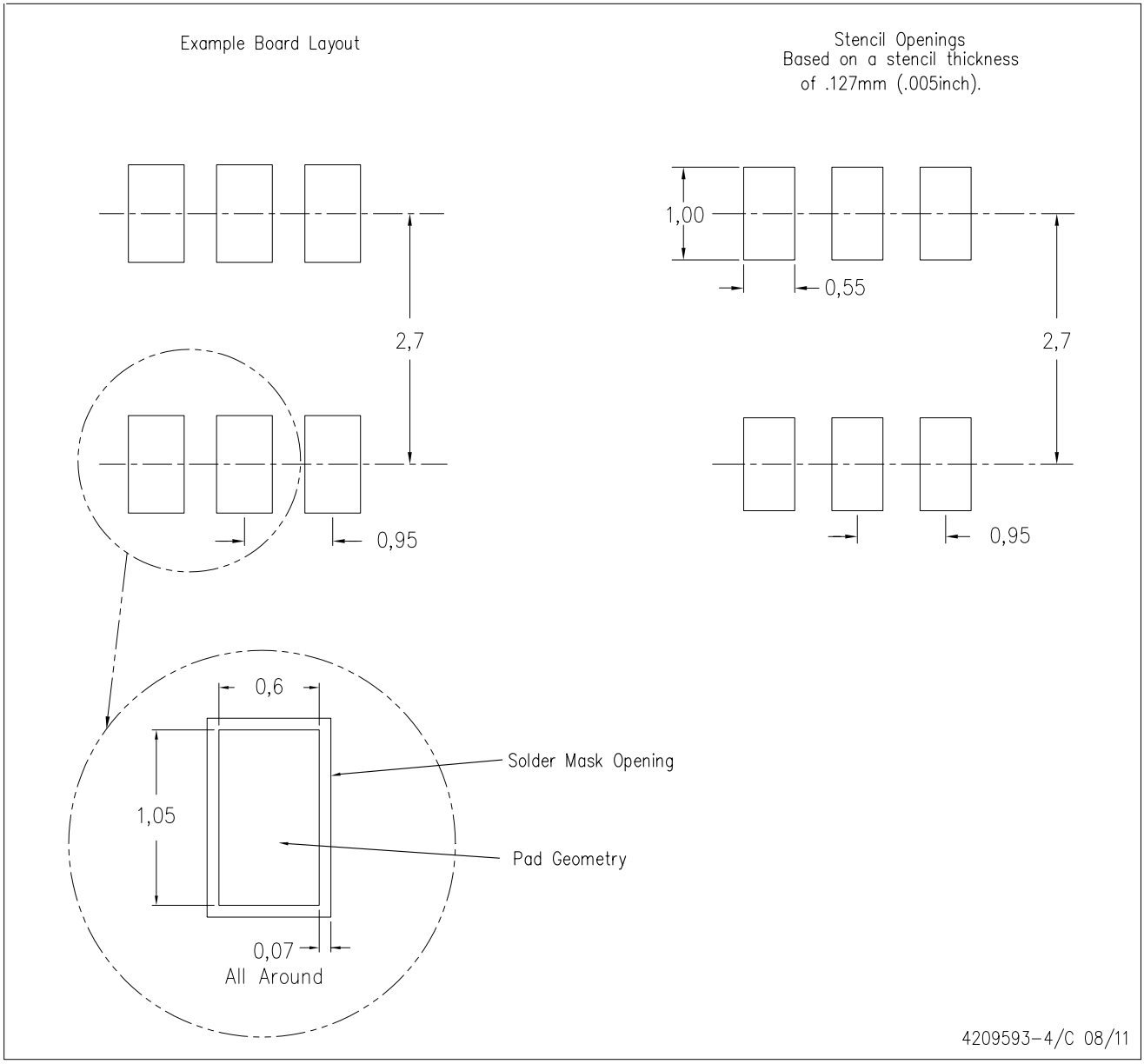
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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