

## Single Synchronous Step-down Controller for Low Voltage Power Rails

Check for Samples: [TPS53014](#)

### FEATURES

- **D-CAP2™ Mode Control**
  - Fast Transient Response
  - No External Parts Required For Loop Compensation
  - Compatible with Ceramic Output Capacitors
- High Initial Reference Accuracy ( $\pm 1\%$ )
- Wide Input Voltage Range: 4.5 V to 28 V
- Output Voltage Range: 0.77 V to 7.0 V
- Low-Side  $R_{DS(on)}$  Loss-Less Current Sensing
- Adjustable Soft Start
- Non-Sinking Pre-Biased Soft Start
- 500 kHz Switching Frequency
- Cycle-By-Cycle Over Current Limiting Control
- Auto-Skip Eco-Mode™ for High Efficiency at Light load

- OCL/OVP/UVP/UVLO/TSD Protections
- Adaptive Gate Drivers with Integrated Boost PMOS Switch
- Thermally Compensated OCP, 4000 ppm/°C
- 10 pin VSSOP

### APPLICATIONS

- Point-of-Load Regulation in Low Power Systems for Wide Range of Applications
  - Digital TV Power Supply
  - Networking Home Terminal
  - Digital Set Top Box (STB)
  - DVD Player / Recorder
  - Gaming Consoles and Other

### DESCRIPTION

The TPS53014 is a single, adaptive on-time D-CAP2™ mode synchronous buck controller. The TPS53014 enables system designers to complete the suite of various end equipment's power bus regulators with cost effective low external component count and low standby current solution. The main control loop for the TPS53014 uses the D-CAP2™ mode control which provides a very fast transient response with no external compensation components. The Adaptive on-time control supports seamless transition between PWM mode at higher load condition and Eco-mode™ operation at light load. Eco-mode™ allows the TPS53014 to maintain high efficiency during lighter load conditions. The TPS53014 is also able to adapt to both low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP and ultra-low ESR ceramic capacitors. The device provides convenient and efficient operation with input voltages from 4.5 V to 28 V and output voltage from 0.77 V to 7.0 V.

The TPS53014 is available in the 3.0mm x 3.0 mm 10-pin VSSOP (DGS) package, and is specified for an ambient temperature range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .



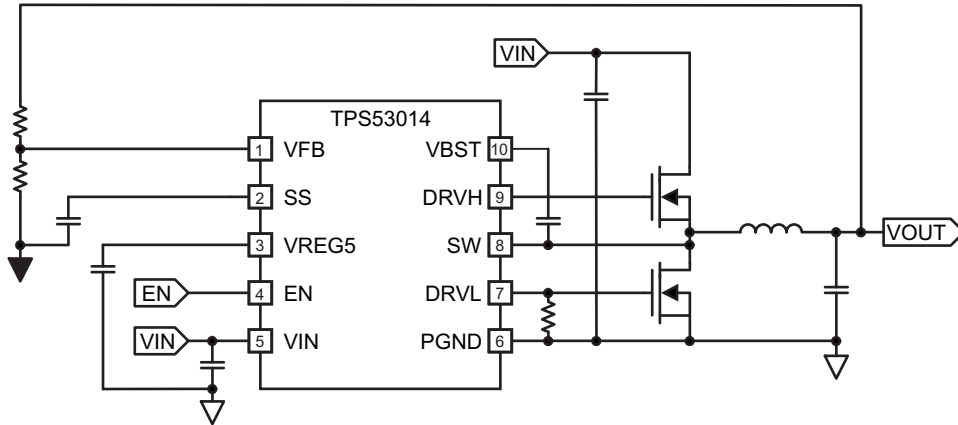
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

D-CAP2, Eco-mode, Eco-Mode are trademarks of Texas Instruments.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**TYPICAL APPLICATION CIRCUITS**



**ORDERING INFORMATION <sup>(1)</sup>**

T <sub>A</sub>	PACKAGE <sup>(1)</sup>	ORDERING PART NUMBER	PINS	OUTPUT SUPPLY	ECO PLAN
-40°C to 85°C	VSSOP	TPS53014DGSR	10	Tape-and-Reel	Green (RoHS & no Sb/Br)
		TPS53014DGS		Tube	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

**ABSOLUTE MAXIMUM RATINGS**

Operating under free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		VALUE	UNIT
Input voltage range	VIN, EN	-0.3 to 30	V
	VBST	-0.3 to 36	
	VBST - SW	-0.3 to 6	
	VFB	-0.3 to 6	
	SW	-0.3 to 30	
	SW (10 nsec transient)	-3.0 to 30	
Output voltage range	DRVH	-2 to 36	V
	DRVH - SW	-0.3 to 6	
	DRVL, VREG5, SS	-0.3 to 6	
	PGND	-0.3 to 0.3	
T <sub>A</sub>	Operating ambient temperature range	-40 to 85	°C
T <sub>STG</sub>	Storage temperature range	-55 to 150	°C
T <sub>J</sub>	Junction temperature range	-40 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		TPS53014	UNITS
		DGS (10 PINS)	
$\theta_{JA}$	Junction-to-ambient thermal resistance	172.2	°C/W
$\theta_{JCTop}$	Junction-to-case (top) thermal resistance	44.0	
$\theta_{JB}$	Junction-to-board thermal resistance	93.0	
$\Psi_{JT}$	Junction-to-top characterization parameter	1.6	
$\Psi_{JB}$	Junction-to-board characterization parameter	91.4	
$\theta_{JCbott}$	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Supply input voltage range	VIN	4.5	28	V
Input voltage range	VBST	-0.1	33.5	V
	VBST - SW	-0.1	5.5	
	VFB	-0.1	5.5	
	EN	-0.1	28	
	SW	-1.0	28	
Output Voltage range	DRVH	-1.0	33.5	V
	DRVH - SW	-0.1	5.5	
	DRVL, VREG5, SS	-0.1	5.5	
	PGND	-0.1	0.1	
T <sub>A</sub>	Operating free-air temperature	-40	85	°C
T <sub>J</sub>	Operating junction temperature	-40	125	°C

## ELECTRICAL CHARACTERISTICS

over recommended free-air temperature range, V<sub>IN</sub> = 12 V (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY CURRENT</b>						
I <sub>IN</sub>	VIN Supply current	VIN current, T <sub>A</sub> = 25°C, EN = 5V, V <sub>VFB</sub> = 0.8V, V <sub>SW</sub> = 0 V		660		μA
I <sub>VINSDN</sub>	VIN Shutdown current	VIN current, T <sub>A</sub> = 25°C, No Load, V <sub>EN</sub> = 0V, VREG5 = OFF		6.0		μA
<b>VFB VOLTAGE and DISCHARGE RESISTANCE</b>						
V <sub>VFBTHL</sub>	VFB Threshold voltage	T <sub>A</sub> = 25°C, V <sub>OUT</sub> = 1.05 V	765.3	773.0	780.7	mV
TC <sub>VFB</sub>	VFB Temperature coefficient	Relative to T <sub>A</sub> = 25°C <sup>(1)</sup>	-140		140	ppm/°C
I <sub>VFB</sub>	VFB Input current	VFB = 0.8V, T <sub>A</sub> = 25°C	-150	-10	100	nA
<b>VREG5 OUTPUT</b>						
V <sub>VREG5</sub>	VREG5 Output voltage	T <sub>A</sub> = 25°C, 6 V < V <sub>IN</sub> < 28 V, I <sub>VREG5</sub> = 5 mA		5.1		V
I <sub>VREG5</sub>	Output current	VIN = 5.5V, V <sub>VREG5</sub> = 4.0V, T <sub>A</sub> = 25°C		120		mA
<b>OUTPUT: N-CHANNEL MOSFET GATE DRIVERS</b>						
R <sub>DRVH</sub>	DRVH resistance	Source, I <sub>DRVH</sub> = -50mA, T <sub>A</sub> = 25°C		3.2	4.7	Ω
		Sink, I <sub>DRVH</sub> = 50mA, T <sub>A</sub> = 25°C		1.4	2.4	
R <sub>DRVL</sub>	DRVL resistance	Source, I <sub>DRVL</sub> = -50mA, T <sub>A</sub> = 25°C		6.9	8.2	Ω
		Sink, I <sub>DRVL</sub> = 50mA, T <sub>A</sub> = 25°C		0.8	1.7	
T <sub>D</sub>	Dead time	DRVH-low to DRVL-on <sup>(1)</sup>		15		ns
		DRVL-low to DRVH-on <sup>(1)</sup>		20		

(1) Ensured by design. Not production tested.

**ELECTRICAL CHARACTERISTICS (continued)**

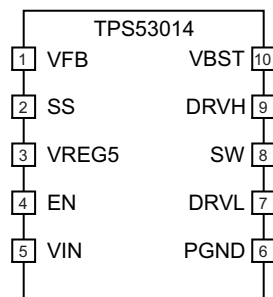
 over recommended free-air temperature range,  $V_{IN} = 12\text{ V}$  (unless otherwise noted)

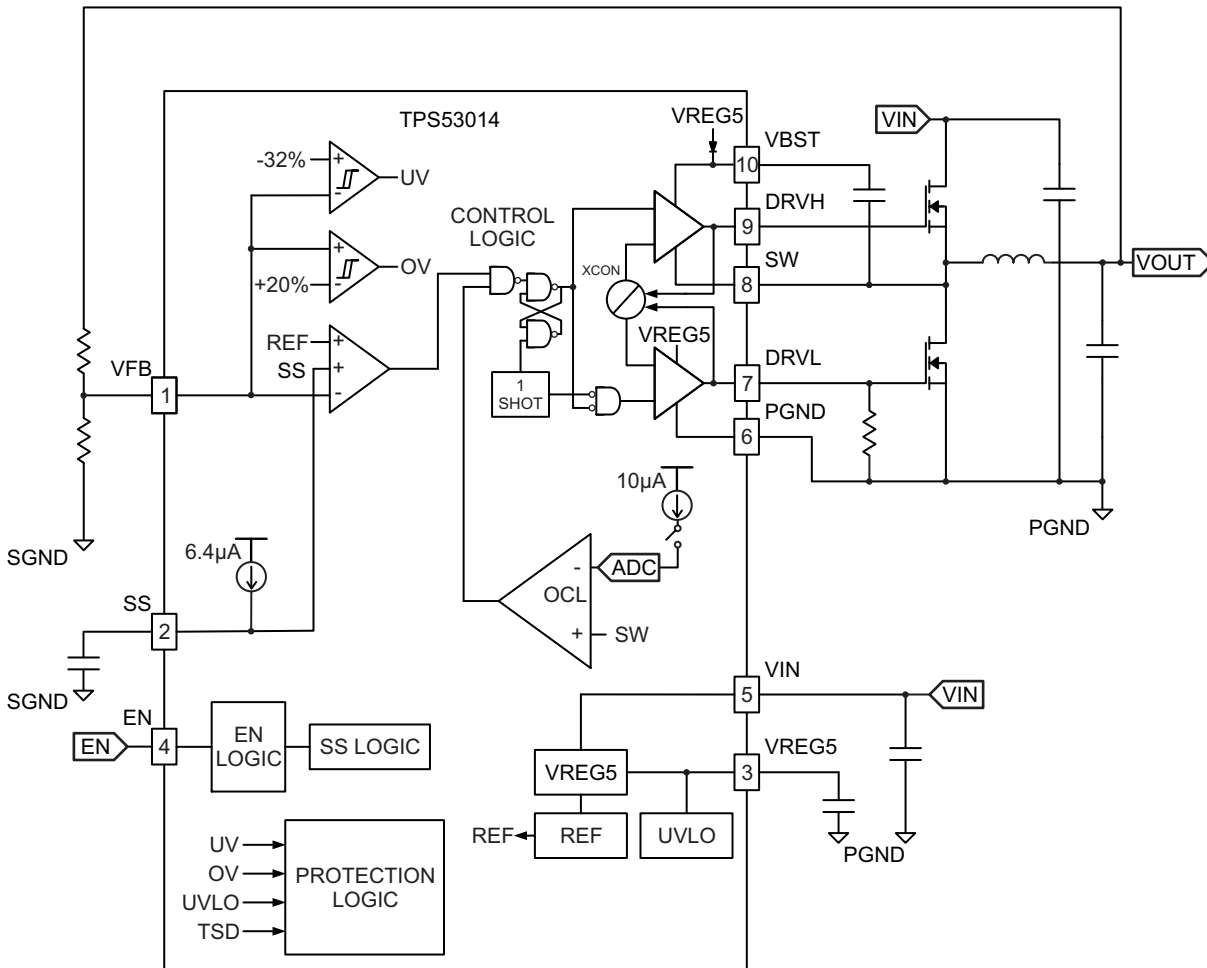
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
<b>INTERNAL BOOST DIODE</b>						
$V_{FBST}$	Forward voltage	$V_{VREG5-VBST}$ , $I_F = 10\text{mA}$ , $T_A = 25^\circ\text{C}$		0.1	0.2	V
<b>SOFT START</b>						
$I_{SSC}$	SS Charge current	$V_{SS} = 0\text{V}$ , $T_A = 25^\circ\text{C}$	-7.36	-6.4	-5.44	$\mu\text{A}$
$I_{SSD}$	SS Discharge current	$V_{SS} = 0.5\text{V}$ , $T_A = 25^\circ\text{C}$	4.5	5.0		mA
$TC_{ISSC}$	$I_{SSC}$ Temperature coefficient	Relative to $T_A = 25^\circ\text{C}$	-4.5		4.5	nA/ $^\circ\text{C}$
<b>UVLO</b>						
$V_{UVVREG5}$	VREG5 UVLO threshold	VREG5 Rising		4.0		V
		Hysteresis		0.3		
<b>LOGIC THRESHOLD</b>						
$V_{ENH}$	EN H-level threshold voltage		1.6			V
$V_{ENL}$	EN L-level threshold voltage				0.5	V
$R_{EN}$	EN pin resistance to GND	$V_{EN} = 12\text{ V}$	225	450	900	k $\Omega$
<b>CURRENT SENSE</b>						
$I_{TRIP}$	TRIP Source current	$V_{DRVL} = 0.1\text{V}$ , $T_A = 25^\circ\text{C}$	14.3	15	15.8	$\mu\text{A}$
$TC_{VTRIP}$	$V_{TRIP}$ Temperature coefficient	Relative to $T_A = 25^\circ\text{C}$		4000		ppm/ $^\circ\text{C}$
$V_{OCL}$	Current limit threshold	$R_{TRIP} = 75\text{k}\Omega$ , $T_A = 25^\circ\text{C}$	234	336	424	mV
		$R_{TRIP} = 27\text{k}\Omega$ , $T_A = 25^\circ\text{C}$	121	174	220	
		$R_{TRIP} = 6.8\text{k}\Omega$ , $T_A = 25^\circ\text{C}$	35	50	63	
<b>ON-TIME TIMER CONTROL</b>						
$T_{ON}$	On time	$V_{OUT} = 1.05\text{ V}^{(2)}$		250		ns
$T_{OFF(MIN)}$	Minimum off time	$V_{IN} = 4.5\text{ V}$ , $V_{VFB} = 0.7\text{ V}$ , $T_A = 25^\circ\text{C}$		230		ns
<b>OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION</b>						
$V_{OVP}$	Output OVP trip threshold	OVP detect voltage	115	120	125	%
$T_{OVPDEL}$	Output OVP propagation delay				10	$\mu\text{s}$
$V_{UVP}$	Output UVP trip threshold	UVP detect voltage	63	68	73	%
$T_{UVPDEL}$	Output UVP delay			1		ms
$T_{UVPEN}$	Output UVP enable delay	UVP enable delay / soft start time	X1.4	X1.7	X2.0	
<b>THERMAL SHUTDOWN</b>						
$T_{SDN}$	Thermal shutdown threshold	Shutdown temperature <sup>(2)</sup>		150		$^\circ\text{C}$
		Hysteresis <sup>(2)</sup>		25		

(2) Ensured by design. Not production tested.

**PIN FUNCTIONS**

PIN		I/O	DESCRIPTION
NAME	VSSOP-10		
VFB	1	I	D-CAP2 feedback input. Connect to output voltage with resistor divider.
SS	2	O	Soft start programming pin. Connect capacitor from SS pin to GND to program soft start time.
VREG5	3	O	Output of 5-V linear regulator and supply for MOSFET driver. Bypass to GND with a minimum 4.7- $\mu$ F high quality ceramic capacitor. VREG5 is active when EN is asserted high.
EN	4	I	Enable. Pull High to enable converter.
VIN	5	I	Supply Input for 5-V linear regulator. Bypass to GND with a minimum 0.1- $\mu$ F high quality ceramic capacitor.
PGND	6	I	System ground.
DRVL	7	O	Low-side N-Channel MOSFET gate driver output. PGND referenced driver switches between PGND(OFF) and VREG5(ON).
SW	8	I/O	Switch node connections for both the high-side driver and over current comparator.
DRVH	9	O	High-side N-channel MOSFET gate driver output. SW referenced driver switches between SW(OFF) and VBST(ON).
VBST	10	I	High-side MOSFET gate driver bootstrap voltage input. Connect a capacitor from VBST to SW. An internal diode is connected between VREG5 and VBST

**10 PIN VSSOP  
(TOP VIEW)**


**FUNCTIONAL BLOCK DIAGRAM**

**OVERVIEW**

The TPS53014 is single synchronous step-down (buck) controller. It operates using D-CAP2™ mode control. The fast transient response of D-CAP2™ control reduces the required amount of output capacitance to meet a specific level of performance. Proprietary internal circuitry allows the use of low ESR output capacitors including ceramic and special polymer types.

**DETAILED DESCRIPTION**
**PWM OPERATION**

The main control loop of the TPS53014 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ control mode. D-CAP2™ control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output. At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off when the internal timer expires. This timer is set by the converter input voltage VIN, and the output voltage VO, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the nominal output voltage. An internal ramp is added to the reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2™ mode control.

## AUTO-SKIP Eco-Mode™ CONTROL

The TPS53014 is designed with Auto-Skip Eco-mode™ to increase light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to point where its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when its zero inductor current is detected. As the load current further decreases the converter run into discontinuous conduction mode. The on-time is kept almost half as it was in the continuous conduction mode because it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. The transition point to the light load operation IOX(LL) current can be calculated in [Equation 1](#) with 500kHz used as fsw.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

## DRIVERS

TPS53014 contains two high-current resistive MOSFET gate drivers. The low-side driver is a PGND referenced, VREG5 powered driver designed to drive the gate of a high-current, low  $R_{DS(on)}$  N-channel MOSFET whose source is connected to PGND. The high-side driver is a floating SW referenced, VBST powered driver designed to drive the gate of a high-current, low  $R_{DS(on)}$  N-channel MOSFET. To maintain the VBST voltage during the high-side driver ON time, a capacitor is placed from SW to VBST. Each driver draws average current equal to Gate Charge ( $Q_g$  @  $V_{gs} = 5V$ ) times Switching frequency (fsw). To prevent cross-conduction, there is a narrow dead-time when both high-side and low-side drivers are OFF between each driver transition. During this time the inductor current is carried by one of the MOSFETs body diodes.

## 5-VOLT REGULATOR

The TPS53014 has an internal 5V Low-Dropout (LDO) Regulator to provide a regulated voltage for all both drivers and the ICs internal logic. A high-quality 4.7μF or greater ceramic capacitor from VREG5 to GND is required to stabilize the internal regulator.

## SOFT START AND PRE-BIASED SOFT START

The soft start function is adjustable. When the EN pin becomes high, 6.4-μA current begins charging the capacitor which is connected from the SS pin to GND. Smooth control of the output voltage is maintained during start up. The equation for the slow start time is shown in [Equation 2](#). VFB voltage is 0.773 V and SS pin source current is 6.4-μA.

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times VFB(V)}{I_{SS}(\mu A)} = \frac{C_{SS}(nF) \times 0.773 V}{6.4\mu A} \quad (2)$$

The TPS53014 contains a unique circuit to prevent current from being pulled from the output during startup if the output is pre-biased. When the soft-start commands a voltage higher than the pre-bias level (internal soft start becomes greater than internal feedback voltage VFB), the controller slowly activates synchronous rectification by starting the first low side FET gate driver pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-biased output, and ensures that the output voltage (VO) starts and ramps up smoothly into regulation from pre-biased startup to normal mode operation.

## OVER CURRENT PROTECTION

TPS53014 has a cycle-by-cycle over current limit feature. The over current limits the inductor valley current by monitoring the voltage drop across the low-side MOSFET  $R_{DS(on)}$  during the low-side driver on-time. If the inductor current is larger than the over current limit (OCL), the TPS53014 delays the start of the next switching cycle until the sensed inductor current falls below the OCL current. MOSFET  $R_{DS(on)}$  current sensing is used to provide an accuracy and cost effective solution without external devices. To program the OCL, a resistor should be connected between DRV1 and PGND. The recommended values are given in [Table 1](#).

**Table 1. OCL Resistor Values**

Resistor Value ( k $\Omega$ )	$V_{trip}$ (V)
6.8	0.050
11	0.087
18	0.125
27	0.174
39	0.224
56	0.274
75	0.336

$I_{OCL}$  is determined by [Equation 3](#).

$$I_{OCL} = \left( \frac{(V_{IN} - V_{OUT})}{2 \times L \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \right) + \frac{V_{TRIP}}{R_{DS(ON)}} \quad (3)$$

The trip voltage is set between 0.05V to 0.336V over all operational temperature, including the 4000ppm/°C temperature slope compensation for the temperature dependency of the  $R_{DS(on)}$ . If the load current exceeds the over-current limit, the voltage will begin to drop. If the over-current conditions continues the output voltage will fall below the under voltage protection threshold and the TPS53014 will shut down.

## OVER/UNDER VOLTAGE PROTECTION

TPS53014 monitors a resistor divided feedback voltage to detect over and under voltage. If the feedback voltage is higher than 120% of the reference voltage, the OVP comparator output goes high and the circuit latches the high-side MOSFET driver OFF and the low-side MOSFET driver ON.

When the feedback voltage is lower than 68% of the reference voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 1ms, TPS53014 latches OFF both top and bottom MOSFET drivers. This function is enabled approximately  $1.7 \times T_{SS}$  after power-on. The OVP and UVP latch off is reset when EN goes low.

## UVLO PROTECTION

TPS53014 has under voltage lock out protection (UVLO) that monitors the voltage of VREG5 pin. When the VREG5 voltage is lower than UVLO threshold voltage, the device is shut off. All output drivers are OFF. The UVLO is non-latch protection.

## THERMAL SHUTDOWN

TPS53014 monitors its temperature. If the temperature exceeds the threshold value (typically 150°C), the device shuts off. When the temperature falls below the threshold, the IC starts again. When VIN starts up and VREG5 output voltage is below its nominal value, the thermal shutdown threshold is kept lower than 150°C. As long as VIN rises,  $T_J$  must be kept less than 110°C.



TYPICAL CHARACTERISTICS

$V_{IN} = 12\text{ V}$ ,  $T_A = 25\text{ }^\circ\text{C}$  (unless otherwise noted)

VIN SUPPLY CURRENT  
vs  
JUNCTION TEMPERATURE

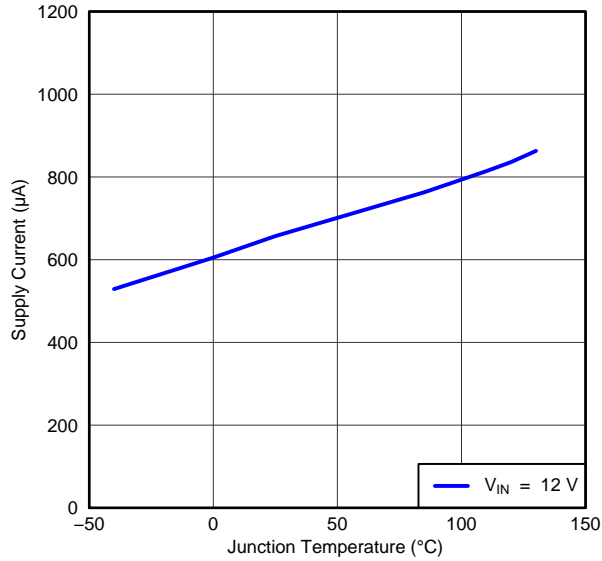


Figure 1.

VIN SHUTDOWN CURRENT  
vs  
JUNCTION TEMPERATURE

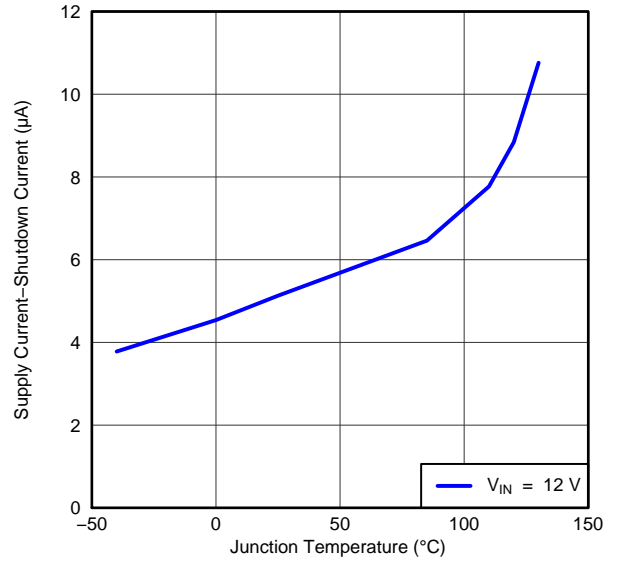


Figure 2.

EN INPUT CURRENT  
vs  
EN INPUT VOLTAGE

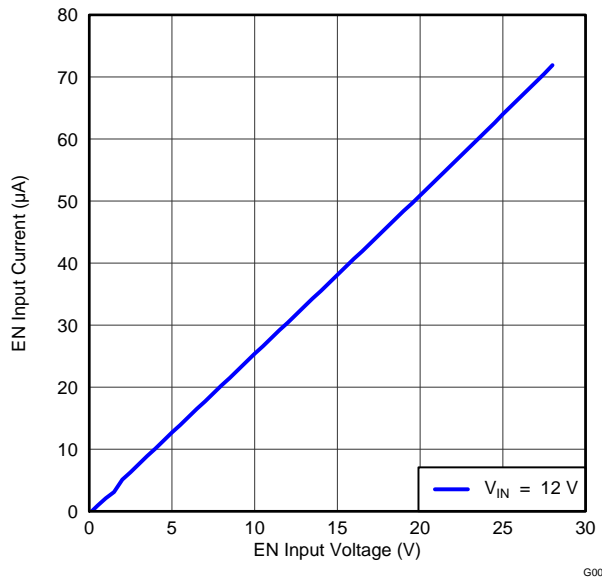


Figure 3.

SWITCHING FREQUENCY  
vs  
JUNCTION TEMPERATURE

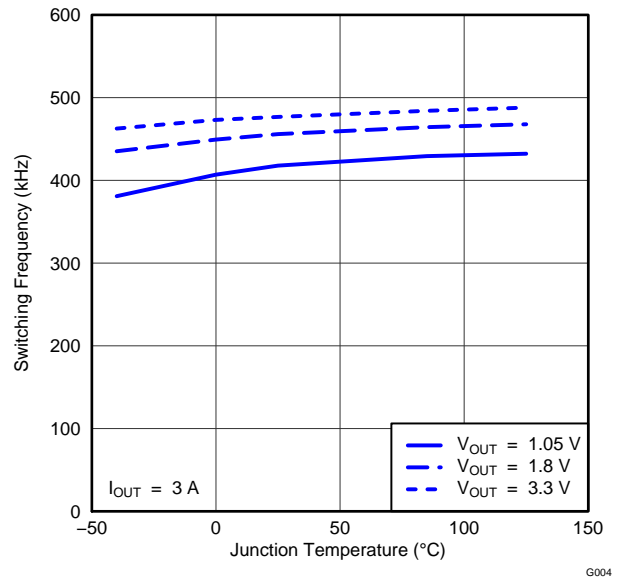


Figure 4.

TYPICAL CHARACTERISTICS (continued)

$V_{IN} = 12\text{ V}$ ,  $T_A = 25\text{ }^\circ\text{C}$  (unless otherwise noted)

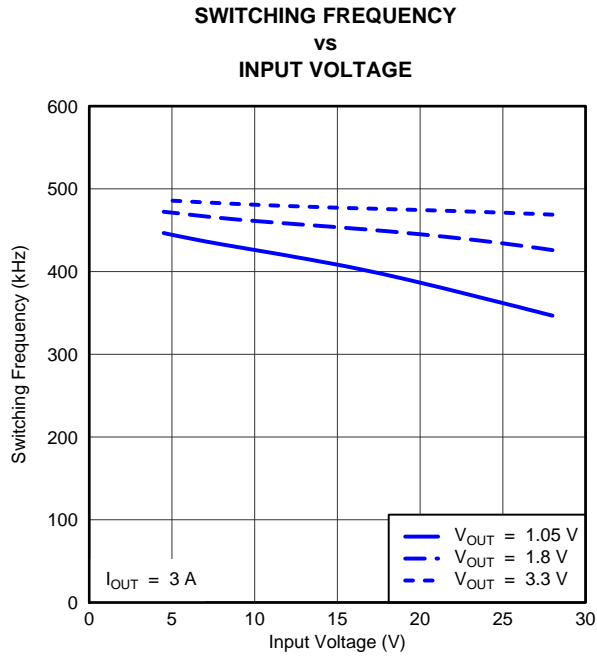


Figure 5.

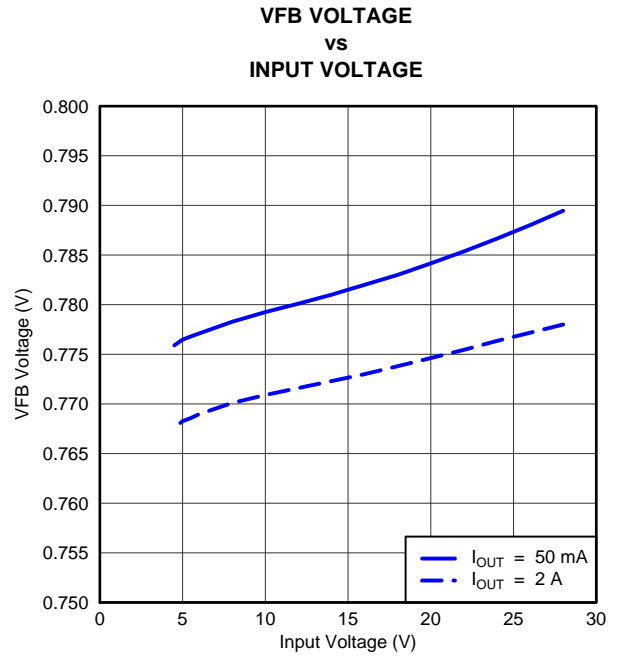


Figure 6.

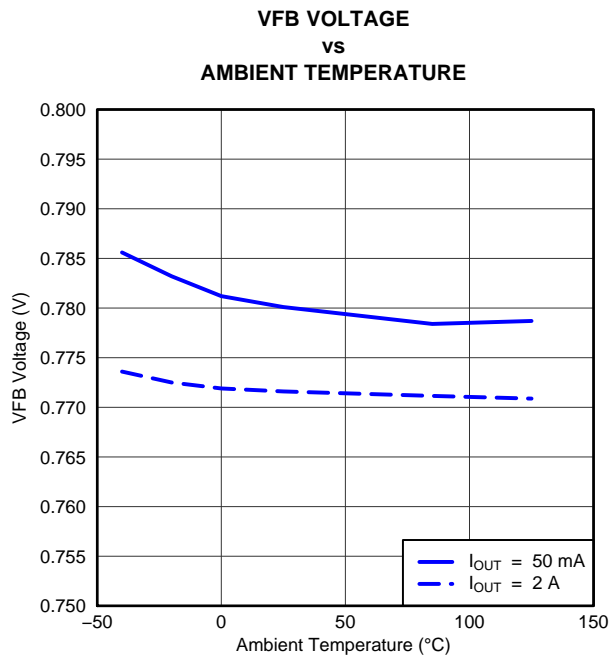


Figure 7.

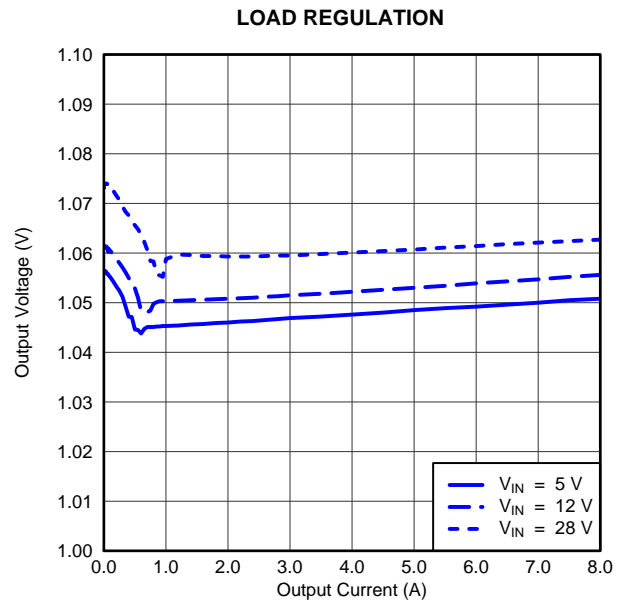


Figure 8.

TYPICAL CHARACTERISTICS (continued)

$V_{IN} = 12\text{ V}$ ,  $T_A = 25\text{ }^\circ\text{C}$  (unless otherwise noted)

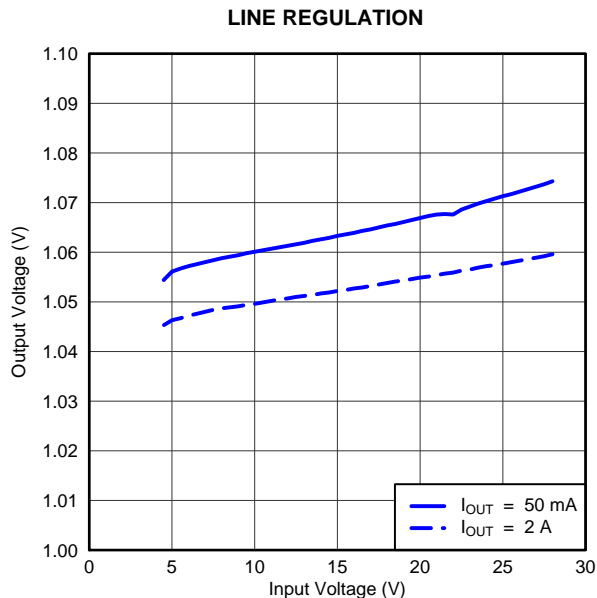


Figure 9.

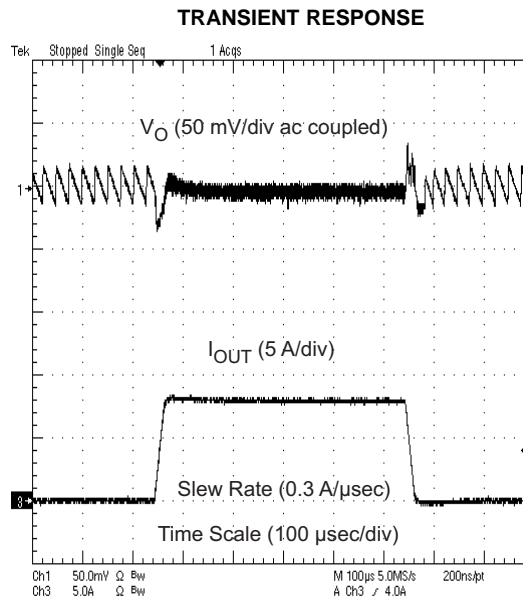


Figure 10.

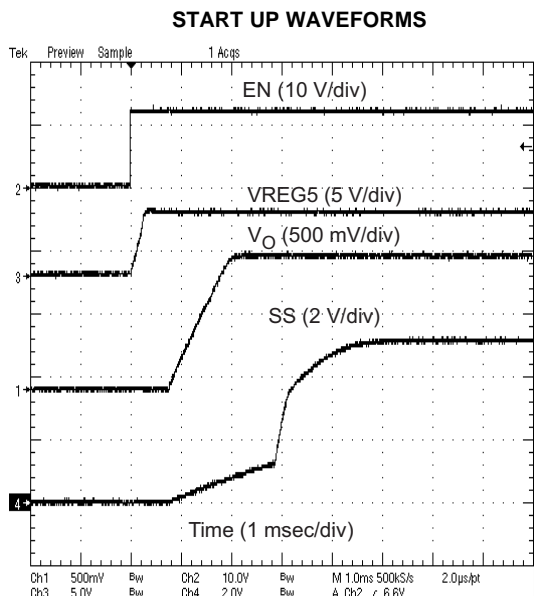


Figure 11.

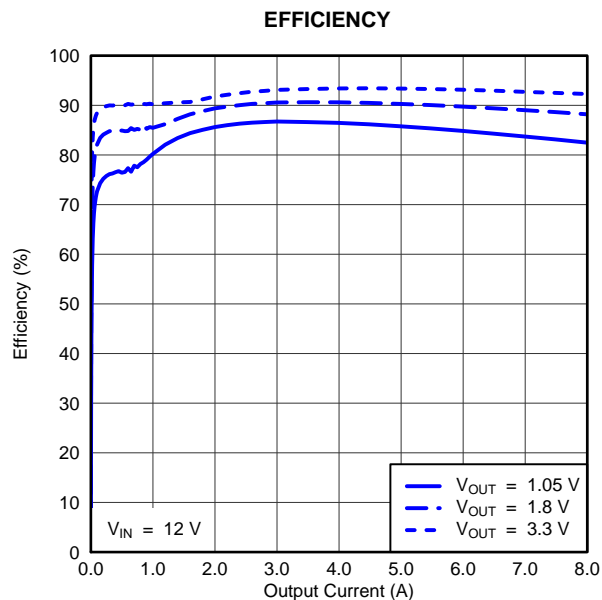


Figure 12.

TYPICAL CHARACTERISTICS (continued)

$V_{IN} = 12\text{ V}$ ,  $T_A = 25\text{ }^\circ\text{C}$  (unless otherwise noted)

LIGHT LOAD EFFICIENCY

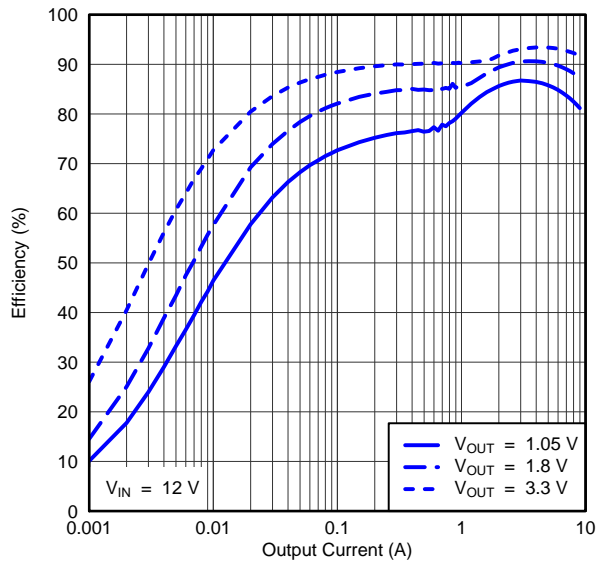


Figure 13.

OUTPUT VOLTAGE RIPPLE,  $I_{OUT} = 8\text{ A}$

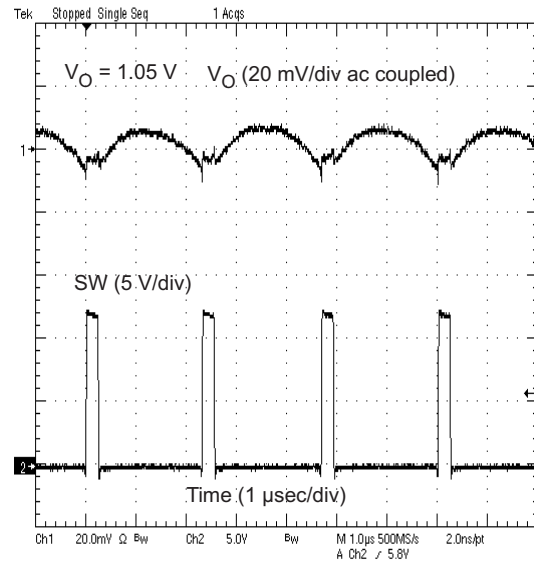


Figure 14.

OUTPUT VOLTAGE RIPPLE,  $I_{OUT} = 50\text{ mA}$

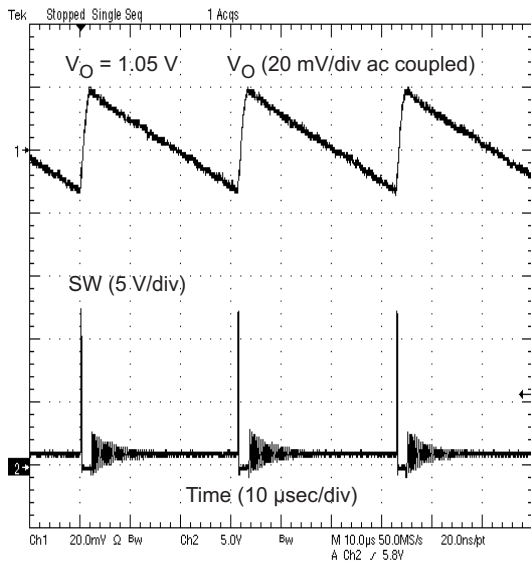


Figure 15.

INPUT VOLTAGE RIPPLE,  $I_{OUT} = 8\text{ A}$

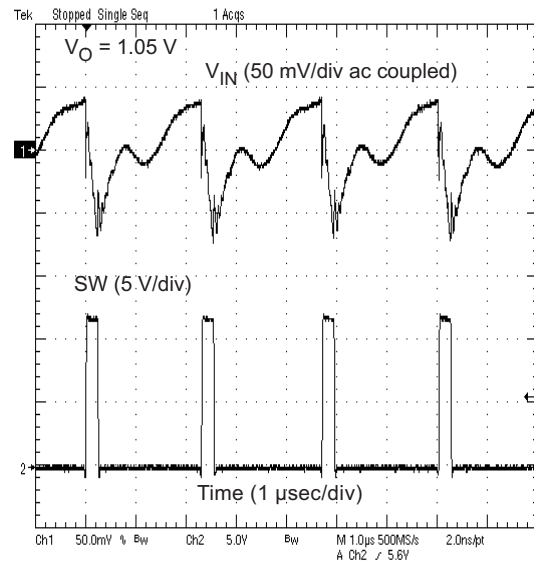
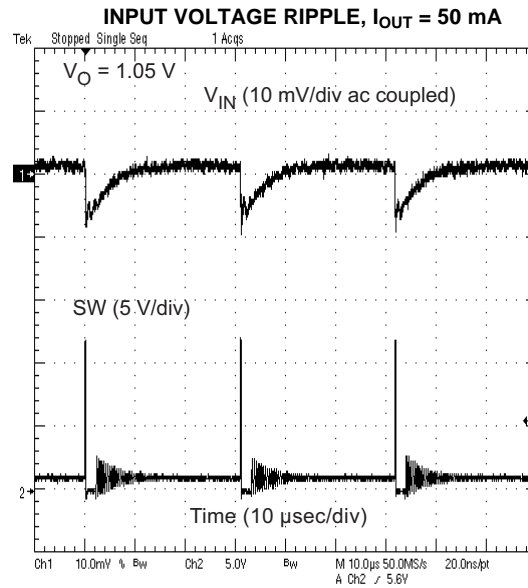


Figure 16.

**TYPICAL CHARACTERISTICS (continued)**

$V_{IN} = 12\text{ V}$ ,  $T_A = 25\text{ }^\circ\text{C}$  (unless otherwise noted)



**Figure 17.**



$$C_{OUT} = \frac{\Delta I_{LOAD}^2}{2 \times V_{OUT} \times \Delta V_{OS}} \times L_{OUT} \quad (9)$$

$$C_{OUT} = \frac{\Delta I_{LOAD}^2}{2 \times K \times \Delta V_{US}} \times L_{OUT} \quad (10)$$

Where:

$$K = (V_{IN} - V_{OUT}) \times \frac{T_{ON}}{T_{ON} - T_{OFF(MIN)}} \quad (11)$$

- $\Delta V_{OS}$  = The allowable amount of overshoot voltage in load transition
- $\Delta V_{US}$  = The allowable amount of undershoot voltage in load transition
- $T_{OFF(MIN)}$  = Minimum off time

Select the capacitance value greater than the largest value calculated from [Equation 8](#), [Equation 9](#) and [Equation 10](#). The minimum recommended output capacitance is 44  $\mu$ F.

### INPUT CAPACITOR

The TPS53014 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A minimum 10- $\mu$ F high-quality ceramic capacitor is recommended for the input capacitor. The capacitor voltage rating needs to be greater than the maximum input voltage.

### BOOTSTRAP CAPACITOR

The TPS53014 requires a bootstrap capacitor from SW to VBST to provide the floating supply for the high-side drivers. A minimum 0.1- $\mu$ F high-quality ceramic capacitor is recommended. The capacitor voltage rating should be greater than 10 V.

### VREG5 CAPACITOR

The TPS53014 requires that the VREG5 regulator is bypassed. A minimum 4.7- $\mu$ F high-quality ceramic capacitor must be connected between the VREG5 and PGND for proper operation. The capacitor voltage rating should be greater than 10 V.

### CHOOSE OUTPUT VOLTAGE RESISTORS

The output voltage is set with a resistor divider from output voltage node to the VFB pin. It is recommended to use 1% tolerance or better resistors. Select R2 between 10 k $\Omega$  and 100 k $\Omega$  and use [Equation 12](#) to calculate R1.

$$R1 = \left( \frac{V_{OUT}}{V_{VFB}} - 1 \right) \times R2 \quad (12)$$

## LAYOUT SUGGESTIONS

- Keep the input switching current loop as small as possible.
- Place the input capacitor close to the top switching FET. The output current loop should also be kept as small as possible.
- Keep the SW node as physically small and short as possible as to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections should be brought from the output to the feedback pin (VFB) of the device.
- Keep analog and non-switching components away from switching components.
- Make a single point connection from the signal ground to power ground.
- Do not allow switching current to flow under the device.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS53014DGS	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
TPS53014DGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53014DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

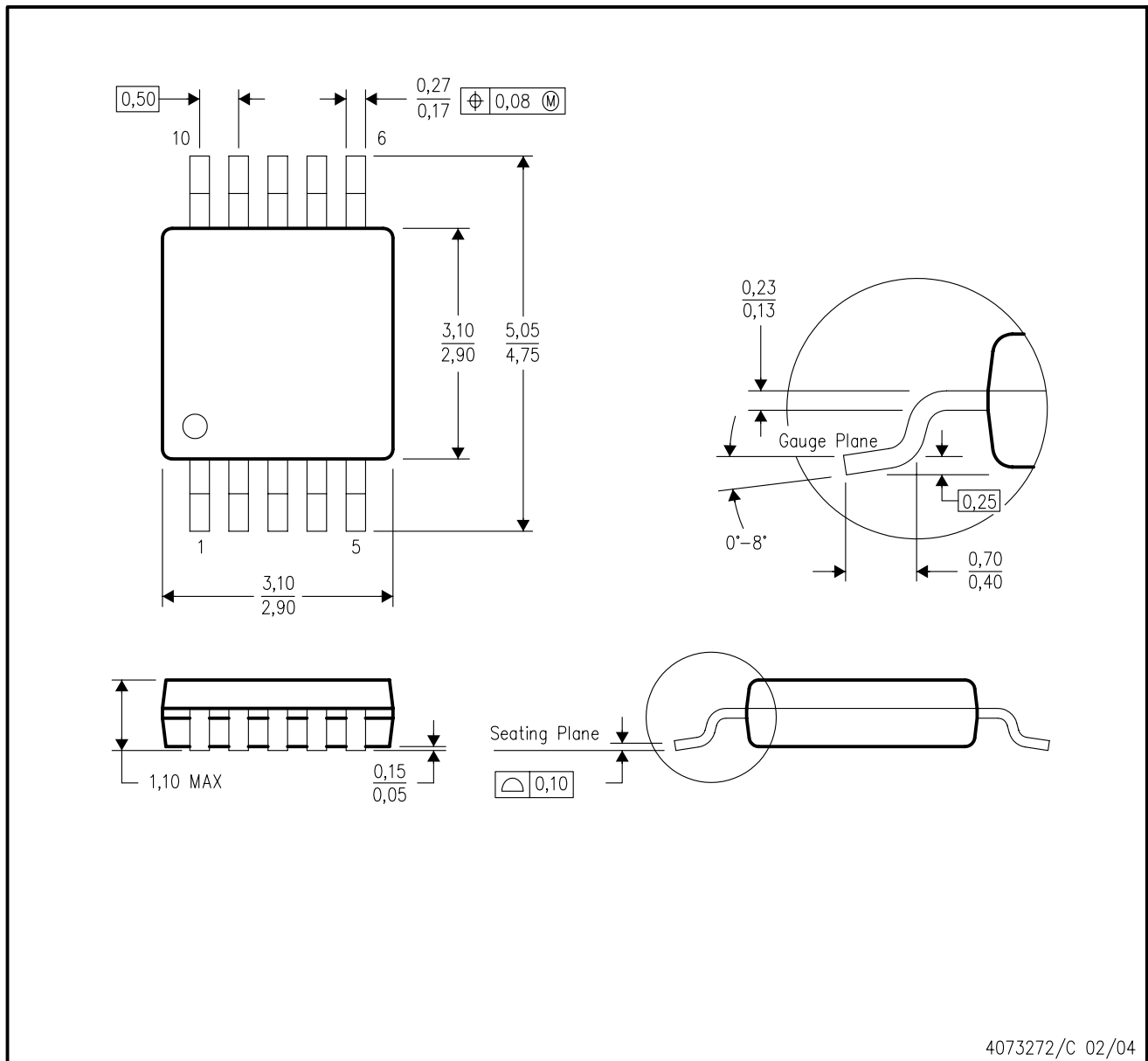


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53014DGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0

DGS (S-PDSO-G10)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion.
  - D. Falls within JEDEC MO-187 variation BA.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Automotive and Transportation	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)