

TPS92640 / TPS92641 Synchronous Buck Controllers for Precision Dimming LED Drivers

Check for Samples: [TPS92640](#), [TPS92641](#)

FEATURES

- V_{IN} range from 7V to 85V
- 2Ω , $1A_{peak}$ MOSFET gate drivers
- Adjustable LED Current Sense voltage
- Input UVLO and output OVP
- Various dimming modes
 - 500:1 Analog Dimming
 - 2500:1 Standard PWM dimming
 - 20000:1 Shunt FET PWM dimming
- Shunt Dimming MOSFET gate driver
- Programmable switching frequency
- Precision Voltage Reference
- Low Power Shutdown Mode and Thermal Shutdown

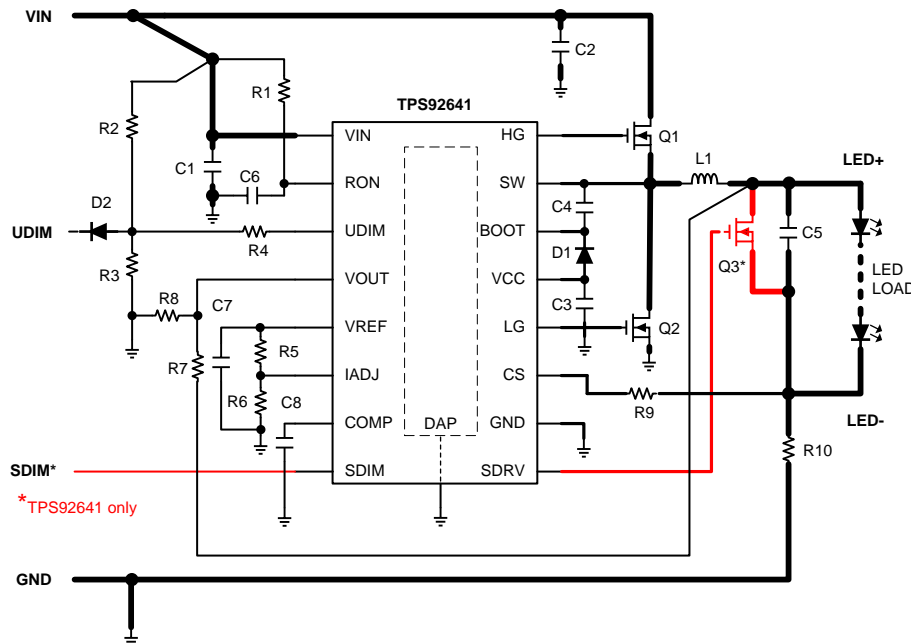
DESCRIPTION

The TPS92640/41 are high voltage, synchronous NFET controllers for buck current regulators. Output current regulation is based on valley current-mode control with a constant on-timer. This control method eases the design of loop compensation. The TPS92640/41 includes a high-voltage start-up regulator that operates over a wide input range of 7V to 85V. The PWM controller is designed for high speed capability including an oscillator frequency range up to 1.0 MHz. The TPS92640/41 is optimized to give superior dimming performance with both analog and PWM dimming. Both devices include an error amplifier, precision reference, thermal shutdown and low power shutdown mode. Additionally, the TPS92641 provides shunt FET dimming capability.

APPLICATIONS

- LED Driver / Constant Current Regulator
- Automotive LED Drivers
- General LED Illumination

TYPICAL APPLICATION DIAGRAM



*TPS92641 only

PRODUCT PREVIEW



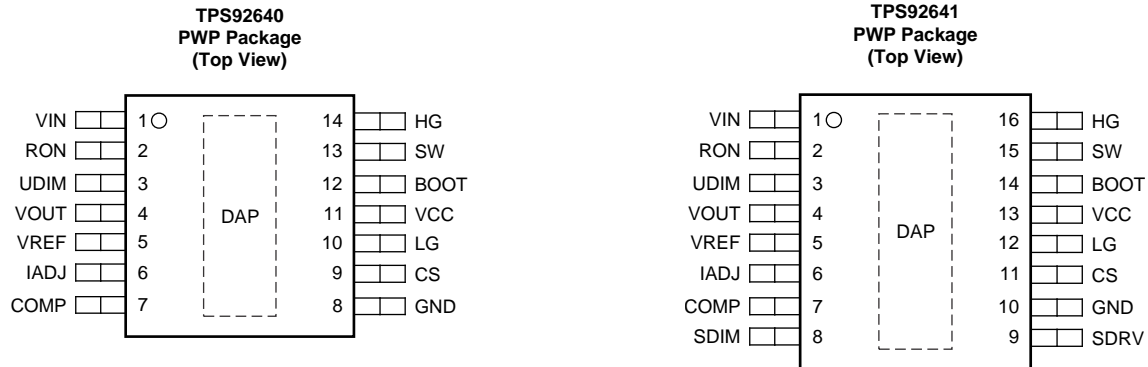
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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PIN CONFIGURATION



PIN FUNCTIONS

TPS92640	TPS92641	NAME	DESCRIPTION
1	1	VIN	Connect to input voltage. Connect 1µF bypass capacitor
2	2	RON	Connect a resistor to VIN and capacitor to GND to set switching frequency.
3	3	UDIM	Connect resistor divider from VIN to set under-voltage lockout threshold.
4	4	VOUT	Connect resistor divider from VOUT, scaled down feedback of VOUT.
5	5	VREF	Connect to top of resistor divider for IADJ. Bypass with 100nF ceramic capacitor.
6	6	IADJ	Connect resistor divider from VREF or directly to VREF to set analog dimming level. Can be used for thermal fold-back also.
7	7	COMP	Connect ceramic capacitor to GND to set loop compensation.
	8	SDIM	PWM dimming input for shunt FET dimming.
	9	SDRV	Connect to gate of external parallel NFET across LED load used for shunt dimming if desired.
8	10	GND	System GND. Connect to DAP.
9	11	CS	Connect to positive terminal of sense resistor at the bottom of the LED stack.
10	12	LG	Connect to gate of low-side NFET of buck regulator.
11	13	VCC	Bypass with 2.2µF ceramic capacitor to provide bias supply for controller.
12	14	BOOT	Connect 100nF ceramic capacitor to switch node and diode to VCC to provide boosted voltage for high-side gate drive.
13	15	SW	Connect to switch node of buck regulator.
14	16	HG	Connect to gate of high-side NFET of buck regulator.
		DAP	Place 6-9 vias from pad to GND plane for thermal relief

Ordering Information

ORDER NUMBER	PACKAGE TYPE	PACKAGE DRAWING	SUPPLIED AS
TPS92640PWP	14L TSSOP EXP PAD	MXA14A	94 Units in Rail
TPS92640PWPT			250 Units on Tape and Reel
TPS92640PWPR			2500 Units on Tape and Reel
TPS92641PWP	16L TSSOP EXP PAD	MXA16A	92 Units in Rail
TPS92641PWPT			250 Units on Tape and Reel
TPS92641PWPR			2500 Units on Tape and Reel

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales/Office/Distributors for availability and specifications.

	VALUE	UNITS	
VIN, UDIM, SW	–0.3 to 90	V	
	–1 (Continuous)	mA	
BOOT	–0.3 to 98.5	V	
HG	–0.3 to 90	V	
	–2.5 for 100	V/ns	
	98.5 for 100	v/ns	
	–1 to +1 (Continuous)	mA	
LG, SDRV, CS	–0.3 to +V _{CC} (Continuous)	V	
	–2.5 for 100	V/ns	
	V _{CC} + 2.5 for 100	V/ms	
	–1 to +1 (Continuous)	mA	
VCC	–0.3 to 15	V	
VREF, RON, COMP, VOUT, IADJ, SDIM	–0.3 to 6	V	
	–200 to +200 (Continuous)	µA	
GND	–0.3 to +0.3 (Continuous)	V	
	–2.5 to +2.5 for 100	V/ns	
Continuous Power Dissipation	Internally Limited		
Maximum Junction Temperature	Internally Limited		
Storage Temperature Range	–65 to +150	°C	
Maximum Lead Temperature (Soldering and Reflow) ⁽²⁾	260	°C	
ESD Rating	Human Body Model, applicable std. JEDEC22-A114-C	2	kV

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified and **do not imply** guaranteed performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics table. All voltages are with respect to the potential at the GND pin, unless otherwise specified.
- (2) Refer to TI's packaging website for more detailed information and mounting techniques.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Input Voltage Range	7		85	V
T _J Junction Temperature Range	–40		125	°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified and **do not imply** guaranteed performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics table. All voltages are with respect to the potential at the GND pin, unless otherwise specified.

ELECTRICAL CHARACTERISTICS⁽¹⁾

Unless otherwise specified $V_{IN} = 24V$. Limits appearing in **bold type** face apply over the entire junction temperature range of operation, $-40^{\circ}C$ to $125^{\circ}C$. Specifications appearing in normal type apply for $T_A = T_J = 25^{\circ}C$. Datasheet min/max specification limits are specified by design, test or statistical analysis.

PARAMETER		CONDITIONS	MIN ⁽²⁾	TYP ⁽³⁾	MAX ⁽²⁾	UNIT
STARTUP REGULATOR (V_{CC})						
V_{CCREG}	V_{CC} Regulation	$I_{CC} = 10\text{ mA}$, $V_{IN} = 24V$, $85V$	7.86	8.5	9.14	V
I_{CCLIM}	V_{CC} Current Limit	$V_{CC} = 0V$	48	63	78	mA
I_Q	Quiescent Current	$V_{UDIM} = 3.0V$, Static $V_{IN} = 7V/24V/85V$		2	3	mA
I_{SD}	Shutdown Current	$V_{UDIM} = 0V$		100		μA
V_{CC-UV}	V_{CC} UVLO Threshold	V_{CC} increasing		5.04	5.90	V
		V_{CC} decreasing	4.5	4.9		
V_{CC-HYS}	V_{CC} UVLO Hysteresis			0.17		V
REFERENCE VOLTAGE (V_{REF})						
V_{REF}	Reference Voltage	No Load, $V_{IN} = 7V/24V/85V$	2.97	3.03	3.09	V
$I_{VREFLIM}$	Current Limit	$V_{REF} = 0V$	1.3	2.1	2.9	mA
ERROR AMPLIFIER (CS, COMP)						
V_{CSREF}	CS Reference Voltage	With respect to GND		$V_{ADJ}/10$		V
$V_{CSREF-OFF}$	Error Amp Input Offset Voltage		-600	0	600	μV
I_{COMP}	COMP Sink Current			85		μA
	COMP Source Current			110		μA
g_{M-CS}	Transconductance			500		$\mu A/V$
	Linear Input Range	See ⁽⁴⁾		± 125		mV
	Transconductance Bandwidth	-6dB unloaded response ⁽⁴⁾		400		kHz
TIMERS / OVER VOLTAGE PROTECTION (R_{ON}, V_{OUT})						
$t_{OFF-MIN}$	Minimum Off-time	$CS = 0V$		230		ns
t_{ON-MIN}	Minimum On-time			235		
t_{ON}	Programmed On-time	$V_{VOUT} = 2V$, $R_{ON} = 25\text{ k}\Omega$, $C_{ON} = 1\text{ nF}$		2.08		μs
R_{RON}	RON Pull-down Resistance			35	120	Ω
t_{CL}	Current Limit Off-time			270		μs
t_{D-ON}	RON Thresh - HG Falling Delay			25		ns
V_{TH-OVP}	V_{OUT} Over-Voltage Threshold	V_{OUT} rising	2.85	3.05	3.25	V
$V_{HYS-OVP}$	V_{OUT} Over-Voltage Hysteresis			0.13		V
GATE DRIVER (HG, LG, BOOT, SW)						
R_{SRC-LG}	LG Sourcing Resistance	LG = High		1.5	6.0	Ω
R_{SNK-LG}	LG Sinking Resistance	LG = Low		1	4.5	Ω
R_{SRC-HG}	HG Sourcing Resistance	HG = High		3.9	6.0	Ω
R_{SNK-HG}	HG Sinking Resistance	HG = Low		1.1	4.5	Ω
$V_{TH-BOOT}$	BOOT UVLO Threshold	BOOT-SW rising	1.9	3.4	4.5	V
$V_{HYS-BOOT}$	BOOT UVLO Hysteresis	BOOT-SW falling		1.8		V
T_{D-HL}	HG to LG deadtime	HG fall to LG rise		60		ns
T_{D-LH}	LG to HG deadtime	LG fall to HG rise		60		ns

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified and **do not imply** guaranteed performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics table. All voltages are with respect to the potential at the GND pin, unless otherwise specified.
- (2) All limits specified at room temperature (standard typeface) and at temperature extremes (**bold typeface**). All room temperature limits are 100% production tested. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
- (3) Typical numbers are at $25^{\circ}C$ and represent the most likely norm.
- (4) These electrical parameters are specified by design, and are not verified by test.

ELECTRICAL CHARACTERISTICS⁽¹⁾ (continued)

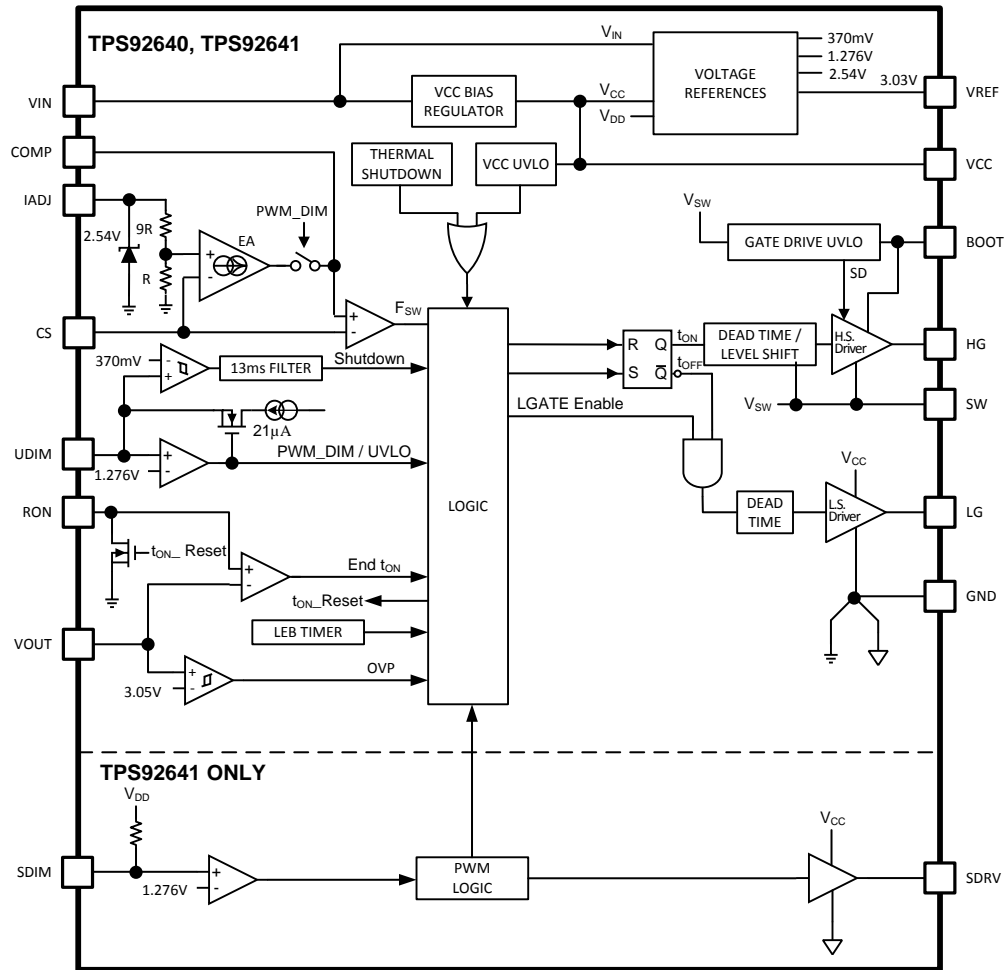
Unless otherwise specified $V_{IN} = 24V$. Limits appearing in **bold type** face apply over the entire junction temperature range of operation, $-40^{\circ}C$ to $125^{\circ}C$. Specifications appearing in normal type apply for $T_A = T_J = 25^{\circ}C$. Datasheet min/max specification limits are specified by design, test or statistical analysis.

PARAMETER		CONDITIONS	MIN ⁽²⁾	TYP ⁽³⁾	MAX ⁽²⁾	UNIT
PWM DIMMING (SDIM, SDRV) (TPS92641 only.)						
$R_{SRC-DDRV}$	SDRV Sourcing Resistance	SDRV = High		5.6	30.0	W
$t_{SDIM-RIS}$	SDIM to SDRV Rising Delay	SDIM rising		68	100	ns
$t_{SDIM-FALL}$	SDIM to SDRV Falling Delay	SDIM falling		29	70	
$V_{SDIM-RIS}$	SDIM Rising Threshold	SDIM rising		1.29	1.74	V
$V_{SDIM-FALL}$	SDIM Falling Threshold	SDIM falling	0.5			V
$R_{SDIM-PU}$	SDIM Pull-Up Resistance			90		kW
ANALOG ADJUST (IADJ)						
$V_{ADJ-MAX}$	IADJ Clamp Voltage		2.46	2.54	2.62	V
R_{ADJ}	IADJ Input Impedance			1		MΩ
UNDER-VOLTAGE / PWM (UDIM)						
$V_{TH-UDIM}$	UDIM Startup Threshold	UDIM rising	1.210	1.276	1.342	V
$I_{HYS-UDIM}$	UDIM Hysteresis Current		12	21	30	μA
$t_{UDIM-RIS}$	UDIM to HG/LG Rising Delay	UDIM rising		168	260	ns
$t_{UDIM-FALL}$	UDIM to HG/LG Falling Delay	UDIM falling		174	280	ns
$V_{UDIM-LP}$	UDIM Low Power Threshold			370		mV
$T_{UDIM-DET}$	UDIM Shutdown Detect Timer	UDIM falling	8.5	13		ms
THERMAL SHUTDOWN						
T_{SD}	Thermal Shutdown Threshold	See ⁽⁵⁾		165		°C
T_{HYS}	Thermal Shutdown Hysteresis	See ⁽⁵⁾		20		°C
THERMAL RESISTANCE						
$\theta_{JA-TPS92640}$	Junction to Ambient	14L TSSOP EXP PAD ⁽⁶⁾		40.0		°C/W
$\theta_{JA-TPS92641}$	Junction to Ambient	16L TSSOP EXP PAD ⁽⁶⁾		37.4		°C/W

(5) These electrical parameters are specified by design, and are not verified by test.

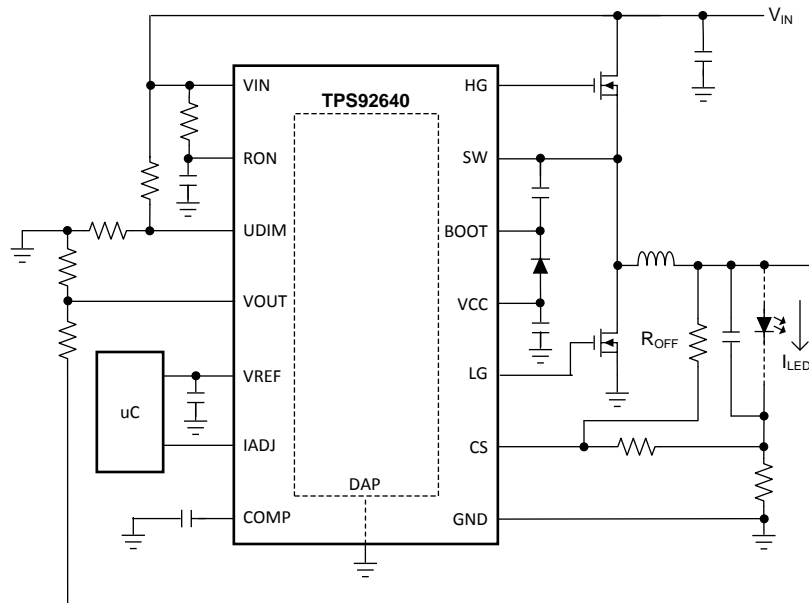
(6) Junction-to-ambient thermal resistance is highly board-layout dependent. In applications where high maximum power dissipation exists, namely driving a large MOSFET at high switching frequency from a high input voltage, special care must be paid to thermal dissipation issues during board design. In high-power dissipation applications, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP} = 125^{\circ}C$), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} - (\theta_{JA} \times P_{D-MAX})$.

FUNCTIONAL BLOCK DIAGRAM

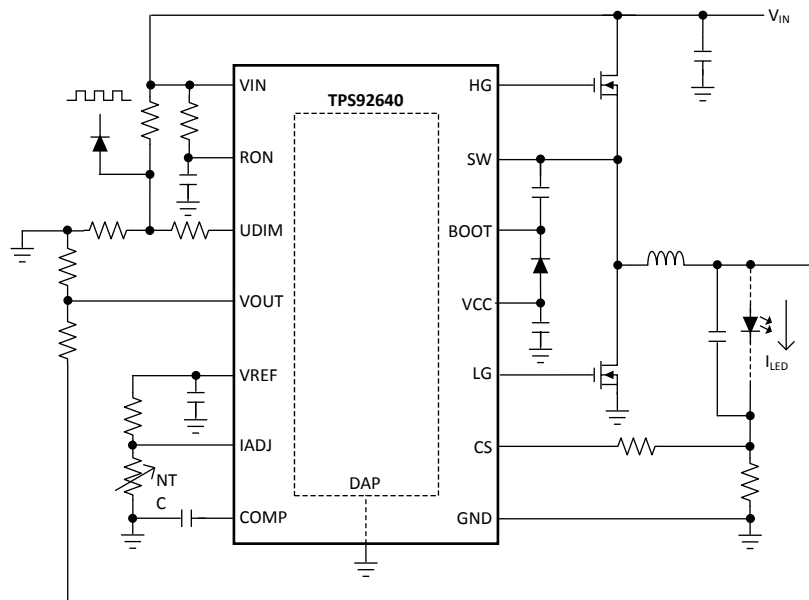


PRODUCT PREVIEW

TPS92640 - Precision Analog Dimming Application

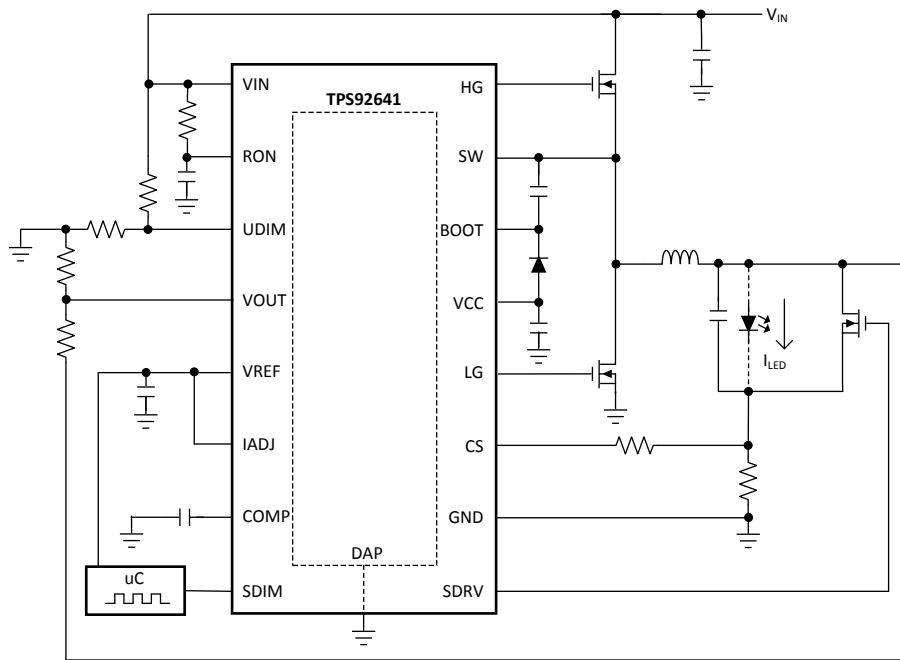


TPS92640 – PWM Dimming Application with Thermal Fold-back



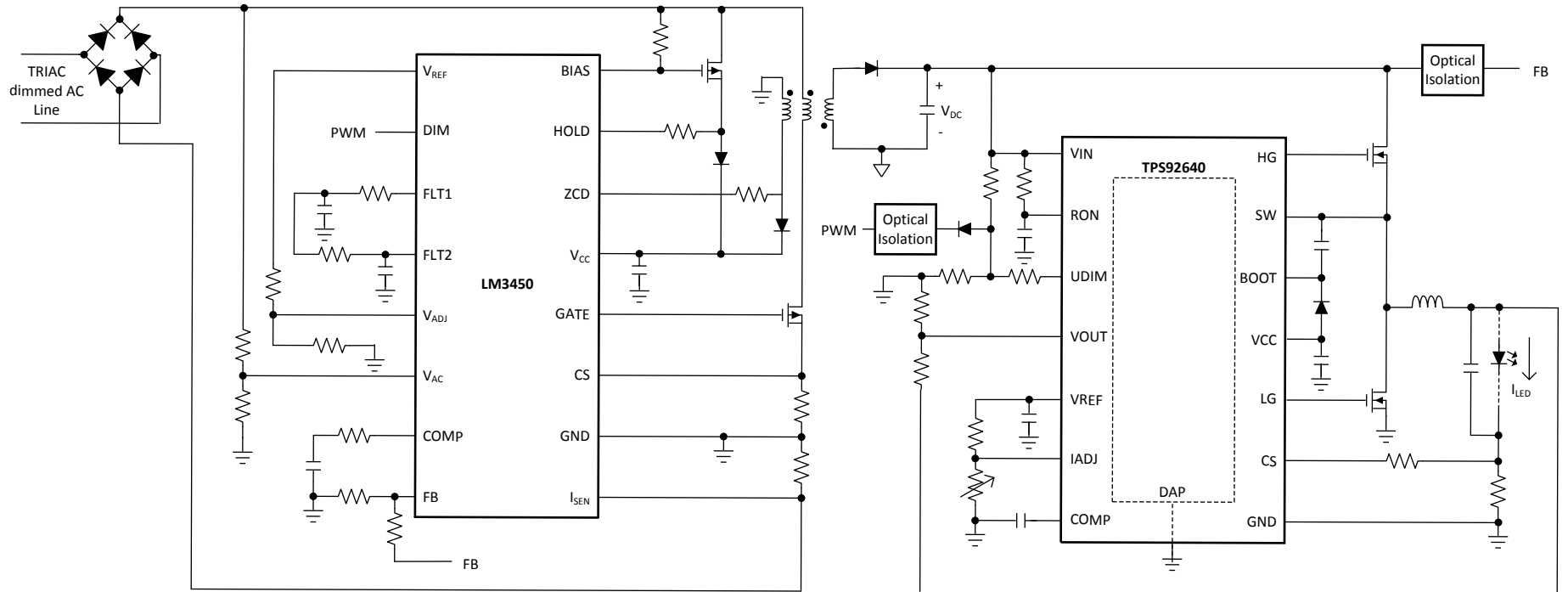
PRODUCT PREVIEW

TPS92641 – Shunt FET PWM Dimming Application



PRODUCT PREVIEW

TPS92640 – AC/DC TRIAC Dimming Application (with LM3450)



PRODUCT PREVIEW

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