RS-232 TRANSCEIVER WITH SPLIT SUPPLY PIN FOR LOGIC SIDE

Check for Samples: **TRS3253E**

FEATURES

- V_L Pin for Compatibility With Mixed-Voltage Systems Down to 1.8 V on Logic Side
- Enhanced ESD Protection on RIN Inputs and DOUT Outputs
  - ±8 kV IEC 61000-4-2 Air-Gap Discharge
  - ±8 kV IEC 61000-4-2 Contact Discharge
  - ±15 kV Human-Body Model
- Low 300-µA Supply Current
- Specified 1000-kbps Data Rate
- Auto Powerdown Plus Feature

APPLICATIONS

- Hand-Held Equipment
- PDAs
- Cell Phones
- Battery-Powered Equipment
- Data Cables

RSM PACKAGE
(TOP VIEW)
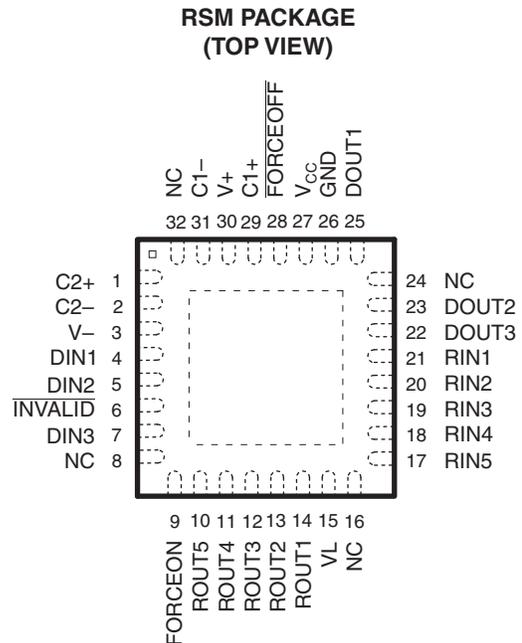
NC – No internal connection

DESCRIPTION/ORDERING INFORMATION

The TRS3253E is a three-driver and five-receiver RS-232 interface device, with split supply pins for mixed-signal operations. All RS-232 inputs and outputs are protected to ±8 kV using the IEC 61000-4-2 Air-Gap Discharge method, ±8 kV using the IEC 61000-4-2 Contact Discharge method, and ±15 kV using the Human-Body Model.

The charge pump requires only four small 0.1-µF capacitors for operation from a 3.3-V supply. The TRS3253E is capable of running at data rates up to 1000 kbps, while maintaining RS-232-compliant output levels.

The TRS3253E has a unique V_L pin that allows operation in mixed-logic voltage systems. Both driver in (DIN) and receiver out (ROUT) logic levels are pin programmable through the V_L pin. This eliminates the need for additional voltage level shifter while interfacing with low-voltage microcontroller or UARTs. The TRS3253E is available in a space-saving QFN package (4 mm × 4 mm RSM).

Auto-powerdown plus can be disabled when FORCEON and FORCEOFF are high. With auto-powerdown plus enabled, the device activates automatically when a valid signal is applied to any receiver or driver input. INVALID is high (valid data) if any receiver input voltage is greater than 2.7 V or less than –2.7 V, or has been between –0.3 V and 0.3 V for less than 30 µs. INVALID is low (invalid data) if all receiver input voltages are between –0.3 V and 0.3 V for more than 30 µs. Refer to Figure 5 for receiver input levels.

ORDERING INFORMATION

T_A	PACKAGE[1] [2]	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RSM	TRS3253EIRSMR	RS53EI

[1] Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
[2] For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

⚠ Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

FUNCTION TABLES

Each Driver[(1)]

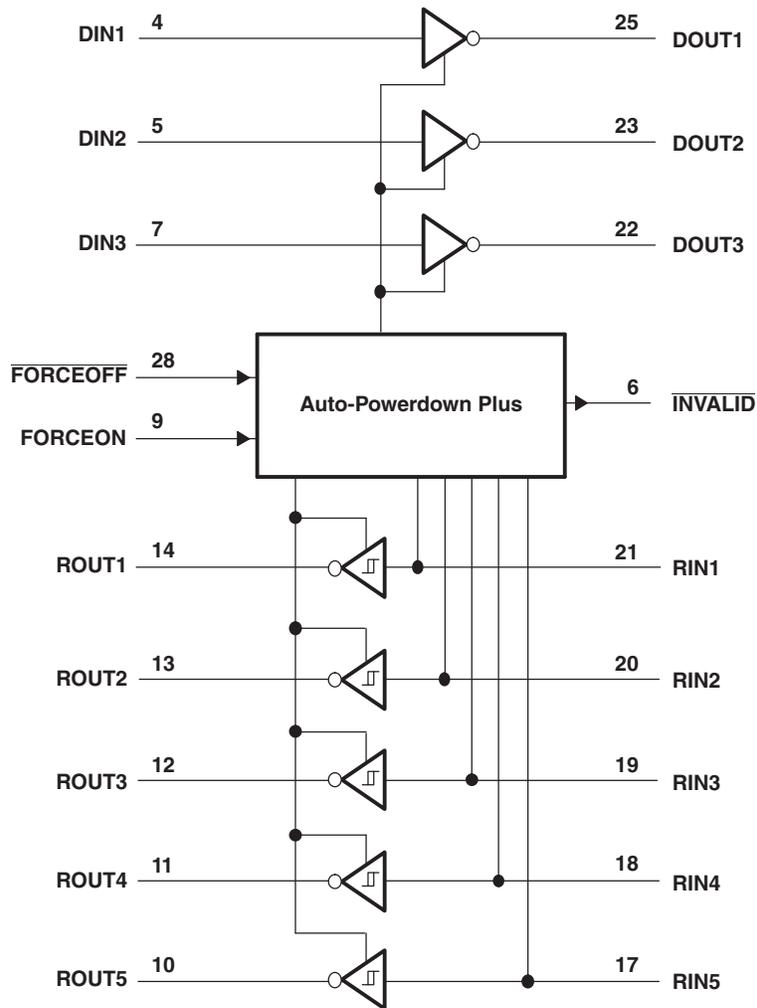| INPUTS				OUTPUT DOUT	DRIVER STATUS
DIN	**FORCEON**	**FORCEOFF**	**TIME ELAPSED SINCE LAST RIN OR DIN TRANSITION**		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown plus disabled
H	H	H	X	L	Normal operation with auto-powerdown plus disabled
L	L	H	<30 s	H	Normal operation with auto-powerdown plus enabled
H	L	H	<30 s	L	Normal operation with auto-powerdown plus enabled
L	L	H	>30 s	Z	Powered off by auto-powerdown plus feature
H	L	H	>30 s	Z	Powered off by auto-powerdown plus feature

(1)   H = high level, L = low level, X = irrelevant, Z = high impedance

Each Receiver[(1)]

INPUTS			OUTPUTS	RECEIVER STATUS
RIN1–RIN5	**FORCEOFF**	**TIME ELAPSED SINCE LAST RIN OR DIN TRANSITION**	**ROUT1-ROUT5**	
X	L	X	Z	Powered off
L	H	<30 s	H	Normal operation with auto-powerdown plus disabled/enabled
H	H	<30 s	L	Normal operation with auto-powerdown plus disabled/enabled
Open	H	<30 s	H	Normal operation with auto-powerdown plus disabled/enabled

(1)   H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

Product Folder Link(s): *TRS3253E*

FUNCTIONAL BLOCK DIAGRAM

DIN1   4   25   DOUT1

DIN2   5   23   DOUT2

DIN3   7   22   DOUT3

FORCEOFF   28

Auto-Powerdown Plus   6   INVALID

FORCEON   9

ROUT1   14   21   RIN1

ROUT2   13   20   RIN2

ROUT3   12   19   RIN3

ROUT4   11   18   RIN4

ROUT5   10   17   RIN5

TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	RSM	
C1+, C2+	29, 1	Positive terminal of the voltage-doubler charge-pump capacitor
V+	30	5.5-V supply generated by the charge pump
C1–, C2-	31, 2	Negative terminal of the voltage-doubler charge-pump capacitor
INVALID	6	Invalid Output Pin
V–	3	–5.5-V supply generated by the charge pump
DIN1 DIN2 DIN3	4 5 7	Driver inputs
ROUT5 - ROUT1	10, 11, 12, 13, 14	Receiver outputs. Swing between 0 and V_L.
V_L	15	Logic-level supply. All CMOS inputs and outputs are referenced to this supply.
RIN5-RIN1	17, 18, 19, 20, 21	RS-232 receiver inputs
DOUT3 DOUT2 DOUT1	22 23 25	RS-232 driver outputs
GND	26	Ground
V_{CC}	27	3-V to 5.5-V supply voltage
$\overline{\text{FORCEOFF}}$	28	Powerdown Control input (Refer to Truth Table)
FORCEON	9	Powerdown Control input (Refer to Truth Table)

ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
	V_{CC} to GND		–0.3	6	V
	V_L to GND		–0.3	V_{CC} + 0.3	V
	V+ to GND		–0.3	7	V
	V– to GND		0.3	–7	V
	V+ + |V–|[2]			13	V
V_I	Input voltage	DIN, $\overline{\text{FORCEOFF}}$ to GND, FORCEON to GND	–0.3	6	V
		RIN to GND		±25	
V_O	Output voltage	DOUT to GND		±13.2	V
		ROUT	–0.3	V_L + 0.3	
	Continuous power dissipation	T_A = 70°C, 32-pin RSM (derate 7 mW/°C above 70°C)		TBD	mW
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
(2) V+ and V– can have maximum magnitudes of 7 V, but their absolute difference cannot exceed 13 V.

RECOMMENDED OPERATING CONDITIONS

				MIN	MAX	UNIT
V_{CC}	Supply voltage			3	5.5	V
V_L	Supply voltage			1.65	V_{CC}	V
	Input logic threshold low	DIN, FORCEOFF, FORCEON	V_L = 3 V or 5.5 V		0.8	V
			V_L = 2.3 V		0.6	
			V_L = 1.65 V		0.5	
	Input logic threshold high	DIN, FORCEOFF, FORCEON	V_L = 5.5 V	2.4		V
			V_L = 3 V	2.0		
			V_L = 2.7 V	1.4		
			V_L = 1.95 V	1.25		
	Operating temperature		TRS3253EIRSMR	–40	85	°C
	Receiver input voltage			–25	25	V

ELECTRICAL CHARACTERISTICS[1]

over operating free-air temperature range, V_{CC} = V_L = 3 V to 5.5 V, C1–C4 = 0.1 µF (tested at 3.3 V ± 10%), C1 = 0.047 µF, C2–C4 = 0.33 µF (tested at 5 V ± 10%) (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	MIN	TYP[2]	MAX	UNIT
I_I	Input leakage current	FORCEOFF, FORCEON			±0.01	±1	µA
I_{CC}	Supply current (T_A = 25°C)	Auto-powerdown plus disabled	No load, FORCEOFF and FORCEON at V_{CC}		0.5	1	mA
		Powered off	No load, FORCEOFF at GND		1	10	µA
		Auto-powerdown plus enabled	No load, FORCEOFF at V_{CC}, FORCEON at GND, All RIN are open or grounded		1	10	

(1) Testing supply conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.15 V; C1–C4 = 0.22 µF at V_{CC} = 3.3 V ± 0.3 V; and C1 = 0.047 µF and C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

ESD PROTECTION

PARAMETER	TEST CONDITIONS	TYP	UNIT
RIN, DOUT	Human-Body Model	±15	kV
	IEC 61000-4-2 Air-Gap Discharge	±8	
	IEC 61000-4-2 Contact Discharge	±8	

RECEIVER SECTION

Electrical Characteristics

over operating free-air temperature range, $V_{CC} = V_L$ = 3 V to 5.5 V, C1–C4 = 0.1 µF (tested at 3.3 V ± 10%), C1 = 0.047 µF, C2–C4 = 0.33 µF (tested at 5 V ± 10%), $T_A = T_{MIN}$ to T_{MAX} (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
I_{off}	Output leakage current	ROUT, receivers disabled			±0.05	±10	µA
V_{OL}	Output voltage low	I_{OUT} = 1.6 mA				0.4	V
V_{OH}	Output voltage high	I_{OUT} = −1 mA		V_L − 0.6	V_L − 0.1		V
$V_{IT−}$	Input threshold low	T_A = 25°C	V_L = 5 V	0.8	1.2		V
			V_L = 3.3 V	0.6	1.5		
V_{IT+}	Input threshold high	T_A = 25°C	V_L = 5 V		1.8	2.4	V
			V_L = 3.3 V		1.5	2.4	
V_{hys}	Input hysteresis				0.5		V
	Input resistance	T_A = 25°C		3	5	7	kΩ

(1) Typical values are at $V_{CC} = V_L$ = 3.3 V, T_A = 25°C

Switching Characteristics

over operating free-air temperature range, $V_{CC} = V_L$ = 3 V to 5.5 V, C1–C4 = 0.1 µF (tested at 3.3 V ± 10%), C1 = 0.047 µF, C2–C4 = 0.33 µF (tested at 5 V ± 10%), $T_A = T_{MIN}$ to T_{MAX} (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	TYP[1]	UNIT
t_{PHL}	Receiver propagation delay	Receiver input to receiver output, C_L = 150 pF	0.15	µs
t_{PLH}			0.15	
$t_{PHL} − t_{PLH}$	Receiver skew		50	ns
t_{en}	Receiver output enable time	From $\overline{FORCEOFF}$	200	ns
t_{dis}	Receiver output disable time	From $\overline{FORCEOFF}$	200	ns

(1) Typical values are at $V_{CC} = V_L$ = 3.3 V, T_A = 25°C.

Product Folder Link(s): *TRS3253E*

DRIVER SECTION

Electrical Characteristics

over operating free-air temperature range, $V_{CC} = V_L = 3$ V to 5.5 V, C1–C4 = 0.1 µF (tested at 3.3 V ± 10%), C1 = 0.047 µF, C2–C4 = 0.33 µF (tested at 5 V ± 10%), $T_A = T_{MIN}$ to T_{MAX} (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
V_{OH}	Output voltage swing	All driver outputs loaded with 3 kΩ to ground, V_{CC}= 3.1V to 5.5V	±5	±5.4		V
r_O	Output resistance	V_{CC} = V+ = V− = 0, Driver output = ±2 V	300	10M		Ω
I_{OS}	Output short-circuit current	V_{T_OUT} = 0			±60	mA
I_{OZ}	Output leakage current	V_{T_OUT} = ±12 V, $\overline{\text{FORCEOFF}}$ = GND, V_{CC} = 3 V to 3.6 V			±25	µA
		V_{T_OUT} = ±12 V, $\overline{\text{FORCEOFF}}$ = GND, V_{CC} = 4.5 V to 5.5 V				
	Driver input hysteresis				0.5	V
	Input leakage current	DIN, $\overline{\text{FORCEOFF}}$, FORCEON		±0.01	±1	µA

(1) Typical values are at $V_{CC} = V_L = 3.3$ V, $T_A = 25$°C

Timing Requirements

over operating free-air temperature range, $V_{CC} = V_L = 3$ V to 5.5 V, C1–C4 = 0.1 µF (tested at 3.3 V ± 10%), C1 = 0.047 µF, C2–C4 = 0.33 µF (tested at 5 V ± 10%), $T_A = T_{MIN}$ to T_{MAX} (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
	Maximum data rate	$R_L = 3$ kΩ, $C_L = 200$ pF, One driver switching		1000			kbps
	Time-to-exit powerdown	$|V_{T\_OUT}| > 3.7$ V				100	µs
$|t_{PHL} - t_{PLH}|$	Driver skew[2]					100	ns
	Transition-region slew rate	$V_{CC} = 3.3$ V, $T_A = 25$°C, $R_L = 3$ kΩ to 7 kΩ, Measured from 3 V to –3 V or –3 V to 3 V	$C_L = 150$ pF to 1000 pF	15		150	V/µs

(1) Typical values are at $V_{CC} = V_L = 3.3$ V, $T_A = 25$°C.
(2) Driver skew is measured at the driver zero crosspoint.

AUTO-POWERDOWN SECTION

### Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 6)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{IT+(valid)}$	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_L		2.7	V
$V_{IT-(valid)}$	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_L	–2.7		V
$V_{T(invalid)}$	Receiver input threshold for $\overline{INVALID}$ low-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_L	–0.3	0.3	V
V_{OH}	$\overline{INVALID}$ high-level output voltage	I_{OH} = -1 mA, FORCEON = GND, $\overline{FORCEOFF}$ = V_L	V_L – 0.6		V
V_{OL}	$\overline{INVALID}$ low-level output voltage	I_{OL} = 1.6 mA, FORCEON = GND, $\overline{FORCEOFF}$ = V_L		0.4	V

Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 6)

PARAMETER		MIN	TYP[1]	MAX	UNIT
t_{valid}	Propagation delay time, low- to high-level output		0.1		µs
$t_{invalid}$	Propagation delay time, high- to low-level output		50		µs
t_{en}	Supply enable time		25		µs
t_{dis}	Receiver or driver edge to auto-powerdown plus	15	30	60	s

(1) All typical values are at V_{CC} = V_L = 3.3 V and TA = 25°C.

Product Folder Link(s): *TRS3253E*

APPLICATION INFORMATION
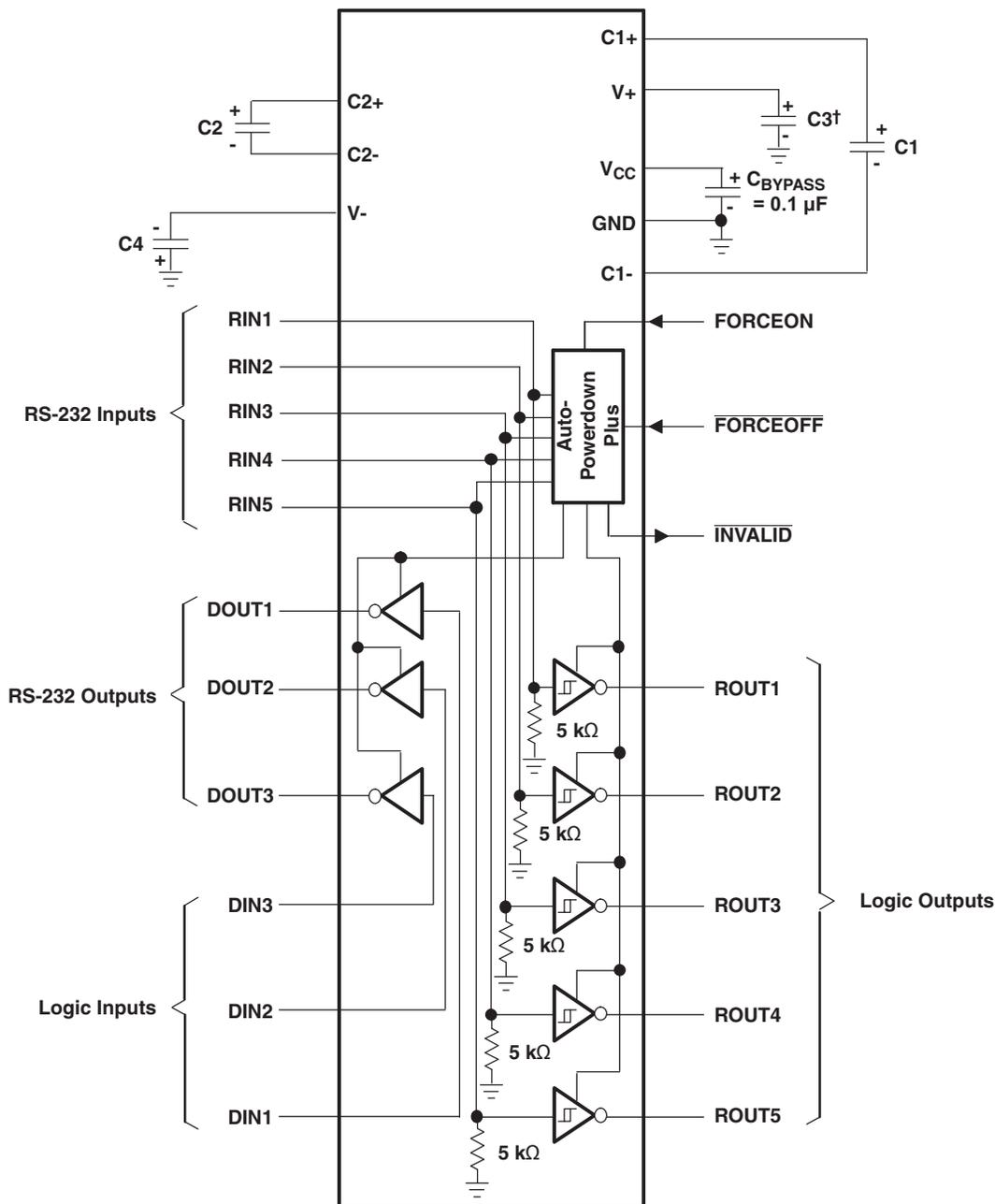
† C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

   B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

V_{CC}	C1	C2, C3, and C4
3.3 V $\pm$ 0.3 V	0.1 µF	0.1 µF
5 V $\pm$ 0.5 V	0.047 µF	0.33 µF
3 V to 5.5 V	0.1 µF	0.47 µF

Figure 1. Typical Operating Circuit and Capacitor Values

PARAMETER MEASUREMENT INFORMATION

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

$$SR(tr) = \frac{6\ V}{t_{THL}\ or\ t_{TLH}}$$

TEST CIRCUIT

VOLTAGE WAVEFORMS
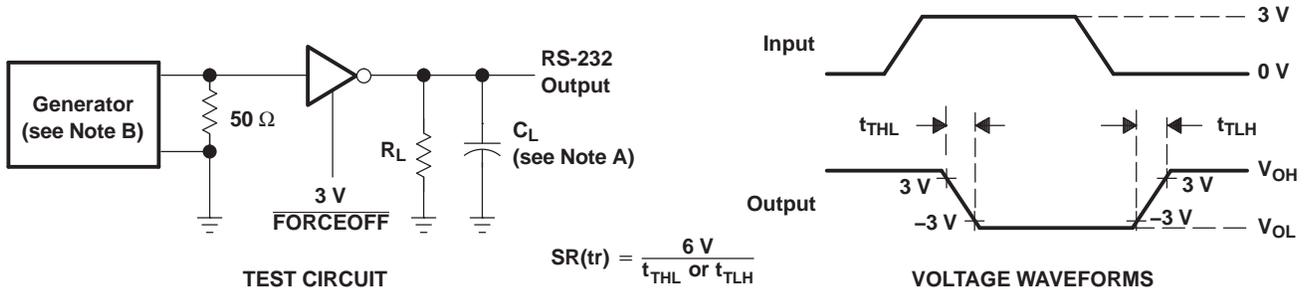
Figure 2. Driver Slew Rate

C. C_L includes probe and jig capacitance.

D. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

TEST CIRCUIT

VOLTAGE WAVEFORMS
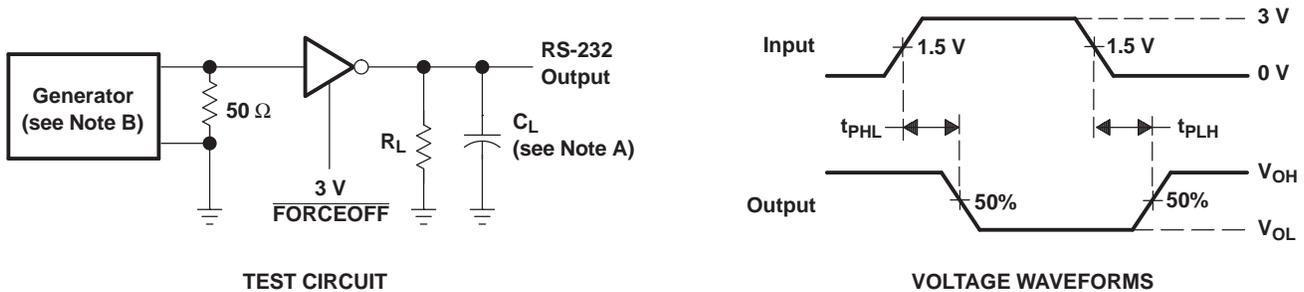
Figure 3. Driver Pulse Skew

E. C_L includes probe and jig capacitance.

F. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

TEST CIRCUIT

VOLTAGE WAVEFORMS
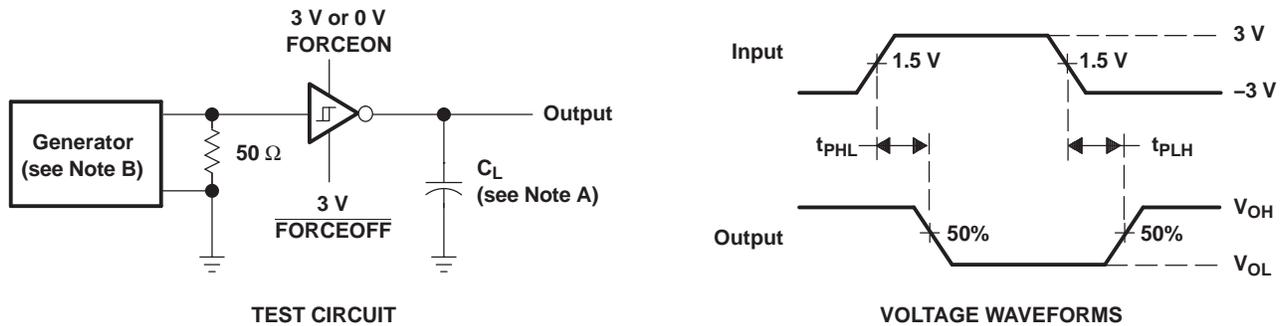
Figure 4. Receiver Propagation Delay Times

G. C_L includes probe and jig capacitance.

H. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

I. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

J. t_{PZL} and t_{PZH} are the same as t_{en}.

Product Folder Link(s): *TRS3253E*

PARAMETER MEASUREMENT INFORMATION (continued)

TEST CIRCUIT

VOLTAGE WAVEFORMS
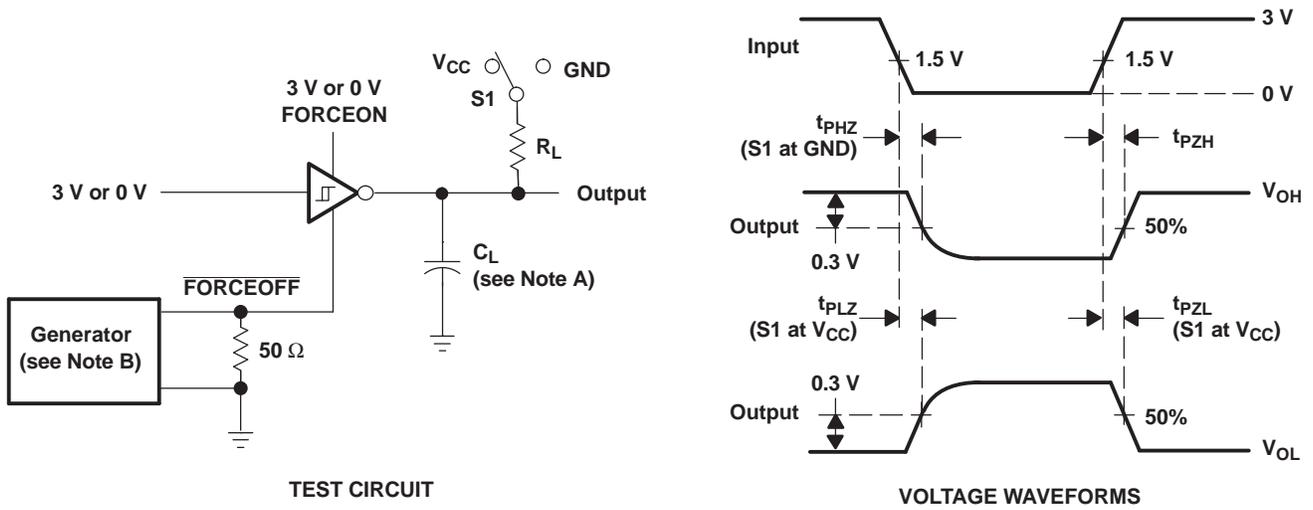
Figure 5. Receiver Enable and Disable Times

PARAMETER MEASUREMENT INFORMATION (continued)
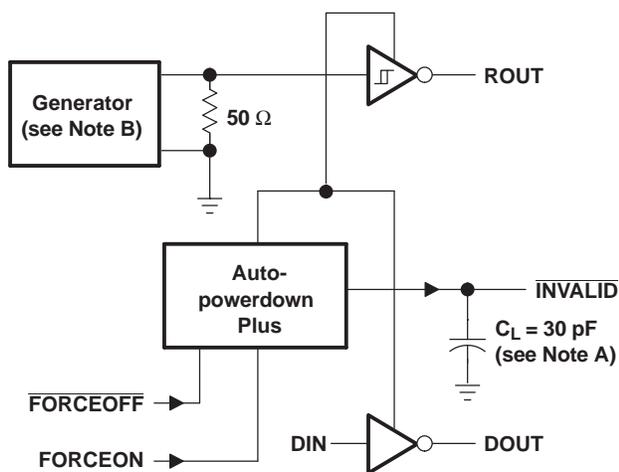
TEST CIRCUIT
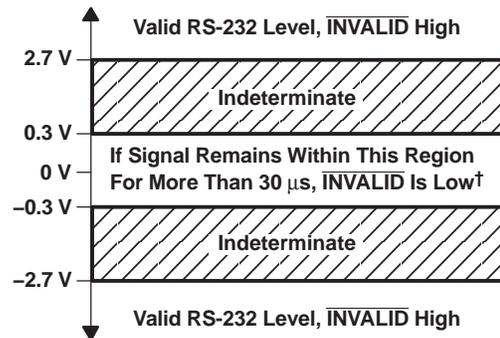
† Auto-powerdown plus disables drivers and reduces supply current to 1 μA.

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 5 kbit/s, Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

Voltage Waveforms and Timing Diagrams
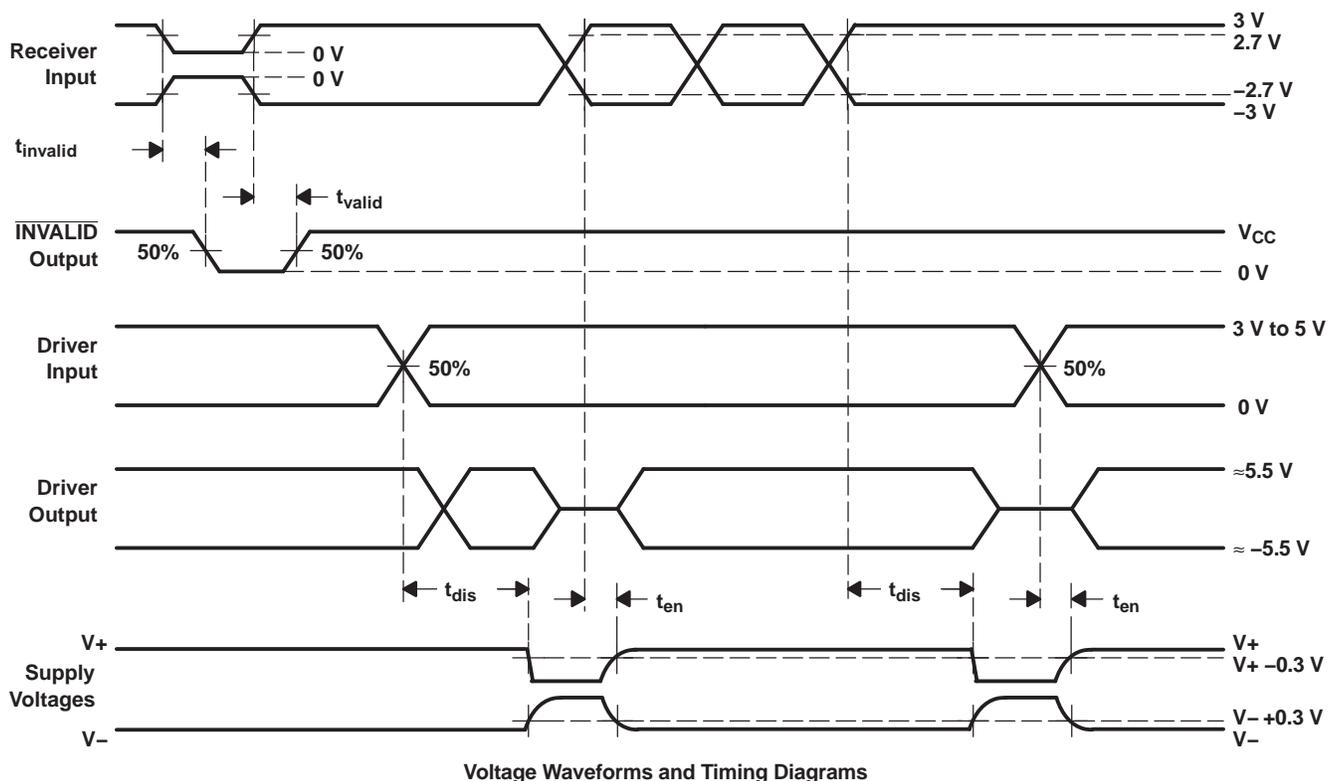
Figure 6. INVALID Propagation-Delay Times and Supply-Enabling Time

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TRS3253EIRSMR	ACTIVE	VQFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

RSM (S−PVQFN−N32)   PLASTIC QUAD FLATPACK NO−LEAD

$\dfrac{4,15}{3,85}$ [A]

[B]

$\dfrac{4,15}{3,85}$

PIN 1 INDEX AREA
TOP AND BOTTOM

32

1

$\dfrac{1,00}{0,80}$

0,20 NOMINAL
LEAD FRAME

SEATING PLANE

▱ | 0,08 | C

$\dfrac{0,05}{0,00}$

[C]

32X $\dfrac{0,50}{0,30}$

1   8

32   9

4X | 2,80 |

EXPOSED THERMAL PAD

⟨D⟩

24   17

16

| 0,40 |

32X $\dfrac{0,25}{0,15}$

⊕ | 0,10 Ⓜ | C | A | B |
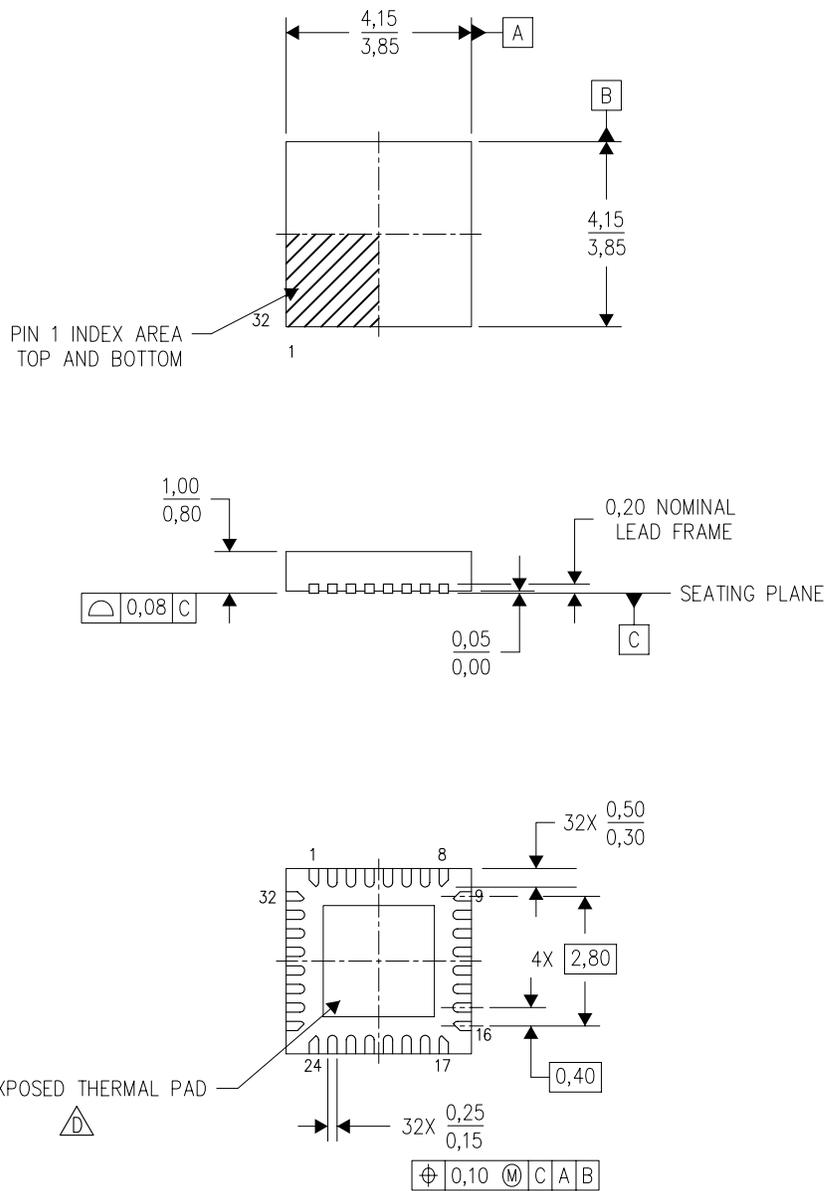
4207560/B   03/10

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
          B. This drawing is subject to change without notice.
          C. QFN (Quad Flatpack No−Lead) Package configuration.
          ⟨D⟩ The package thermal pad must be soldered to the board for thermal and mechanical performance.
               See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

TEXAS
INSTRUMENTS
www.ti.com

RSM (S−PVQFN−N32)   PLASTIC QUAD FLATPACK NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.
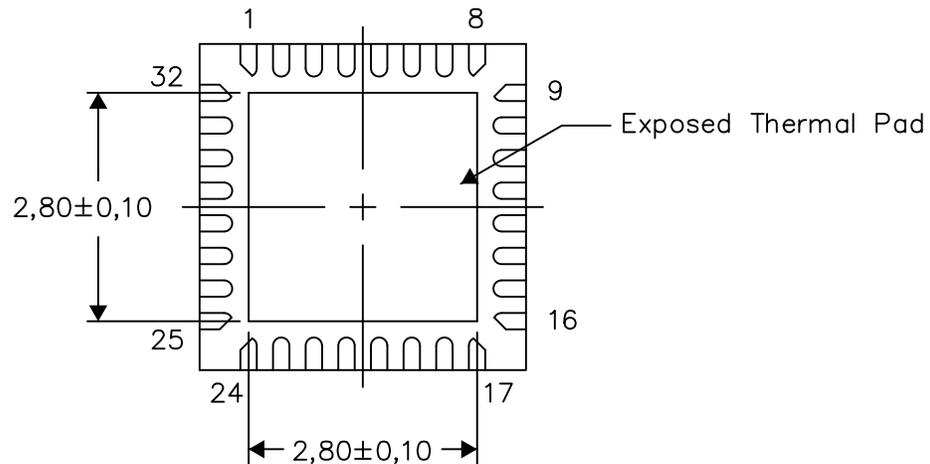
Bottom View

Exposed Thermal Pad Dimensions

4207868−2/G   08/12

NOTE: All linear dimensions are in millimeters

RSM (S−PVQFN−N32)   PLASTIC QUAD FLATPACK NO−LEAD

Example Board Layout

28x0,4

Note D

2,8 3,2 4,8

2,8
3,2
4,8

Non Solder Mask Defined Pad

R0,1

0,1

0,8

0,2

0,05

All Around

Example Stencil Design
0.125 Thick Stencil or Thinner
(Note E)

32x0,20   28x0,4

R0,1

0,3   0,3

4x1,2   4x
1,2

3,20 4,80

3,20

4,80

(73% Printed Solder Coverage by Area)

Example
Solder Mask Opening
(Note F)

Example
Pad Geometry
(Note C)

Example Via Layout Design
Via layout may vary depending
on layout constraints
(Note D, F)

⌀0,3

6x1,0

6x1,0

4207134/F 04/12
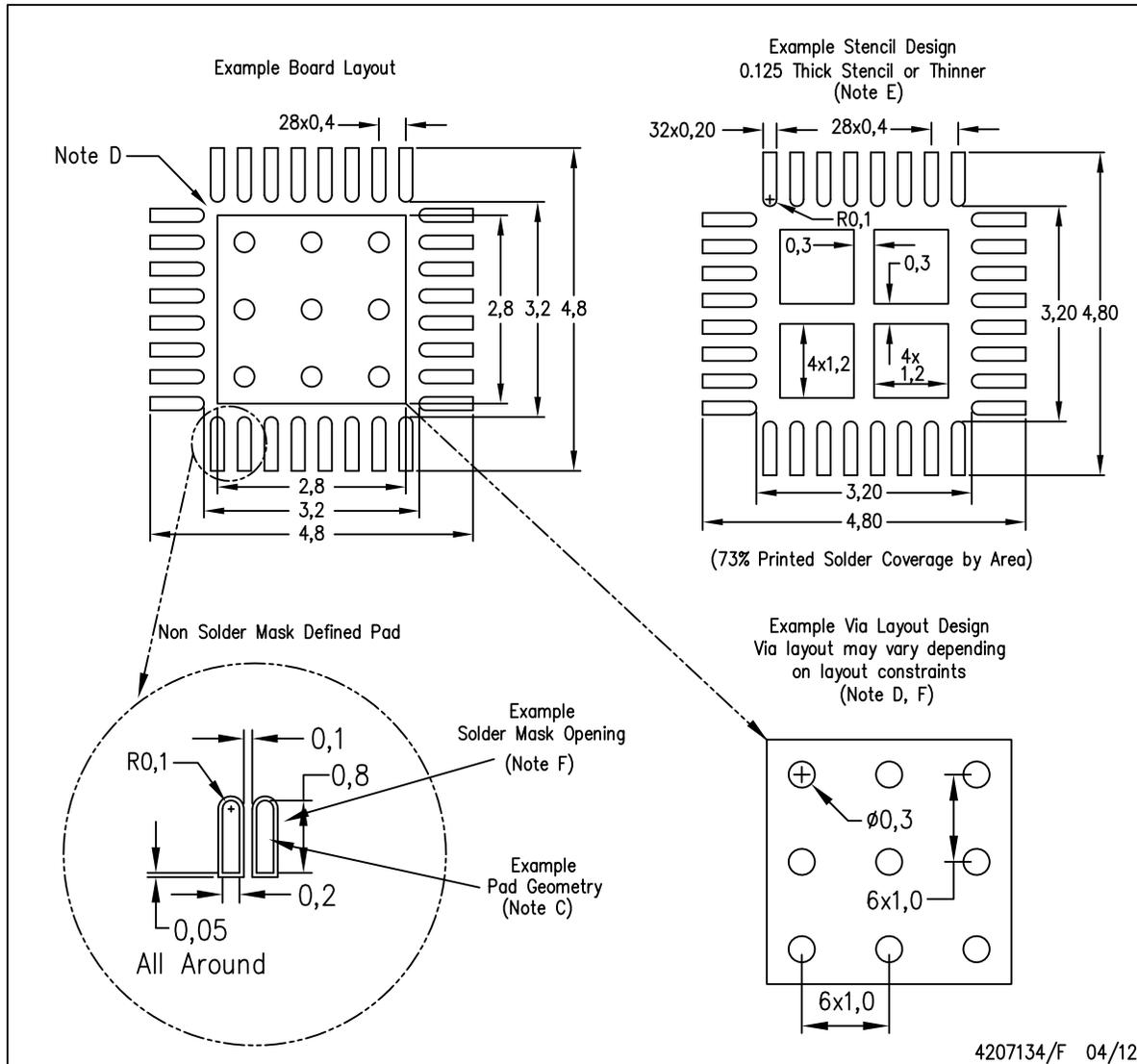
NOTES: A. All linear dimensions are in millimeters.
          B. This drawing is subject to change without notice.
          C. Publication IPC−7351 is recommended for alternate designs.
          D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat−Pack
              Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
              for specific thermal information, via requirements, and recommended board layout. These documents are available at
              www.ti.com <http://www.ti.com>.
          E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
          F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting
              recommendations for vias placed in the thermal pad.

TEXAS
INSTRUMENTS
www.ti.com

IMPORTANT NOTICE

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		