# 0.5Ω Dual SPDT Bidirectional Analog Switch

**Check for Samples: TS3A5223**

## FEATURES

- **Low ON Resistance Switches**
  - **0.5 Ω (Typical) at 3.6V**
  - **0.8 Ω(Typical) at 1.8V**
- **Wide Supply Range: 1.65 V to 3.6 V**
- **1.0 V Compatible Logic Interface**
- **High Switch Bandwidth 75 MHz**
- **0.01% THD Across Entire Band**
- **Specified min Break-before-make**
- **Bi-directional Switching**
- **–80 dB Channel-to-Channel Cross Talk**
- **–72 dB Channel-to-Channel OFF Isolation of Very Low Power Dissipation and Leakage Currents**
- **Very Small QFN-10 Package: 1.8mm × 1.4mm**
- **ESD Protection on all Pins**
  - **2kV HBM, 500 V CDM**

## APPLICATIONS

- **Portable Electronics**
- **Smarphones, Tablets**
- **Home Electronics**
- **Wireline Communication**

## DESCRIPTION

The TS3A5223 is a high-speed dual analog switch with break-before-make and bi-directional signal switching capability. The TS3A5223 can be used as a dual 2:1 multiplexer or a 1:2 dual de-multiplexer.

The TS3A5223 offers very low ON resistance, very low THD, channel-to-channel crosstalk and very high OFF isolation. These features make TS3A5223 suitable for application in Audio signal routing and switching applications.

The TS3A5223 control logic supports 1.0V-3.6V CMOS logic levels. The logic interface allows direct interface with a wide range of CPUs and microcontrollers without increasint the current drawn from supply (ICC) and thus lowering power consumption.

**Table 1. TS3A5223 Function Table**

| SEL1 | SEL2 | COM1 | COM2 |
|---|---|---|---|
| 0 | 0 | NC1 | NC2 |
| 1 | 1 | NO1 | NO2 |
| 1 | 0 | NO1 | NC2 |
| 0 | 1 | NC1 | NO2 |

PRODUCT PREVIEW

## TS3A5223 FUNCTIONAL DIAGRAM

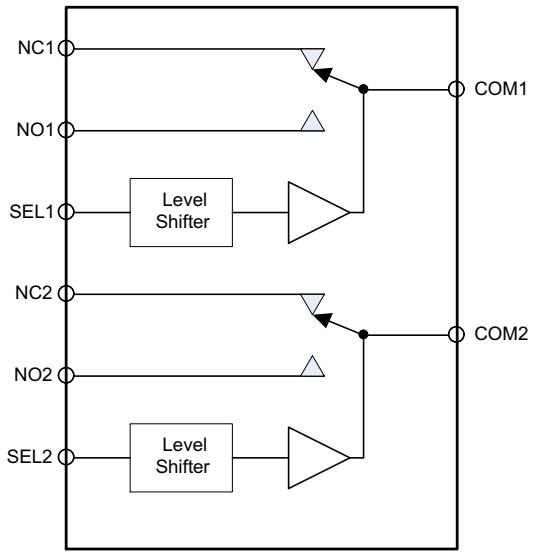
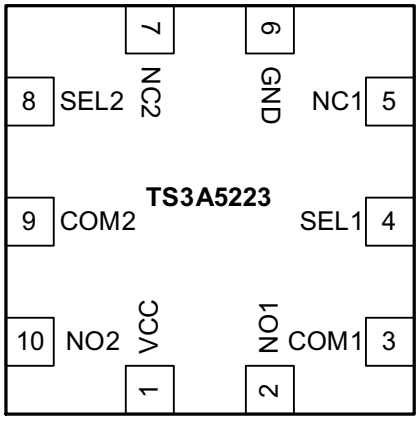



**Figure 1. Functional Diagram**

## TS3A5223 RSW (Top View)



## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TS3A5223RSWR | PREVIEW | UQFN | RSW | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | | |

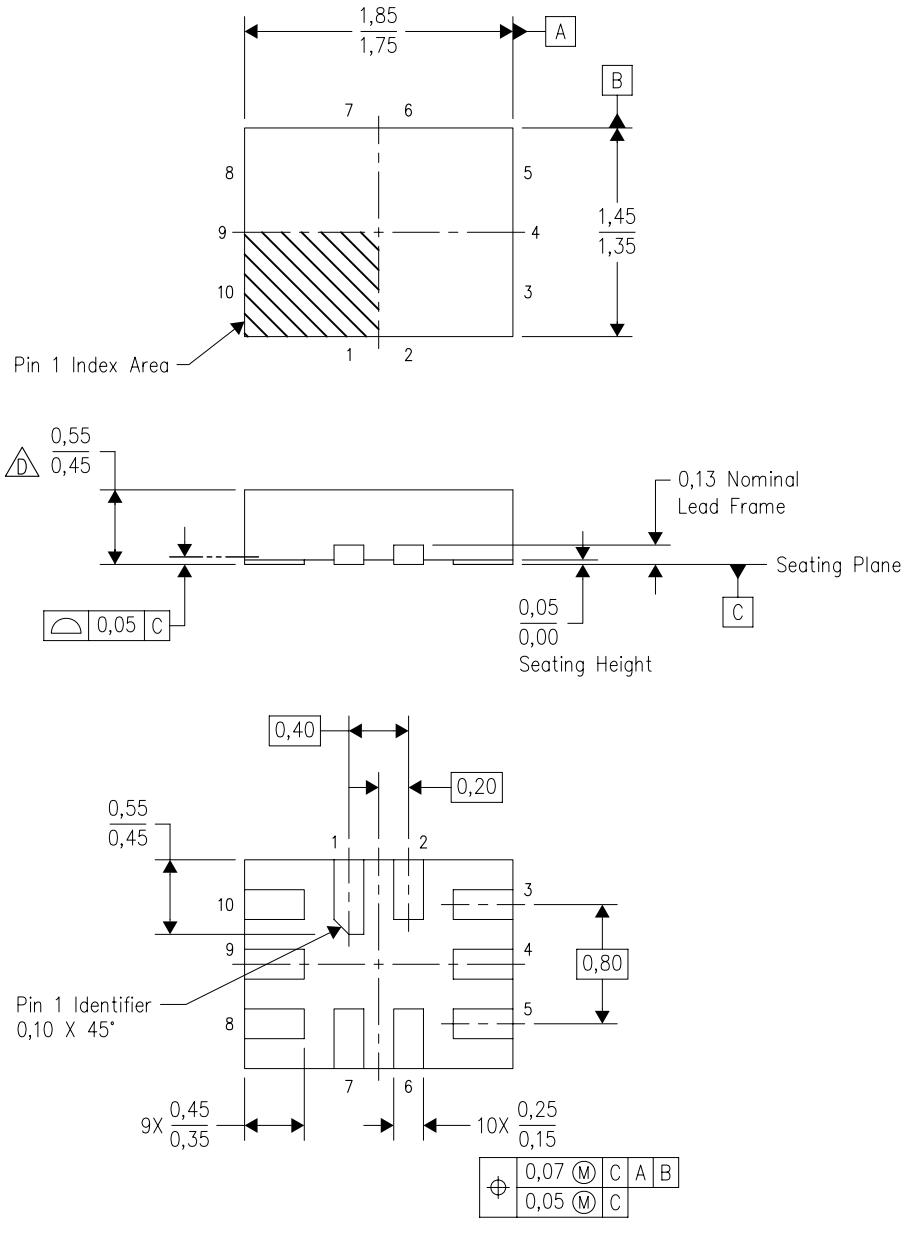
(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

RSW (R–PUQFN–N10) PLASTIC QUAD FLATPACK NO–LEAD

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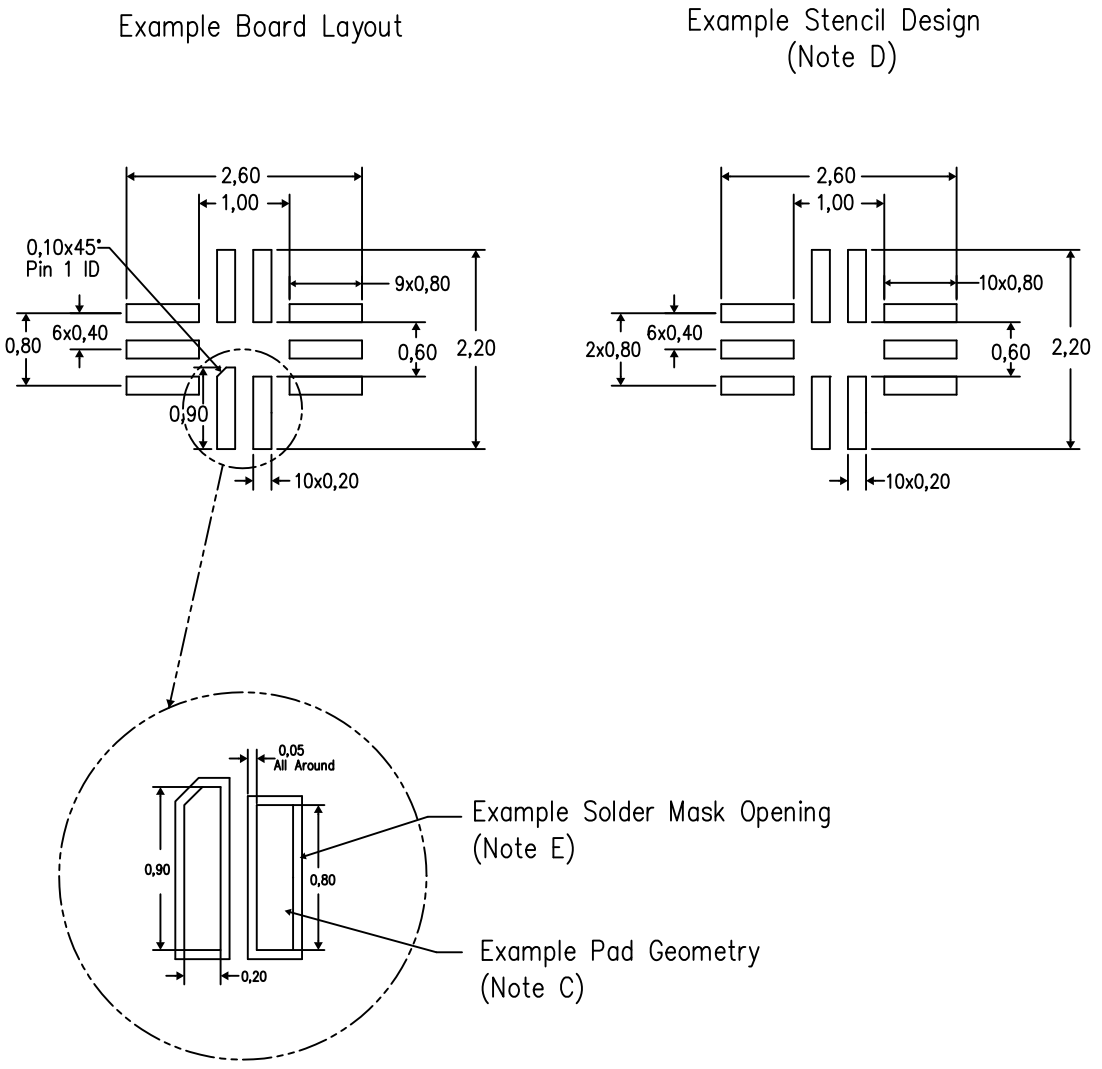
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–lead) package configuration.
D. This package complies to JEDEC MO–288 variation UDEE, except minimum package height.

RSW (R–PUQFN–N10) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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