SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

TS5070/5071 COMBO II PROGRAMMING AND HYBRID BALANCING WITH SOLID-STATE SLICs

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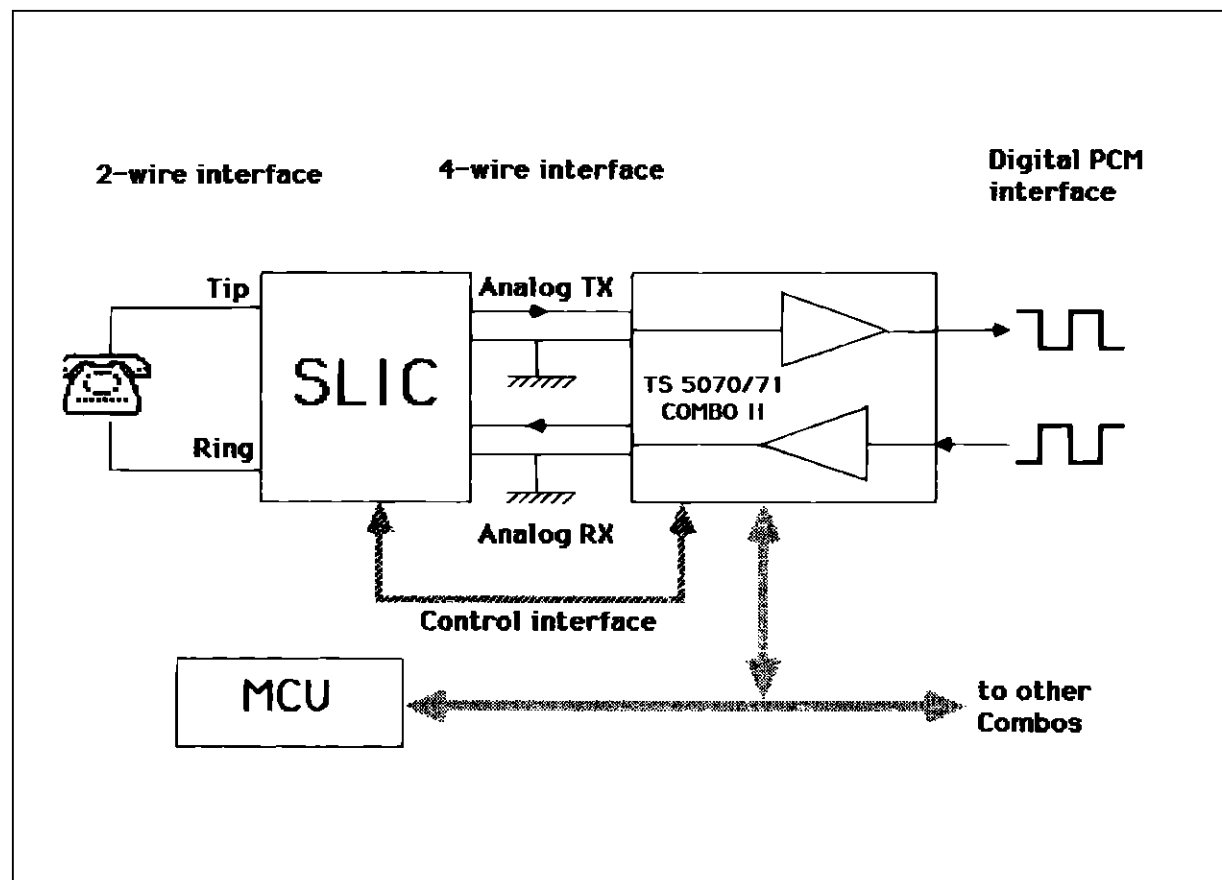
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1. INTRODUCTION

The TS5070/71 COMBO II is a programmable Codec/Filter circuit especially developped for the subscriber line card applications in a central office or PABX.

Compared to the currently used first generation cofidecs, such as : ETC 5054/57, M5913/14, ... the TS5070/71 COMBO II provides two major enhancements :

1) Several functions, previously assumed by external components, are now "on-chip" with the TS5070/71 COMBO II. Such features include :

- Gain adjustable transmit and receive amplifiers (25.4dB range).
- Time-slot assignment (one out of 64).
- PCM port assignment (2 transmit and receive ports, on the TS5070).
- Analog and digital loopback, for test mode.
- Hybrid balance cancellation filter.

2) All these added functions are programmed by the card-controller, through a 4-wire serial bus. Other programmable features include :

- A-law or μ-law selection.
- European (2.048 or 4.096MHz) or North American master clock (1.536 or 1.544MHz).
- 6 input/output interface latches (5 on the TS5071). These latches facilitate the logical interface with a transformer or an electronic parallel control SLIC, such as L3000N+L3092 kit or L303X monochip SLIC or any other function.

The programmable features of the TS5070/71 COMBO II simplify the design of the line card and provide more flexibility, especially when the same module must operate in different countries and must deal with the various telecom administrations requirements : only a few external components must be changed in the SLIC and the major adaptations are assumed by the TS5070/71 COMBO II programming.

As an example, this note describes briefly the design of a line card module, using a TS5070/71 COMBO II with a transformer SLIC and the solid state SLICs from SGS-THOMSON Microelectronics L3000N/L3092 kit and the L303X monochip SLIC. The adaptation of the line card kit to several telecom administrations requirements is also discussed..

The TS5071 basic version of the COMBO II is packaged in a 20-pin DIL case. The TS5070 is a full feature version available in a 28-pin PLCC or 28-pin DIP package :

- Interface latch pin IL5 is bonded out : 6 input/output latches are available.

- Programmable ports : DX1, DR1, and TSX1 are bonded out : 2 PCM port are available.
- Serial interface : CI and CO are separated.
- Clock inputs : BCLK and MCLK are not bonded together, providing two separate clock inputs.

2. SCHEMATIC DIAGRAM

TRANSFORMER SLIC

The design of the transformer is greatly simplified, due to the on-chip hybrid balance cancellation filter : Only one single secondary winding is required (see fig. 1). ZT is the line termination impedance as reflected through the transformer (impedance measured between Tip and Ring) : its value is determined by the administration requirements and the transformer characteristics.

ZT provides an echo : a part of the receive signal on VFRO is injected into the transmit path VFXI. The internal hybrid balance filter is designed in order to replicate the echo path, and thus to cancel it.

In this application, the input/output latches are used as relay drivers (buffered through an external transistor) : ring relay, test relays... and line monitoring : off-hook detection, ground key detection. Thus, the card controller can monitor the whole line card module through the unique control port of the TS5070/71 COMBO II.

When the CS pin is held high by the card controller (chip disabled), the CO output of the TS5070 is placed in a high impedance state, allowing several TS5070/71 COMBO II to share the same data link.

SGS-THOMSON MICROELECTRONICS SLIC AND THE TS5070/71 COMBO II : A KIT APPROACH

SGS-THOMSON Microelectronics provides now solid-state monolithic SLICs. These chips associated with the TS5070/71 COMBO II and the especially designed protection components, feature all the BORSCH functions (i.e. Battery feeding, Overvoltage protection, Ringing injection, Supervision of the loop, Codec/Filter and Hybrid 2-wire to 4-wire conversion). The versatility of these kits allows an easy adaptation for the different Telecom Administrations requirements throughout the world.

The schematic diagrams are detailed in fig. 2 and 3. The SGS-THOMSON SLICS parallel control interface allows the use of the IL interface latches of the TS5070/71 COMBO II (see fig. 2 and 3).

The ZAC impedance synthesizes the output impedance of the SLIC on Tip & Ring ; hence, this network should be designed differently for each country. The

structure of this network is a copy of the line imped-ance ; please, refer to the relevant SLIC data-sheet for more details. The "balancing" network, ZA and ZB is used by the SLIC to balance the 2-wire/4-wire conversion. When using the TS5070/71 COMBO II, this balancing network is no more necessary (ZB pin to GND) being the hybrid balancing performed by the "Hybal" filter of the Combo.

3. PROGRAMMING THE TS5070/71 COMBO II

The control information of the TS5070/71 COMBO II require 2 bytes of informations, with the exception of a single-byte power-up/down command.

When CS is pulled low a first "instruction" byte is shifted into the TS5070 COMBO II, at pin CI (or CI/O for the TS5071) on the falling edge of each CCLK clock pulse, the most significant bit first. During the 8th (dummy) bit, the content of this instruction is de-coded by the Combo and, depending wether a "read" or a "write" instruction is performed, a second "data" byte is shifted into or shifted out from the Combo.

* Bit #1 is the single-byte control bit : when 0, this is a single-byte power-up/down instruction, no data byte is expected.

* Bit #2 is the read/write control bit : when 0, the data byte will be written by the card controller into the Combo. When 1, the data byte will be read by the card controller from the Combo.

* Bit #3, 4, 5, 6 specify which one of the 10 registers of the TS5070/71 COMBO II is to be accessed.

* Bit #7 is the power control bit : when 0, the Combo is placed in power-up state ; when 1, the Combo is placed in power-down. Note that the power state can be set in any instruction.

* Bit #0, the last bit, is a dummy bit to allow for de-coding of the 7 previously entered bits. Its value is not taken into account and has no influence on the TS5070/71 COMBO II operation.

When writing to the TS5070/71 COMBO II, the data byte may follow the instruction byte immediately, or CS may be pulled high between the 2 bytes. The data byte is shifted into the Combo in the same way as the instruction byte : MSB first, on the falling edge of each CCLK clock pulse.

When reading from the TS5070 COMBO II, the data byte is shifted out, onto the CO pin (CI/O pin for the TS5071), MSB first, on the rising edge of each CCLK clock pulse. As for the write operation, CS can be pulled high between the instruction and the data byte.

After a read or a write operation is completed, it is recommended, although this is not mandatory, that the CS pin should be put high to reset the control port logic.

The content of the instruction byte is detailed in table 1 :

Table 1 : Instruction Byte.

Bit #	7	6	5	4	3	2	1	0
Single Byte Power-up/down	P	X	X	X	X	X	0	X
Control Register	P	0	0	0	0	W	1	X
Latch Direction Register	P	0	0	1	0	W	1	X
Interface Latch Register	P	0	0	0	1	W	1	X
Receive Time-slot/port	P	1	0	0	1	W	1	X
Transmit Time-slot/port	P	1	0	1	0	W	1	X
Receive Gain Register	P	0	1	0	0	W	1	X
Transmit Gain Register	P	0	1	0	1	W	1	X
Hybrid Balance Register # 1	P	0	1	1	0	W	1	X
Hybrid Balance Register # 2	P	0	1	1	1	W	1	X
Hybrid Balance Register # 3	P	1	0	0	0	W	1	X

P = Power control bit : "0" = Power-up, "1" Power-down
W = Read/Write control bit : "0" = Write, "1" = Read
X = don't care (0 or 1)

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DATA BYTE : CONTROL REGISTER

The content of the control register is detailed in table 2 :

Table 2 : Control Register.

Bit Number								Function
7	6	5	4	3	2	1	0	
0	0							MCLK = 512KHz
0	1							MCLK = 1.536 or 1.544MHz
1	0							MCLK = 2.048MHz*
0	1							MCLK = 4.096MHz
		0	X					µ-255 Law*
		1	0					A-law, with Even Bit Inversion
		1	1					A-law, no Even Bit Inversion
				0				Delayed Data Timing
				1				Non-delayed Data Timing*
					0	0		Normal Operation*
					1	X		Digital Loopback
					0	1		Analog Loopback
							0	Power Amp Enabled in PDN
							1	Power Amp Disabled in PDN*

* = State at power-on initialization.

The * specifies the default value of the control register at the power-on initialization.

MCLK : Master clock used by the Combo's filters, encoder and decoder. It is necessary to indicate which frequency is beeing applied to the Combo, for a correct filter operation.

COMPANDING LAW : the µ-255 compressing and expanding law is used in USA & Japan, A-law in Europe. Usually, in A-law, even bits are inverted : 0000 0000 becomes : 0101 0101 ; if this even bit inversion is performed in another part of the switching system, a "No even bit inversion" is available.

DATA TIMING : In Non-delayed Data Timing mode, the time-slot always begin with the rising-edge of FSX or FSR ; Time-slot Assignment is not available in this mode.
In Delayed Data Timing mode, time-slot begins after a falling edge of BCLK, when FSX or FSR is set high ; the Time-slot Assignment feature of COMBO II can be used in this mode only.

Note that PCM port selection is available in both timing modes.

LOOPBACK : Test modes : In Analog Loopback, VFXI is isolated from input pin and internally connected to the VFRO output, providing a complete D to D test loop.

In Digital Loopback, the PCM byte written into the Receive register, can be read back in any Transmit Time-slot at DX0 (or DX1) pin.

POWER AMP : if "1", the power amplifier, at VFRO output is disabled during the power-down state, i.e. VFRO pin is high impedance state.

It is very easy to set the TS5070/71 COMBO II configuration in any "U.S." or "European" environment.

In the following example, the line card module must be adapted to an european telecom administration specifications ; should be selected :

- Master clock = 2.048MHz
- A-law with even bit inversion
- Delayed data timing (which allows the Time-slot assignment feature)
- Normal operation (no loop back)
- Power amp disabled in power-down

Consequently, the instruction byte 10000010 (82 hexadecimal), followed by the data byte "10100001" (A1 hexadecimal) should be written into the COMBO II.

DATA BYTE : LATCH DIRECTION REGISTER

Bit Number							
7	6	5	4	3	2	1	0
L0	L1	L2	L3	L4	L5	X	X

* The bits #7 to #2 specify the function of each interface latch pin ; bit #0 and bit #1 are dummy bits.
* If Ln = 0 then ILn is a high-impedance input.
* If Ln = 1 then ILn is an output.
Notes : - unused pins should be programmed as outputs.
  - When using the TS5071 the IL5 pin should be programmed as an output.

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In the case of a L3092 SLIC, as described in fig. 3, IL0 pin, IL1 and IL4 are connected to L3092 inputs : they must be programmed as outputs. IL2 and IL3 must be set as inputs, because they are connected to L3092 outputs and IL5 is not used : this pin should be set as output.

In this example a "11001100" (CC hexadecimal) code should be written into the Latch Direction Register.

DATA BYTE : INTERFACE LATCH REGISTER

Bit Number							
7	6	5	4	3	2	1	0
D0	D1	D2	D3	D4	D5	X	X

X = Don't Care.

DATA BYTE : RECEIVE TIME-SLOT REGISTER AND TRANSMIT TIME-SLOT REGISTER

Bit Number and Name								
7	6	5	4	3	2	1	0	
EN	PS	T5	T4	T3	T2	T1	T0	
0	1	X	X	X	X	X	X	Disable DX Outputs (in TX reg.) Disable DR Inputs (in RX reg.)
1	0	Time-slot (0-63)						Enable DX0 Output, Disable DX1 (in TX reg.) Enable DR0 Input, Disable DR1 (in RX reg.)
1	1	Time-slot (0-63)						Enable DX1 Output, Disable DX0 (in TX reg.) Enable DR1 Input, Disable DR0 (in TX reg.)

* The 6 bits T5-T0 assign one time-slot from 0 to 63 (111111 in binary) ; available in Delayed Data Timing only.

* The PS "Port Selection" bit #6 selects the DR0 input, when 0, or the DR1 input, when 1, in the Receive Time-slot register, and, respectively DX0 or DX1 output in the Transmit Time-slot register.

Note : On the TS5071 the DR1 and DX1 pins are not bonded out : the PS bit must always be set to 0.

* The EN bit enables (when 1) the PCM input or output selected by the PS bit or disables them (when 0).

Note : the disabled pins are in a high impedance state.

In the above example, "Delayed Data Timing" was selected in the Control Register : when using the DX0/DR0 PCM port, time-slot #5 for transmission and time-slot #27 for reception, the contents of the TX time-slot and RX time-slot registers must be : "10000101" (85 hexadecimal) and "10011011" (9B hexadecimal).

* When writing to this register, the IL pins programmed as outputs assume the state of the corresponding bit Dn, in data byte.

* When reading from this register : for the IL pins programmed as outputs, the Dn bits correspond to the data previously written in this register ; for the IL pins programmed as inputs, the Dn bits correspond to the data read by these input pins.

In the case of the L3092 (fig. 3), if the SLIC must be put in "stand-by" mode, i.e. PWON and RNG pins = 0 and NCS = 1, "00001000" (08 hexadecimal) should be written into the Interface Latch Register. Note that bit #5 and bit #4 have no effect, since the IL2 and IL3 pins are programmed as input.

DATA BYTE : TRANSMIT GAIN AND RECEIVE GAIN REGISTER

The TS5070/71 COMBO II includes a transmit and a receive programmable amplifier ; these amplifiers allow an easy setting of the transmission level point (0TLP = 0dBm0) of the COMBO II, within the specified limits. The following formulas give the 2 bytes to be programmed in the TX and the RX gain registers :

$200 \times \log10 \ (V_{VFXI} / \sqrt{0.6}) + 191$, for the TX Gain Register, converted in binary.

$200 \times \log10 \ (V_{VFRO} / \sqrt{0.6}) + 174$, for the RX Gain Register, converted in binary.

V is the desired analog voltage, at VFXI pin for TX gain and VFRO pin for RX gain, expressed in Vrms, and corresponding to a digital 0dBm0 PCM level, as defined in CCITT G.711 ; the transmit input signal at VFXI must be in the range of 0.087 to 1.619Vrms, and the output receive amplifier at VFRO provides a signal from 0.106 to 1.96Vrms (for a 0dBm0 PCM signal).

The TX and RX gains can be also calculated from
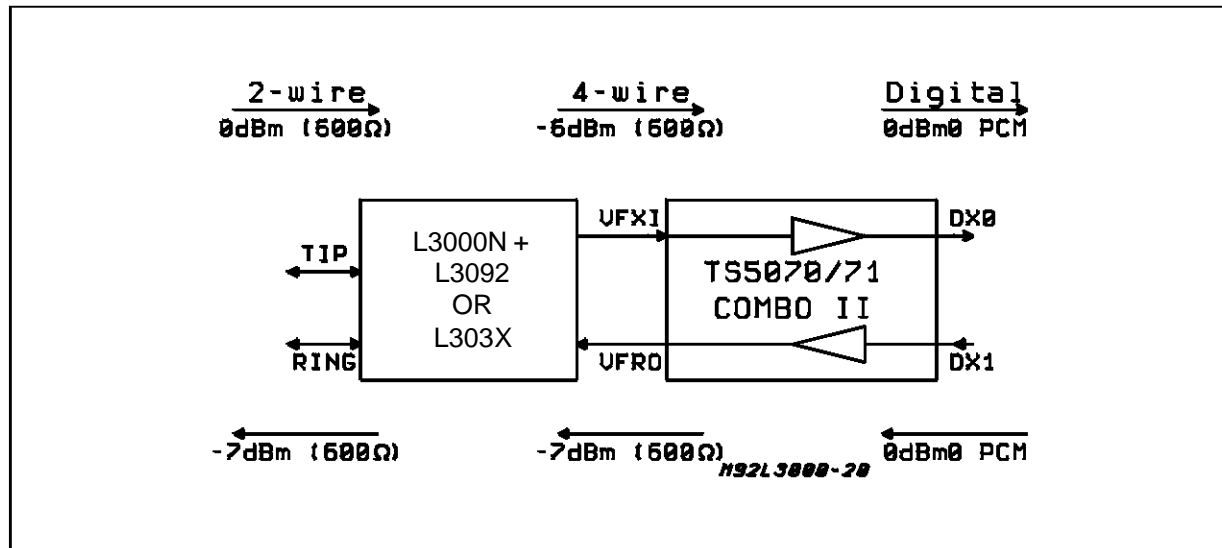
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the desired analog levels at VFXI and VFRO expressed in dBm into 600Ω ; in this case, the bytes to be programmed are calculated as follows :

10 X (VFXI level in dBm 600Ω) + 191, for the TX Gain Register, converted in binary.

10 X (VFRO level in dBm 600Ω) + 174, for the RX Gain Register, converted in binary.

Refer to the following example (fig. 4) :

Figure 4 : Example of TX and RX Levels.

- the transmit signal is 0dBm (600Ω) on Tip-Ring wires for a 0dBm0 PCM level at the DX0 output.
- the receive signal is - 7dBm (600Ω) on Tip-Ring wires for a 0dBm0 PCM level at the DR0 input.

The 0dBm0 PCM level is the bit sequence defined in the CCITT recommendation G.711.

We must first determine the analog levels at VFXI input and VFRO output of the TS5070/71 COMBO II. Due to their "feedback loop" structure, the SGS-THOMSON SLICs considered have a 0dB gain, in RX direction and –6dB in TX direction. This particular TX gain has been chosen in order to optimize hybal COMBO II filter dynamic range. Consequently the analog level at VFXI input will be : –6dBm (600Ω) = 0.3873Vrms, and the output level at VFRO : – 7dBm(600Ω) = 0.346Vrms.

The TX gain to be programmed in the TS5070/71 COMBO II will be :

10 X (–6dBm) + 131 = 83 hexa = 10000011 binary

this byte must be written in the TX gain register.

The RX gain will be :

10 X (- 7dBm) + 174 = 174 - 70 = 104 = 68 hexa = 01101000 binary

this byte must be written into the RX gain register.

These programmable gains provide more flexibility for the design of the line-card : if the transmit signal is - 8dBm instead of –6dBm, it is easy to re-program the TX gain register :

10 X (- 8dBm) + 191 = 191 - 80 = 111 = 6F hexa = 01101111 binary

In this case, TX gain must be set to 111 decimal = 6F hexadecimal = 01101111 binary. It is easy to adapt this example to any particular configuration. The designers shall notice that the gains are adjusted in 0.1dB steps. Consequently, the gain for - 8dBm will be 20 steps below the gain for –6dBm, i.e. 131 - 20 = 111.

Note that if the analog output level, at VFRO, exceeds 1.7Vrms, for a 0dBm0 PCM input at DR0, there are some restrictions on the value of the load connected at VFRO :
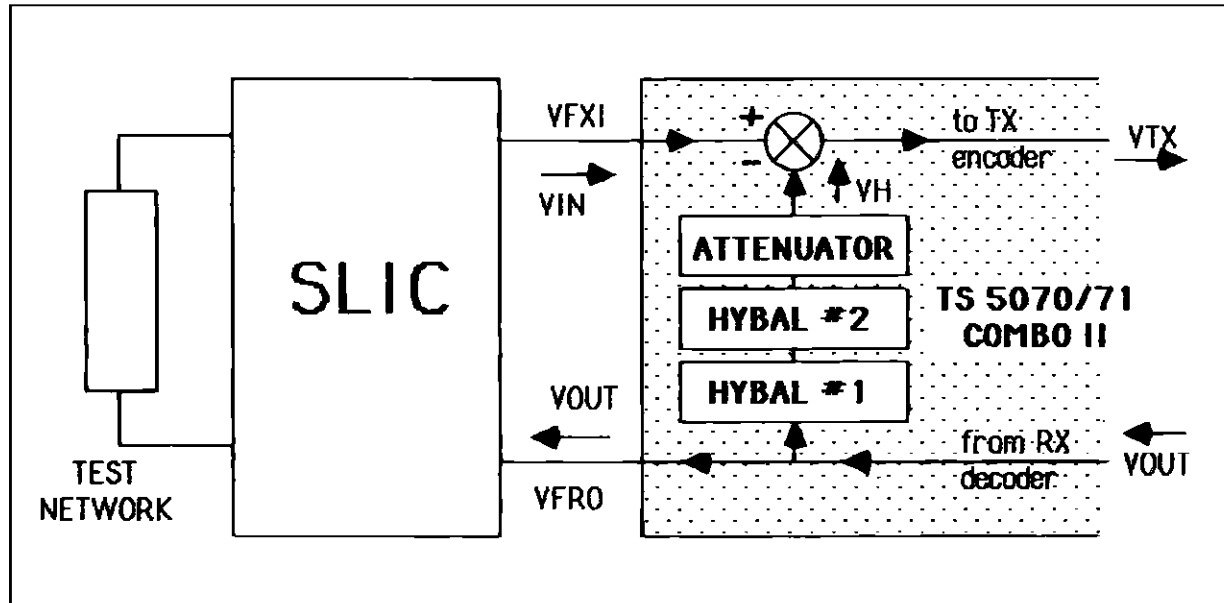
- if the level is less than 1.7Vrms, the load impedance must be greater than 300Ω
- if the level is between 1.7Vrms and 1.9Vrms, the load impedance must be greater than 600Ω
- if the level is between 1.9Vrms and 1.96Vrms, the load impedance must be greater than 15KΩ

4. HYBRID BALANCING

The hybrid balance filter of the TS5070/71 COMBO II is entirely programmable : the "zero" and "pole" combinations for the low frequency Hybal filter #1

and the high frequency Hybal filter #2 can be set by the card controller ; in addition, a programmable attenuator adjust the amplitude of the cancellation signal (see fig. 5).

Figure 5 : Hybrid Balance Cancellation Filter.

The Hybrid Balance Filter is set by the contents of 3 registers ; an optimization software (TS5077) determines the 3 bytes to be written in these registers.

ECHO PATH OF THE SLIC

The first step for the calculation of the Hybrid Balance Filter is the echo path of the SLIC : VIN/VOUT (see fig. 5). The amplitude and the phase of the echo signal must be determined for 14 frequencies, from 200 to 3500Hz. A "Hybrid Balance" test network must be connected between Tip and Ring wires.

The echo path can be measured or calculated by simulation of the transfer function of the SLIC. The TS5077 optimization software includes a simulation module for a transformer SLIC.

OPTIMIZATION SOFTWARE

The echo path must be entered into the program, for

each balancing network, then the optimization routine is run. This routine tests all the combinations of the Hybrid Balance Filter and selects the one which is the closest to the echo path, and then provides the three bytes to be programmed into the three Hybrid Balance registers. Some optimization examples with the different SLIC kits from SGS-THOMSON Microelectronics are described in the Application Note "SGS-THOMSON SLIC KITS and COMBO II".

5. CONCLUSION

These examples show the great flexibility of the TS5070/71 COMBO II in its adaptation with different line-cards, different SLICs and different countries. This flexibility, coupled with the programmable features, enhance the integration of the line-card : more subscribers per board, more reliability, easier adaptation, ... and, last but not least : a significant reduction of the total cost of the line card.

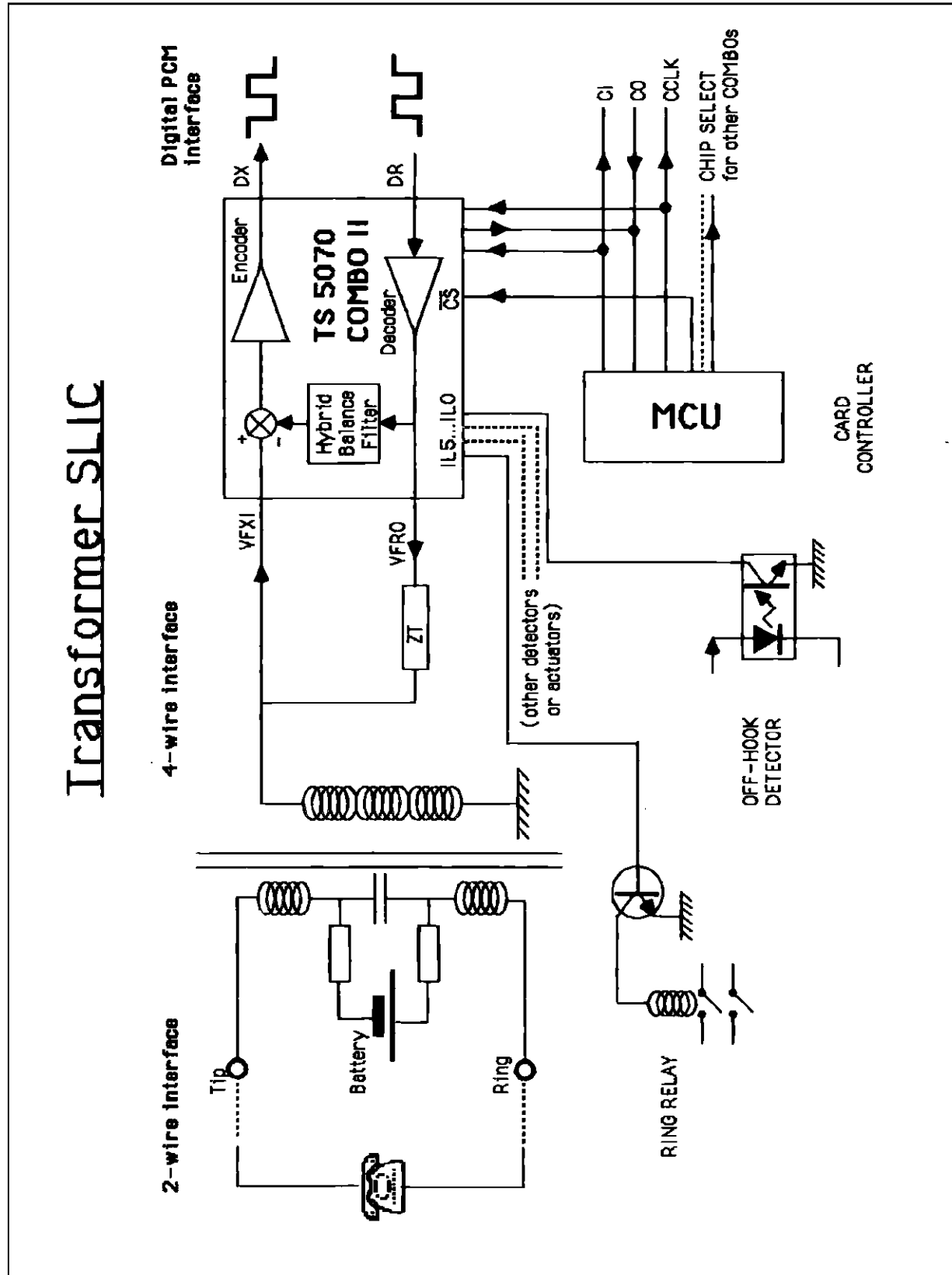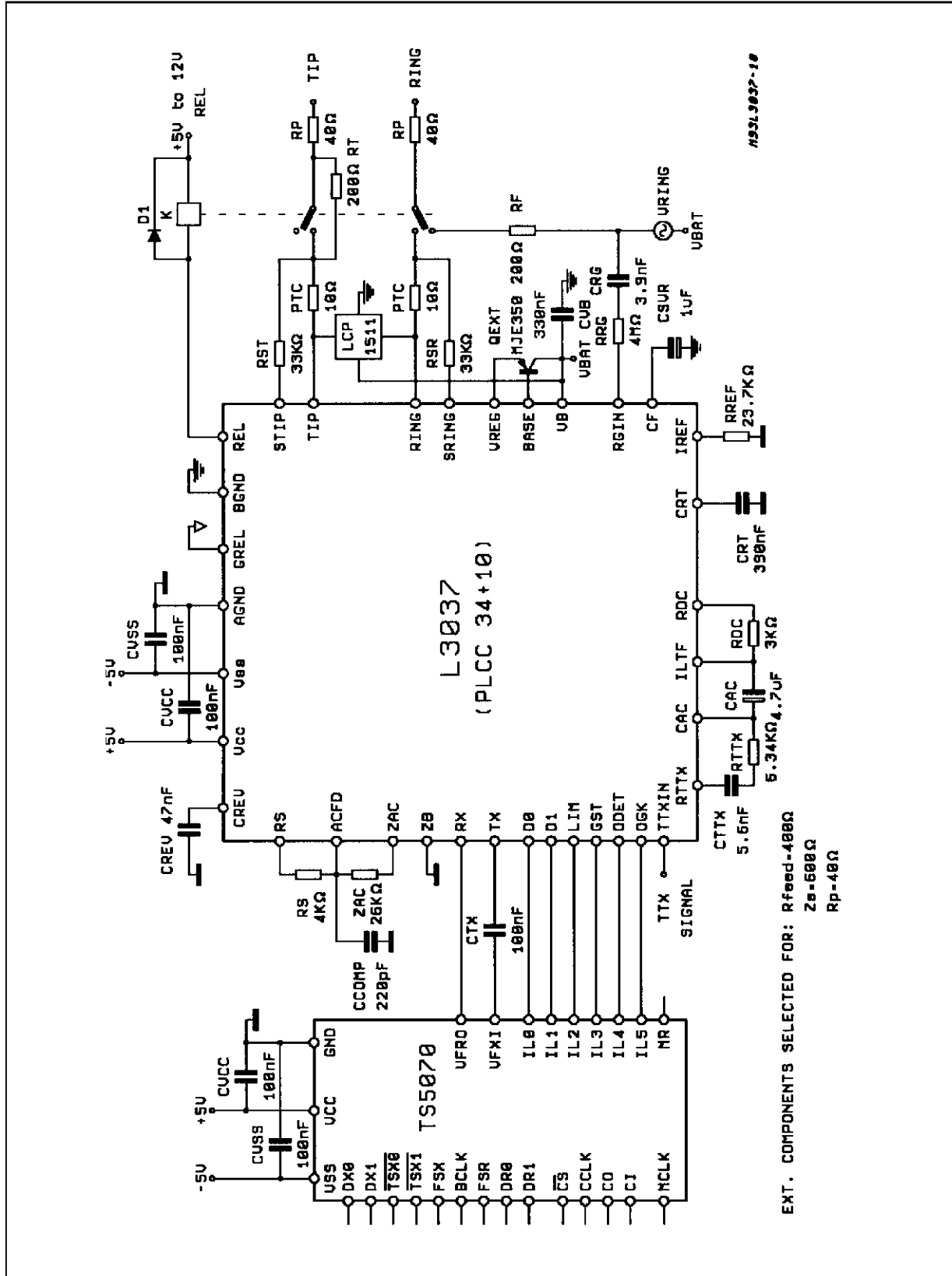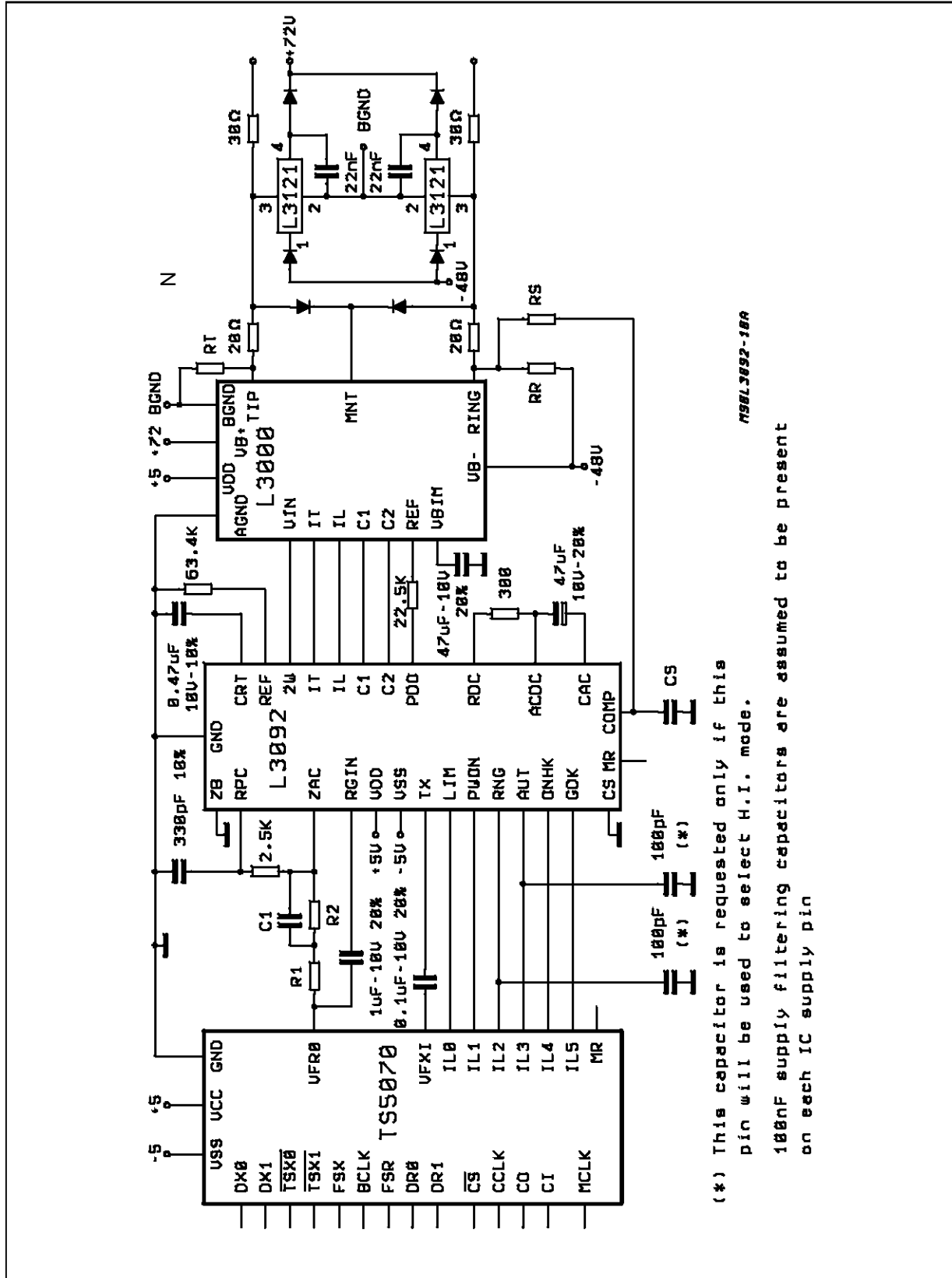**Figure 1 :** Interface with Transformer SLIC.

Figure 2 : Interface with L3037 Monochip SLIC.

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Figure 3 : Interface with L3000N + L3092 Solid-state SLIC.