MAIN FEATURES

- 8-bit resolution.
- 500 Msps (min) sampling rate.
- 1.3 GHz full power input bandwidth.
- Band Flatness: **TBD**
- Input VSWR (packaged device): **TBD**
- SINAD = 45 dB (7.2 Effective Bits), SFDR = 54 dBc
  @ F_S = 500 Msps, F_{IN} = 20 MHz :
- SINAD = 43 dB (7.1 Effective Bits), SFDR = 53 dBc
  @ F_S = 500 Msps, F_{IN} = 250 MHz :
- SINAD = 42 dB (7.0 Effective Bits), SFDR = 52 dBc
  @ F_S = 500 Msps, F_{IN} = 500 MHz (-3 dB FS)
- 2-tone IMD : **TBD** (199.5 MHz, 200.5 MHz) @ 500 MSPS.
- DNL = ± 0.3 LSB   INL = ± 0.7 LSB.
- Low Bit Error Rate (10^{-13}) @ 500 Msps, Tj = 90°C
- Power consumption : 3.8 W @ Tj = 70°C Typical
- 500 mVpp differential or single-ended analog inputs.
- Differential or single-ended 50Ω ECL compatible clock inputs.
- ECL or LVDS/HSTL output compatibility.
- ADC gain adjust.
- Data ready output with asynchronous reset.
- Gray or Binary selectable output data ; NRZ output mode.

APPLICATIONS

- Digital Sampling Oscilloscopes.
- Satellite receiver.
- Electronic countermeasures / Electronic warfare.
- Direct RF down–conversion.

SCREENING

- Atmel-Grenoble standard screening level
- Temperature range: up to 0°C < Tc ; Tj < +90°C

DESCRIPTION

The TS8308500 is a monolithic 8–bit analog–to–digital converter, designed for digitizing wide bandwidth analog signals at very high sampling rates of up to 500 Msps.

The TS8308500 is using an innovative architecture, including an on chip Sample and Hold (S/H), and is fabricated with an advanced high speed bipolar process. The on–chip S/H has a 1.3 GHz full power input bandwidth, providing excellent dynamic performance in undersampling applications (High IF digitizing).
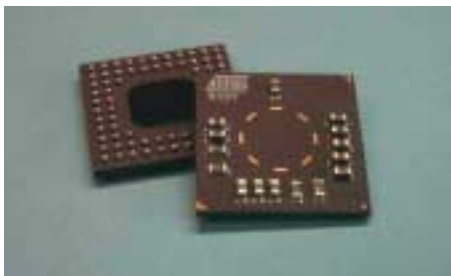
G Suffix : CBGA 72
Ceramic Ball Grid Array
With decoupling R and C on the package

ADC 8-bit 500 Msps

TS8308500

1/ Evaluation board :
TSEV8308500
Detailed specification on request.

2/ Demultiplexer : parallel 8-bit 2 Gsps
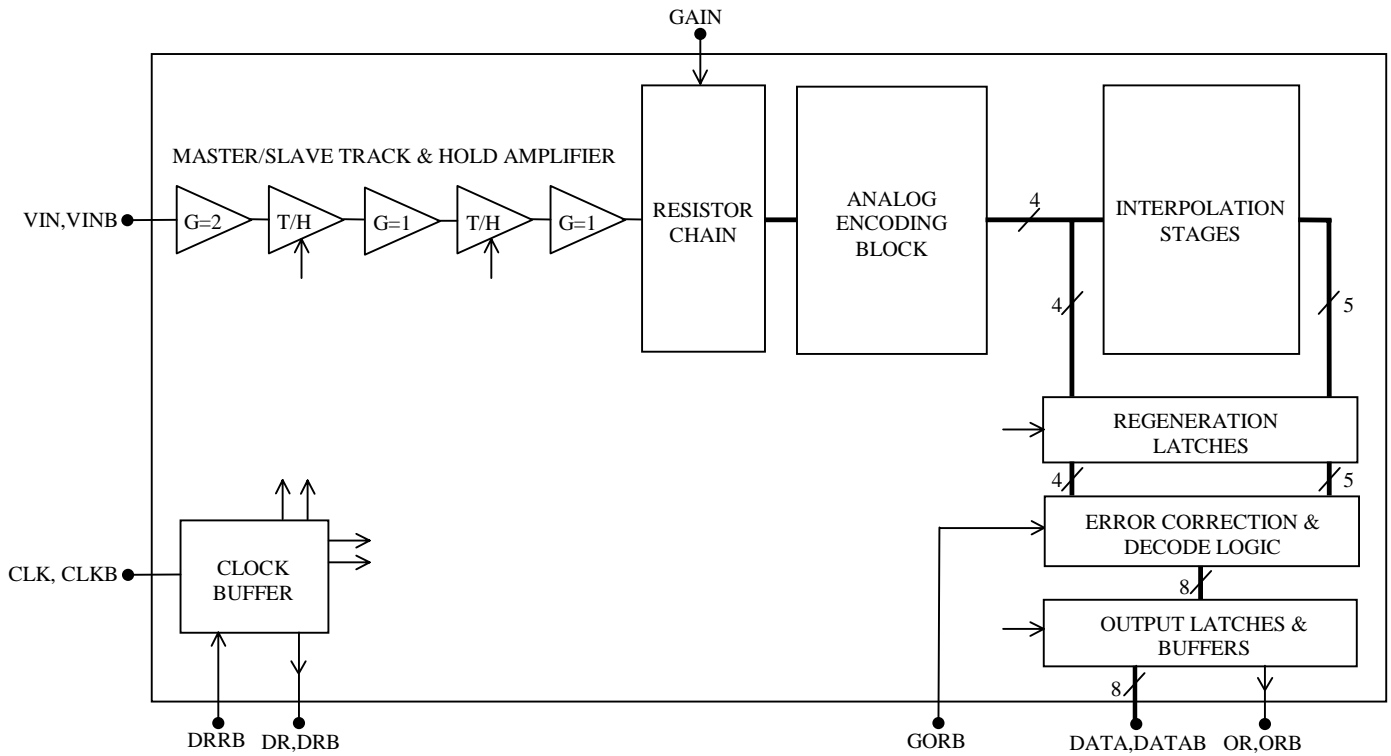TS81102G0 : companion device available

January 2002

Product Specification β-site

TABLE OF CONTENTS

1. SIMPLIFIED BLOCK DIAGRAM

2. FUNCTIONAL DESCRIPTION

The TS8308500 is an 8 bit 500MSPS ADC based on an advanced high speed bipolar technology featuring a cutoff frequency of 25 GHz.

The TS8308500 includes a front-end master/slave Track and Hold stage (S/H), followed by an analog encoding stage and interpolation circuitry.

Successive banks of latches are regenerating the analog residues into logical data before entering an error correction circuitry and a resynchronization stage followed by 75 Ω differential output buffers.

The TS8308500 works in fully differential mode from analog inputs up to digital outputs.

The TS8308500 features a full power input bandwidth of 1.3 GHz.

Control pin GORB is provided to select either Gray or Binary data output format.

Gain control pin is provided in order to adjust the ADC gain.

A Data Ready output asynchronous reset (DRRB) is available on TS8308500.

The TS8308500 uses only vertical isolated NPN transistors together with oxide isolated polysilicon resistors, which allow enhanced radiation tolerance (no performance drift measured at 150kRad total dose).

3. SPECIFICATIONS

3.1. ABSOLUTE MAXIMUM RATINGS (SEE NOTES BELOW)

Parameter	Symbol	Comments	Value	Unit
Positive supply voltage	V_{CC}		GND to 6	V
Digital negative supply voltage	DV_{EE}		GND to -5.7	V
Digital positive supply voltage	V_{PLUSD}		GND-0.3 to 2.8	V
Negative supply voltage	V_{EE}		GND to -6	V
Maximum difference between negative supply voltages	DV_{EE} to V_{EE}		0.3	V
Analog input voltages	V_{IN} or V_{INB}		-1 to +1	V
Maximum difference between V_{IN} and V_{INB}	V_{IN} - V_{INB}		-2 to +2	V
Digital input voltage	V_D	GORB	-0.3 to V_{CC} +0.3	V
Digital input voltage	V_D	DRRB	V_{EE} -0.3 to +0.9	V
Digital output voltage	Vo		V_{PLUSD}-3 to V_{PLUSD} -0.5	V
Clock input voltage	V_{CLK} or V_{CLKB}		-3 to +1.5	V
Maximum difference between V_{CLK} and V_{CLKB}	V_{CLK} - V_{CLKB}		-2 to +2	V
Maximum junction temperature	T_j		+135	^{o}C
Storage temperature	T_{stg}		-65 to +150	^{o}C
Lid temperature (soldering 10s)	T_{leads}	For dry pack (see chapter 4.5)	+300	^{o}C

Notes :   Absolute maximum ratings are limiting values (referenced to GND=0V), to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum rating may affect device reliability.
The use of a thermal heat sink is mandatory (see Thermal characteristics).

3.2. RECOMMENDED CONDITIONS OF USE

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
Positive supply voltage	V_{CC}		4.75	+5	5.25	V
Positive digital supply voltage	V_{PLUSD}	ECL output compatibility		GND		V
	V_{PLUSD}	LVDS output compatibility	+1.4	+2.4	+2.6	V
Negative supply voltages	$V_{EE, DVEE}$		-5.25	-5.0	-4.75	V
Differential analog input voltage (Full Scale)	V_{IN}, V_{INB}	50 Ω differential or single-ended	±113	±125	±137	mV
	V_{IN} -V_{INB}		450	500	550	mVpp
Clock input power level	P_{CLK} P_{CLKB}	50 Ω single–ended clock input	3	4	10	dBm
Operating temperature range	T_J	Commercial grade: "C"	0 < Tc ; Tj < 90			^{o}C

3.3. ELECTRICAL OPERATING CHARACTERISTICS

VEE = DVEE = -5 V ; V_{CC} = +5 V ; V_{IN} -V_{INB} = 500 mVpp Full Scale differential input ;
Digital outputs 75 or 50 Ω differentially terminated ;
Tj (typical) = 70°C.

Parameter		Symb	Test level	Min	Typ	Max	Unit
POWER REQUIREMENTS							
Positive supply voltage	Analog	VCC	1	4.5	5	5.5	V
	Digital (ECL)	V_{PLUSD}	4		0		V
	Digital (LVDS)	V_{PLUSD}	4	1.4	2.4	2.6	V
Positive supply current	Analog	ICC	1		420	445	mA
	Digital	I_{PLUSD}	1		130	145	mA
Negative supply voltage		VEE	1	-5.5	-5	-4.5	V
Negative supply current	Analog	AIEE	1		185	200	mA
	Digital	DIEE	1		160	180	mA
Nominal power dissipation		PD	1		3.8	4.1	W
Power supply rejection ratio	(note 2)	PSRR	4		0.5	2	mV/V
RESOLUTION						8	bits
ANALOG INPUTS							
Full Scale Input Voltage range (differential mode)		V_{IN}	4	-125		125	mV
(0 Volt common mode voltage)		V_{INB}		-125		125	mV
Full Scale Input Voltage range (single–ended input option)		V_{IN}	4	-250		250	mV
(see Application Notes)		V_{INB}			0		mV
Analog input capacitance		C_{IN}	4		3	3.5	pF
Input bias current		I_{IN}	4		10	20	µA
Input Resistance		R_{IN}	4	0.5	1		MΩ
Full Power input Bandwidth		FPBW	4	1.2	1.3		GHz
Small Signal input Bandwidth (10 % full scale)		SSBW	4	1.2	1.3		GHz
CLOCK INPUTS							
Logic compatibility for clock inputs (note 10) (see Application Notes)				ECL or specified clock input power level in dBm			
ECL Clock inputs voltages (V_{CLK} or V_{CLKB}) :			4				
• Logic "0" voltage		V_{IL}				-1.5	V
• Logic "1" voltage		V_{IH}		-1.1			V
• Logic "0" current		I_{IL}			5	50	µA
• Logic "1" current		I_{IH}			5	50	µA
Clock input power level into 50 Ω termination				DBm into 50 Ω			
Clock input power level			4	-2	4	10	dBm
Clock input capacitance		C_{CLK}	4		3	3.5	pF

Parameter	Symb	Test level	Min	Typ	Max	Unit
DIGITAL OUTPUTS *(notes 1,6)*						
Single ended or differential input mode, 50 % clock duty cycle (CLK,CLKB), Binary output data format, Tj (typical) = 70°C. Full temperature range : 0°C < Tc ; Tj < +90°C						
Logic compatibility for digital outputs (Depending on the value of V_{PLUSD}) *(see Application Notes)*				ECL or LVDS		
Differential output voltage swings (assuming V_{PLUSD} = 0V) :		4				
75 Ω open transmission lines (ECL levels)			1.50	1.620		V
75 Ω differentially terminated			0.70	0.825		V
50 Ω differentially terminated			0.54	0.660		V
Output levels (assuming V_{PLUSD} = 0V)		4				
75 Ω open transmission lines *(note 6)*						
• Logic "0" voltage	V_{OL}			-1.62	-1.54	V
• Logic "1" voltage	V_{OH}		-0.88	-0.8		V
Output levels (assuming V_{PLUSD} = 0V)		4				
75 Ω differentially terminated *(note 6)*						
• Logic "0" voltage	V_{OL}			-1.41	-1.34	V
• Logic "1" voltage	V_{OH}		-1.07	-1		V
Output levels (assuming V_{PLUSD} = 0V)						
50 Ω differentially terminated *(note 6)*						
• Logic "0" voltage	V_{OL}	1, 2		-1.40	-1.32	V
• Logic "1" voltage	V_{OH}	1, 2	-1.16	-1.10		V
Differential Output Swing	DOS	4	270	300		mV
Output level drift with temperature		4			1.6	mV/°C
DC ACCURACY						
Single ended or differential input mode, 50 % clock duty cycle (CLK,CLKB), Binary output data format, Tj (typical) = 70°C.						
Differential non linearity *(notes 2,3)*	DNL-	1	-0.6	-0.3		LSB
	DNL+	1		0.3	0.6	LSB
Integral non linearity *(notes 2,3)*	INL-	1	-1.0	-0.7		LSB
	INL+	1		0.7	1.0	LSB
No missing codes *(note 3)*			Guaranteed over specified temperature range			
Gain error		1, 2	-10	-2	10	% FS
Input offset voltage		1, 2	-26	-5	26	mV
Gain error drift		4	100	125	150	ppm/°C
Offset error drift		4	40	50	60	ppm/°C

Parameter		Symb	Test level	Min	Typ	Max	Unit
TRANSIENT PERFORMANCE							
Bit Error Rate *(notes 2, 4)* FS = 1 Gsps Fin = 62.5 MHz		BER	4			1E-12	Error/ sample
ADC settling time *(note 2)* V_{In} -V_{inB} = 400 mVpp		TS	4		0.5	1	ns
Overvoltage recovery time *(note 2)*		TOR	4		0.5	1	ns
AC PERFORMANCE (Expected values)							
Single ended or differential input and clock mode, 50 % clock duty cycle (CLK,CLKB), Binary output data format, Tj. = 70°C, unless otherwise specified.							
Signal to Noise and Distortion ratio *(note 2)*		SINAD					
FS = 500 Msps Fin = 20 MHz			4		44		dB
FS = 500 Msps Fin = 500 MHz (Tj = 90°C)			4	43	44	45	dB
FS = 500 Msps Fin = 1000 MHz (-1dB Fs)			4				dB
FS = 50 Msps Fin = 25 MHz			1	40	45		dB
Effective Number Of bits		ENOB					
FS = 500 Msps Fin = 20 MHz			4		7.2		Bits
FS =500 Msps Fin = 500 MHz (Tj = 90°C)			4	6.8	7.0	7.3	Bits
FS = 500 Msps Fin = 1000 MHz (-1dBFs)			4	6.4	6.6		Bits
FS = 50 Msps Fin = 25 MHz			1	7.0	7.2		Bits
Signal to Noise Ratio *(note 2)*		SNR					
FS = 500 Msps Fin = 20 MHz			4		45		dB
FS = 500 msps Fin = 500 MHz (Tj = 90°C)			4	44	45	46	dB
FS = 500 Msps Fin = 1000 MHz (-1dBFs)			4	40	41		dB
FS = 50 Msps Fin = 25 MHz			1	44	45		dB
Total Harmonic Distortion *(note 2)*		THD					
FS = 500 Msps Fin = 20 MHz			4		50		dB
FS = 500 Msps Fin = 500 MHz (Tj = 90°C)			4	48	49	53	dB
FS = 500 Msps Fin = 1000 MHz (-1dBFs)			4				dB
FS = 50 Msps Fin = 25 MHz			1	46	51		dB
Spurious Free Dynamic Range *(note 2)*		SFDR					
FS = 500 Msps Fin = 20 MHz			4		54		dBc
FS = 500 Msps Fin = 500 MHz (Tj = 90°C)			4	52	53	54	dBc
FS = 500 Msps Fin = 1000 MHz (-1dBFs)			4				dBc
FS = 500 Gsps Fin = 1000 MHz (-3dBFs)			4				dBc
FS = 50 Msps Fin = 25 MHz			1	48	55		dBc
Two-tone inter-modulation distortion *(note 2)* F_{IN1} = 199.5 MHz @ F_S = 500 Msps F_{IN2} = 200.5 MHz @ F_S = 500 Msps		IMD	4	TBD	TBD		dBc

Parameter		Symb	Test level	Min	Typ	Max	Unit
SWITCHING PERFORMANCE AND CHARACTERISTICS – *See Timing Diagrams Figure 1, Figure 2*							
Maximum clock frequency	*(Note 14)*	F_S		500		700	Msps
Minimum clock frequency	*(Note 15)*	F_S	4	10		50	Msps
Minimum Clock pulse width (high)		TC1	4	1710	2	50	ns
Minimum Clock pulse width (low)		TC2	4	1710	2	50	ns
Aperture delay	*(Note 2)*	TA	4	100	+250	400	ps
Aperture uncertainty	*(Notes 2, 5)*	Jitter	4		0.4	0.6	ps (rms)
Data output delay	*(Notes 2, 10, 11, 12)*	TOD	4	1150	1360	1660	ps
Output rise/fall time for DATA (20 % – 80 %) *(note 11)*		TR/TF	4	250	350	550	ps
Output rise/fall time for DATA READY (20 % – 80 %) *(note 11)*		TR/TF	4	250	350	550	ps
Data ready output delay	*(Notes 2,10, 11, 12)*	TDR	4	1110	1320	1620	ps
Data ready reset delay		TRDR	4		720	1000	ps
Data to data ready – clock low pulse width *(See timing diagram, notes 9, 13,14)*		TOD-TDR	4	0	40	80	ps
Data to data ready output delay (50% duty cycle) *(See timing diagram, notes 2, 15)* @ 500 Msps		TD1	4	920	960	1000	ps
Data pipeline delay		TPD	4		4		clock cycles

Note 1 : Differential output buffers are internally loaded by 75 Ω resistors. Buffer bias current = 11 mA.

Note 2 : See definition of terms

Note 3 : Histogram testing based on sampling of a 10 MHz sinewave at 50 MSPS.

Note 4 : Output error amplitude < ± 4 LSB around worst code.

Note 5 :   Maximum jitter value obtained for single–ended clock input on the JTS8308500 die (chip on board) : 200 fs.
  (500 fs expected on TS8308500)

Note 6 : Digital output back termination options depicted in Application Notes figures 3,4,5 .

Note 7 : With a typical value of TD = 465 ps, at 500 Msps, the timing safety margin for the data storing using the ECLinPS 10E452 output registers from Motorola is of ± 315 ps, equally shared before and after the rising edge of the Data Ready signals (DR, DRB).

Note 8 : The clock inputs may be indifferently entered in differential or single–ended, using ECL levels or 4 dBm typical power level into the 50 Ω termination resistor of the inphase clock input.
  (4 dBm into 50 Ω clock input correspond to 10 dBm power level for the clock generator.)

Note 9 : At 500 MSPS, 50/50 clock duty cycle, TC2 = 1 ns (TC1). TDR - TOD = -100 ps (typ) does not depend on the sampling rate.

Note 10 : Specified loading conditions for digital outputs :
  - 50 Ω or 75 Ω controlled impedance traces properly 50 / 75 Ω terminated, or unterminated 75 Ω controlled impedance traces.
  - Controlled impedance traces far end loaded by 1 standard ECLinPS register from Motorola.(e.g. : 10E452) (Typical input parasitic capacitance of 1.5 pF including package and ESD protections.)

Note 11 : Termination load parasitic capacitance derating values :
   - 50 Ω or 75 Ω controlled impedance traces properly 50 / 75 Ω terminated : 60 ps / pF or 75 ps per additional ECLinPS load.
   - Unterminated (source terminated) 75 Ω controlled impedance lines : 100 ps / pF or 150 ps per additional ECLinPS termination load.

Note 12 : apply proper 50 / 75 Ω impedance traces propagation time derating values : 6 ps / mm (155 ps/inch) for TSEV8308500 Evaluation Board.

Note 13 : Values for TOD and TDR track each other over temperature, (1 % variation for TOD - TDR per 100 ^{o}C temperature variation). Therefore TOD - TDR variation over temperature is negligible. Moreover, the internal (onchip) and package skews between each Data TODs and TDR effect can be considered as negligible. Consequently, minimum values for TOD and TDR are never more than 100 ps apart. The same is true for the TOD and TDR maximum values (see Advanced Application Notes about TOD - TDR variation over temperature in section 7).

Note 14 : Min value guarantees performance. Max value guarantees functionality.

Note 15 : Min value guarantees functionality. Max value guarantees performance.
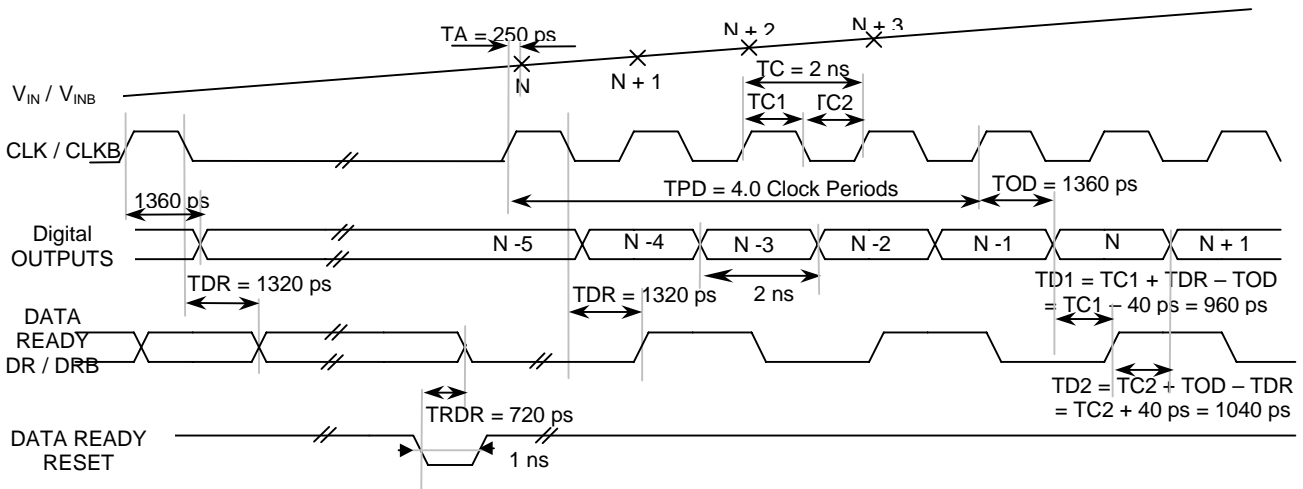
3.4. TIMING DIAGRAMS

Figure 1: TS8308500 TIMING DIAGRAM (500 MSPS CLOCK RATE)
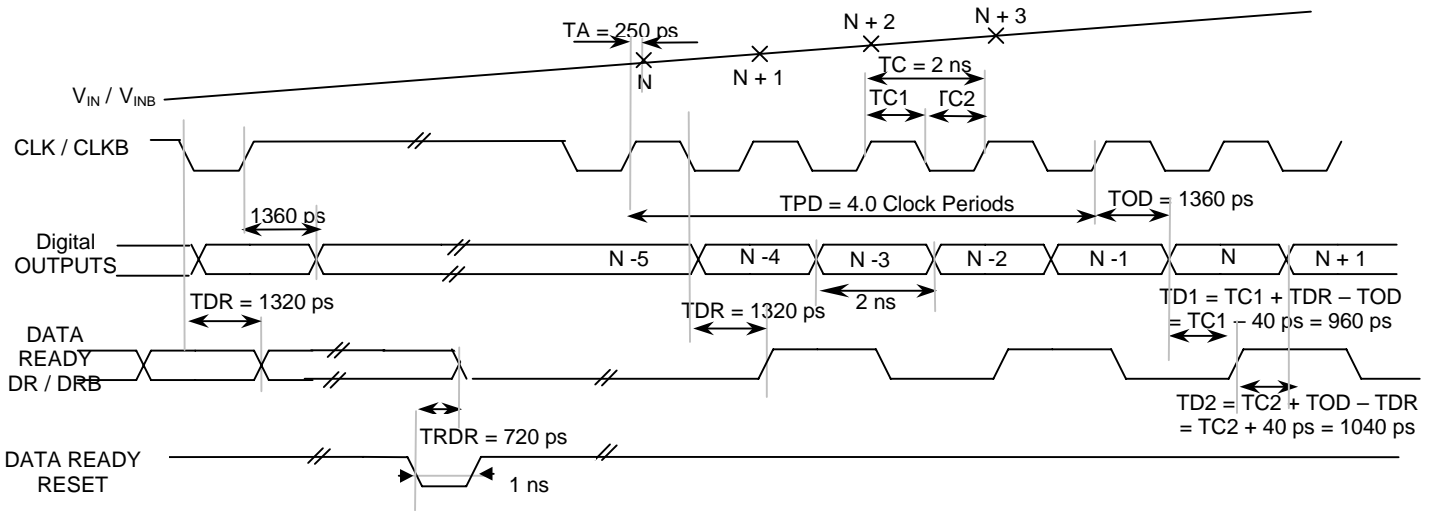Data Ready Reset, Clock Held at LOW Level

Figure 2: TS8308500 TIMING DIAGRAM (500 MSPS CLOCK RATE)
Data Ready Reset, Clock Held at HIGH Level
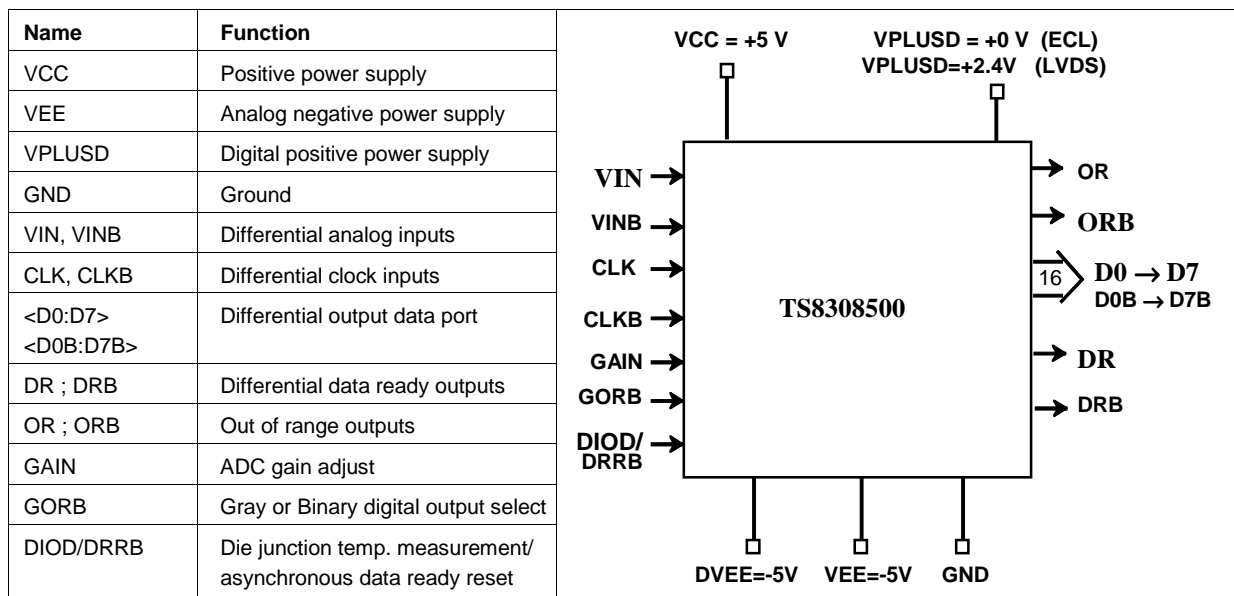
3.5. EXPLANATION OF TEST LEVELS

1	100% production tested at +25°C [1] (for "C" Temperature range [2]).
2	100 % production tested at +25°C [1], and sample tested at specified temperatures (for "V" and "M" Temperature ranges [2]).
3	Sample tested only at specified temperatures
4	Parameter is guaranteed by design and characterization testing (thermal steady-state conditions at specified temperature).
5	Parameter is a typical value only

Only MIN and MAX values are guaranteed (typical values are issuing from characterization results).

[1] *Unless otherwise specified, all tests are pulsed tests : therefore Tc = Ta where Tc and Ta are case and ambient temperature.*
[2] *Refer to ORDERING INFORMATION chapter.*

3.6. FUNCTIONS DESCRIPTION

Name	Function
VCC	Positive power supply
VEE	Analog negative power supply
VPLUSD	Digital positive power supply
GND	Ground
VIN, VINB	Differential analog inputs
CLK, CLKB	Differential clock inputs
<D0:D7> <D0B:D7B>	Differential output data port
DR ; DRB	Differential data ready outputs
OR ; ORB	Out of range outputs
GAIN	ADC gain adjust
GORB	Gray or Binary digital output select
DIOD/DRRB	Die junction temp. measurement/ asynchronous data ready reset

VCC = +5 V   VPLUSD = +0 V (ECL)   VPLUSD=+2.4V (LVDS)

VIN, VINB, CLK, CLKB, GAIN, GORB, DIOD/DRRB → TS8308500 → OR, ORB, 16 D0 → D7 / D0B → D7B, DR, DRB

DVEE=-5V   VEE=-5V   GND

3.7. DIGITAL OUTPUT CODING

NRZ (Non Return to Zero) mode, ideal coding : does not include gain, offset, and linearity voltage errors.

Differential analog input	Voltage level	Digital output		Out of Range
		Binary GORB = VCC or floating	Gray GORB = GND	
> +251 mV	> Positive full scale + 1/2 LSB	1 1 1 1 1 1 1 1	1 0 0 0 0 0 0 0	1
+251 mV +249 mV	Positive full scale + 1/2 LSB Positive full scale – 1/2 LSB	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0	1 0 0 0 0 0 0 0 1 0 0 0 0 0 0 1	0 0
+126 mV +124 mV	Positive 1/2 scale + 1/2 LSB Positive1/2 scale – 1/2 LSB	1 1 0 0 0 0 0 0 1 0 1 1 1 1 1 1	1 0 1 0 0 0 0 0 1 1 1 0 0 0 0 0	0 0
+1 mV -1 mV	Bipolar zero + 1/2 LSB Bipolar zero - 1/2 LSB	1 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1	1 1 0 0 0 0 0 0 0 1 0 0 0 0 0 0	0 0
-124 mV -126 mV	Negative 1/2 scale + 1/2 LSB Negative 1/2 scale - 1/2 LSB	0 1 0 0 0 0 0 0 0 0 1 1 1 1 1 1	0 1 1 0 0 0 0 0 0 0 1 0 0 0 0 0	0 0
-249 mV -251 mV	Negative full scale + 1/2 LSB Negative full scale - 1/2 LSB	0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0	0 0
< -251 mV	< Negative full scale - 1/2 LSB	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1

4. PACKAGE DESCRIPTION.

4.1. TS8308500 PAD DESCRIPTION

Pad number	Chip pad Name	Chip Pad Function
1	V$_{PLUSD}$	Positive digital supply (double pad) (note 2)
2	D5	In phase (+) digital output, bit 5 (D7 is the MSB ; Bit 7, D0 is the LSB ; Bit 0)
3	D5B	Inverted phase (-)digital output, bit 5
4	D4	In phase (+) digital output, bit 4
5	D4B	Inverted phase (-) digital output, bit 4
6	DV$_{EE}$	-5V digital supply (double pad)
7	DR	In phase (+) Data Ready
8	DRB	Inverted Phase (-) Data Ready
9	D3	In phase (+) digital output, bit 3
10	D3B	Inverted phase (-) digital output, bit 3
11	V$_{PLUSD}$	Positive digital supply (double pad) (note 2)
12	D2	In phase (+) digital output, bit 2
13	D2B	Inverted phase (-) digital output, bit 2
14	D1	In phase (+) digital output, bit 1
15	D1B	Inverted phase (-) digital output, bit 1
16	D0	In phase (+) digital output, bit 0, Least Significant Bit
17	D0B	Inverted phase (-) digital output, bit 0, Least Significant Bit
18	GORB	Gray or Binary data output format select. (Note 1)
19	V$_{CC}$	+5V supply (double pad)
20	GND	Analog Ground (double pad)
21	V$_{CC}$	+5V supply (double pad)
22	V$_{EE}$	-5V analog supply (double pad)
23	V$_{CC}$	+5V supply (double pad)
24	GND	Analog Ground (double pad)
25	CLK	In phase (+) clock input (double pad)
26	GND	Analog Ground
27	CLKB	Inverted phase (-) clock input (double pad)
28	GND	Analog Ground (double pad)
29	V$_{EE}$	-5V analog supply (double pad)
30	V$_{CC}$	+5V supply (double pad)
31	V$_{EE}$	-5V analog supply (double pad)
32	DIOD/DRRB	Diode input for Tj monitoring / Input for asynchronous Data Ready Reset
33	GND	Analog Ground
34	V$_{IN}$	In phase (+) analog input (double pad)
35	GND	Analog Ground
36	V$_{IN}$B	Inverted phase (-) analog input (double pad)
37	GND	Analog Ground (double pad)
38	GAIN	ADC gain adjust input
39	V$_{CC}$	+5V supply (double pad)
40	V$_{CC}$	+5V supply
41	OR	In phase (+) Out of Range digital output
42	ORB	Inverted phase (-) Out of Range digital output
43	D7	In phase (+) digital output, bit 7, Most Significant Bit
44	D7B	Inverted phase (-) digital output bit 7
45	D6	In phase (+) digital output, bit 6
46	D6B	Inverted phase (-) digital output, bit 6

Note 1: GORB tied to Vcc or floating : Binary output data format. GORB tied to GND : Gray output data format

Note2: The common mode level of the output buffers is 1.2V below the positive digital supply.
For ECL compatibility the positive digital supply must be set at 0V (ground).
For LVDS compatibility (output common mode at +1.2V) the positive digital supply must be set at 2.4V.
*If the subsequent LVDS circuitry can withstand a lower level for input common mode, it is recommended to lower the positive digital supply level in the name proportion in order to spare power dissipation.*

4.2.   TS8308500 PIN DESCRIPTION

Symbol	Pin number	Function
GND	A2, A5, B1, B5, B10, C2, C9, D2, E1, E2, E11, F1, F2, G11, J3, J9, K2, K3, K4, K5, K10, L2, L5	Ground pins. To be connected to external ground plane.
V_{CC}	A4, A6, B2, B4, B6, C3, H1, H2, L6, L7	+5 V positive supply.
V_{EE}	A3, B3, G1, G2, J1, J2	5 V analog negative supply
DV_{EE}	F10, F11	-5 V digital negative supply.
V_{IN}	L3	In phase (+) analog input signal of the sample and Hold differential preamplifier.
V_{INB}	L4	Inverted phase (-) of ECL clock input signal (CLK).
CLK	C1	In phase (+) ECL clock input signal. The analog input is sampled and held on the rising edge of the CLK signal.
CLKB	D1	Inverted phase (-) of ECL clock input signal (CLK).
B0, B1, B2, B3, B4, B5, B6, B7	A8, A9, A10, D10, H11, J11, K9, K8	In phase (+) digital outputs. B0 is the LSB. B7 is the MSB.
B0B, B1B, B2B, B3B, B4B, B5B, B6B, B7B	B7, B8, B9, C11, G10, H10, L10, L9	Inverted phase (-) Digital outputs. B0B is the inverted LSB. B7B is the inverted MSB.
OR	K7	In phase (+) Out of Range Bit. Out of Range is high on the leading edge of code 0 and code 256.
ORB	L8	Inverted phase (+) of Out of Range Bit (OR).
DR	E10	In phase (+) output of Data Ready Signal.
DRB	D11	Inverted phase (-) output of Data Ready Signal (DR).
GORB	A7	Gray or Binary select output format control pin. – Binary output format if GORB is floating or V_{CC}. – Gray output format if GORB is connected at ground (0 V).
GAIN	K6	ADC gain adjust pin. The gain pin is by default grounded, the ADC gain transfer fuction is nominally close to one.
DIOD/DRRB	K1	Die function temperature measurement pin and asynchronous data ready reset active low, single ended ECL input.
V_{PLUSD}	B11, C10, J10, K11	+ 2.4 V for LVDS output levels otherwise to GND [1]
NC	A1, A11, L1, L11	Not connected.

Note 1 :   *The common mode level of the output buffers is 1.2V below the positive digital supply.*
For ECL compatibility the positive digital supply must be set at 0V (ground).
For LVDS compatibility (output common mode at +1.2V) the positive digital supply must be set at 2.4V.
If the subsequent LVDS circuitry can withstand a lower level for input common mode, it is recommended to lower the positive digital supply level in the same proportion in order to spare power dissipation.
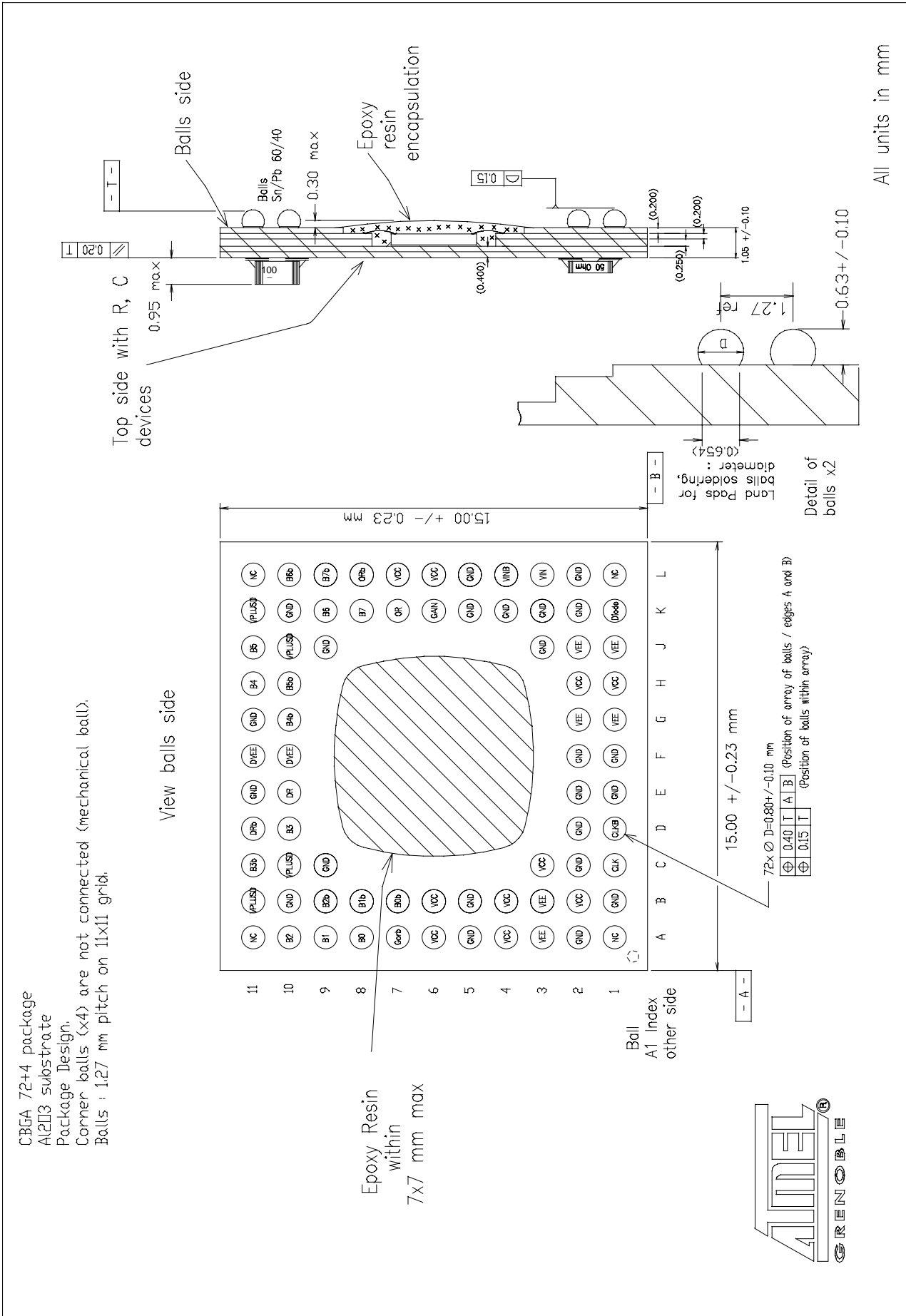
4.3. TS8308500 PINOUT OF CBGA72 PACKAGE

BOTTOM VIEW
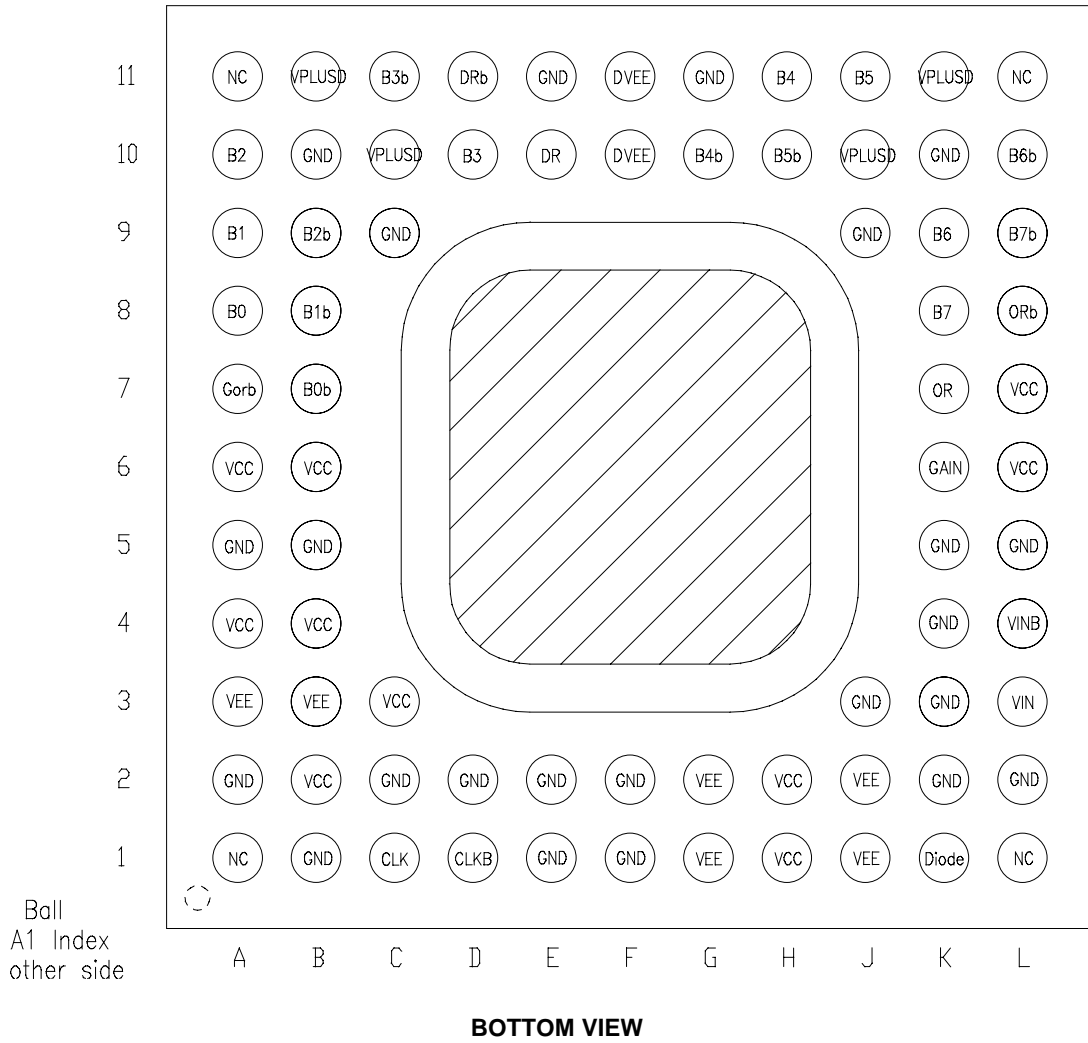
4.4. TS8308500 CAPACITIES AND RESISTANCES IMPLANT
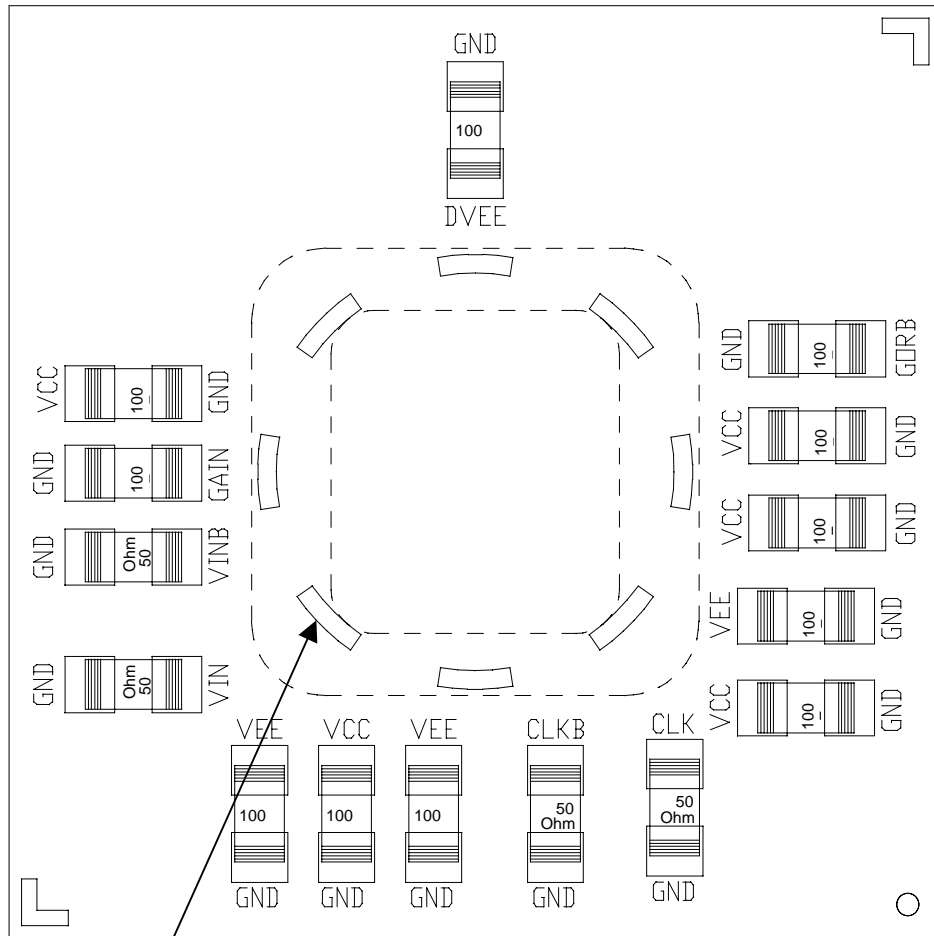
Only on-package marking
Electrically isolated

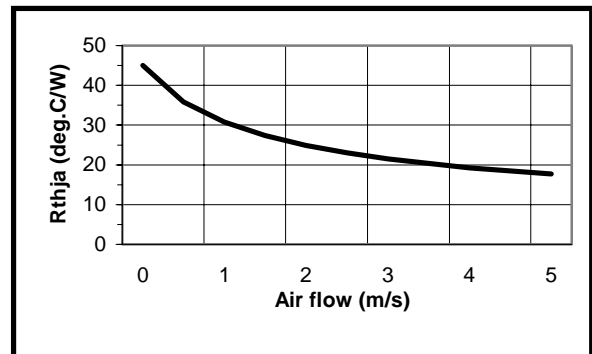**OUTLINE DIMENSIONS - 72 PINS CBGA**

4.5. THERMAL AND MOISTURE CHARACTERISTICS

4.5.1. THERMAL RESISTANCE FROM JUNCTION TO AMBIENT : RTHJA

The following table lists the convector thermal performances parameters of the device itself, with no external heatsink added.

Air flow (m/s)	Estimated ja thermal resistance (^{o}C / W)
0	45
0,5	35,8
1	30,8
1,5	27,4
2	24,9
2,5	23
3	21,5
4	19,3
5	17,7

4.5.2. THERMAL RESISTANCE FROM JUNCTION TO CASE : RTHJC

Typical value for Rthjc is given to 1.56°C/W.

This value does not include thermal contact resistance between package and external component (heatsink or PCBoard).
As an example, 2.0°C/W can be taken for 50 µm of thermal grease.

4.5.3. CBGA72 BOARD ASSEMBLY WITH EXTERNAL HEATSINK

It is recommended to use an external heatsink or PCBoard special design.

Cooling system efficiency can be monitored using the Temperature Sensing Diode, integrated in the device.
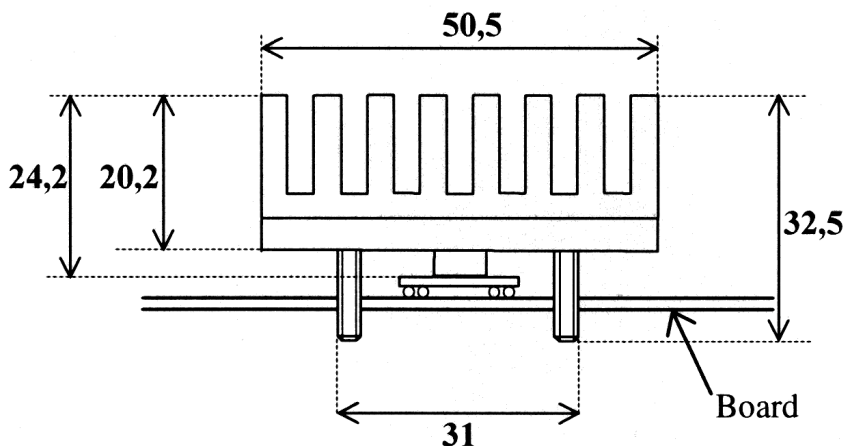
Note: Units = mm

4.5.4. MOISTURE CHARACTERISTICS

This device is very sensitive to the moisture (MSL6 according JEDEC standard).
When receiving the devices (in dry pack), you must follow strictly the instructions on the sticker.
The devices must be mounted within 6 hours at factory conditions of ≤ 30°C/60% Relative Humidity (RH).
These devices, if subjected to infrared reflow, vapor-phase reflow, or equivalent processing (peak package body temp. 220°C), must be baked before mounting for :
- 192 hours at 40°C + 5°C/-0°C and <5% RH for low-temperature device containers, or
- 24 hours at 125°C ± 5°C for high-temperature device containers.

Note : in case of reworking of a component on a board containing this device, the board could need to be heated. In this case and to preserve the TS8308500, it is important to bake the board first, according to the instructions above.

5. TYPICAL CHARACTERIZATION RESULTS

50/50 clock duty cycle, Binary output coding, Tj = 70°C, single-ended analog and clock inputs, unless otherwise specified.

5.1. STATIC LINEARITY – FS = 50 MSPS / FIN = 10 MHZ

5.1.1. INTEGRAL NON LINEARITY

INL = +/- 0.7 LSB

code
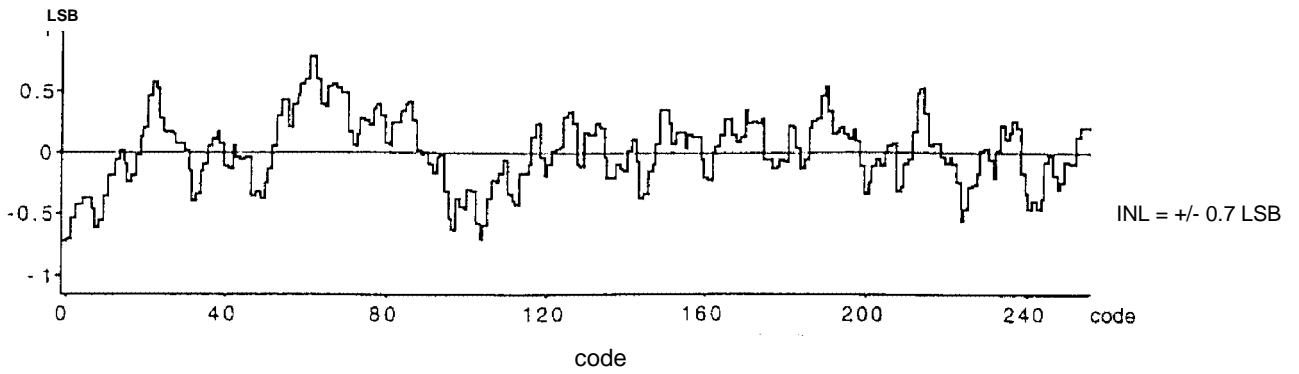
Clock Frequency = 50Msps   Signal Frequency = 10MHz

Positive peak : 0.68 LSB   Negative peak : -0.69 LSB

5.1.2. DIFFERENTIAL NON LINEARITY

DNL = +/- 0.3 LSB

code
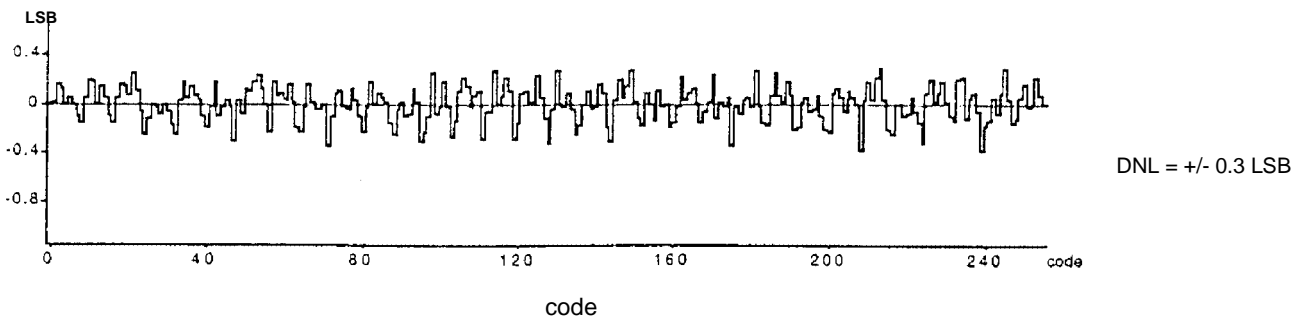
Clock Frequency = 50Msps   Signal Frequency = 10MHz

Positive peak : 0.3 LSB   Negative peak : -0.29 LSB

5.2. EFFECTIVE NUMBER OF BITS VERSUS POWER SUPPLIES VARIATION

Effective number of bits = f (VEEA) ; Fs = 500 MSPS ; Fin = 100 MHz

Effective number of bits = f (VCC) ; Fs = 500 MSPS ; Fin = 100 MHz

**Effective number of bits = f (VEED) ; Fs = 500 MSPS ; Fin = 100 MHz**
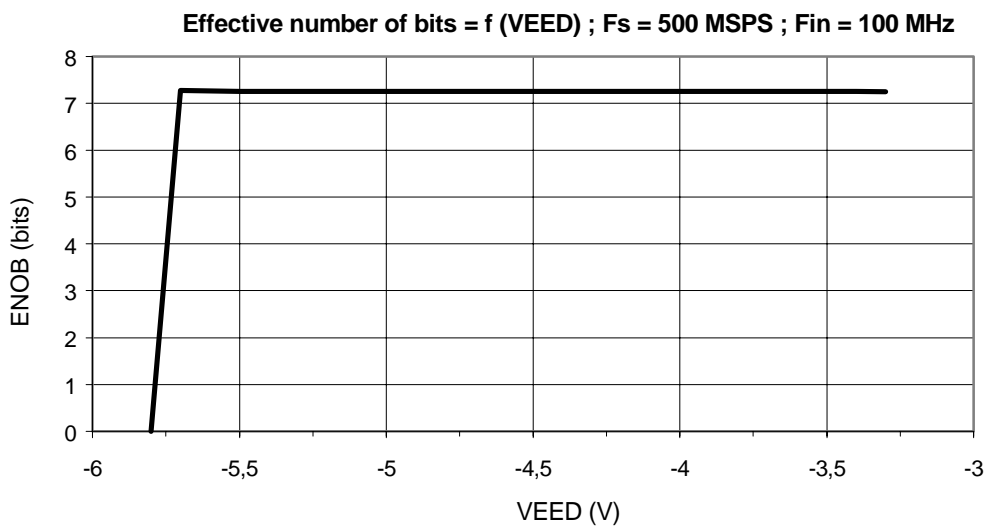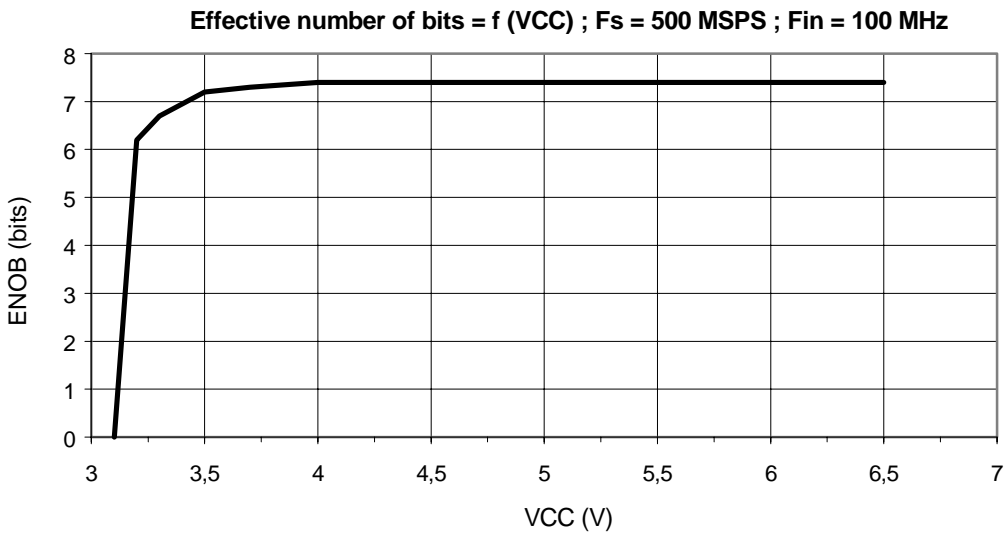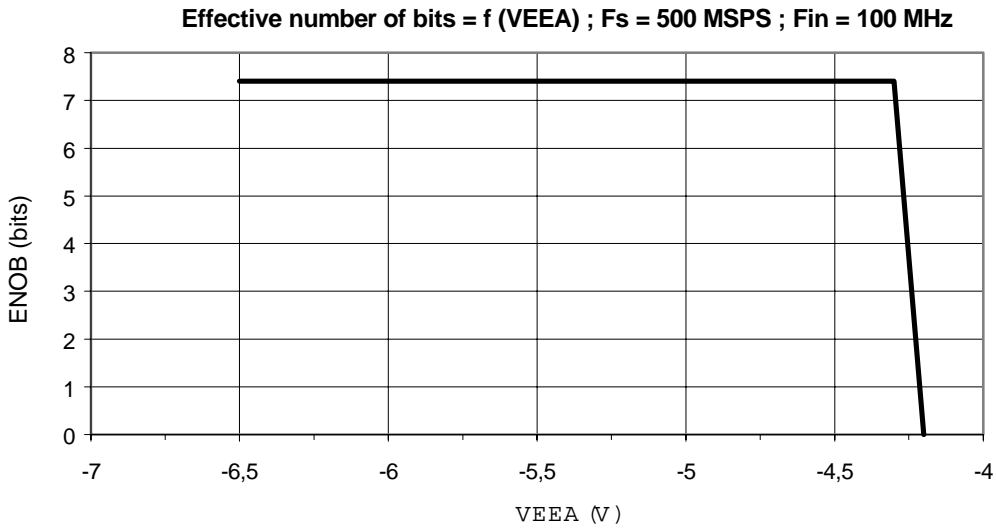
5.3. TYPICAL FFT RESULTS

5.3.1 SPECTRUM FOR Fs = 500 MSPS, Fin = 498 MHz (FULL SCALE INPUT)
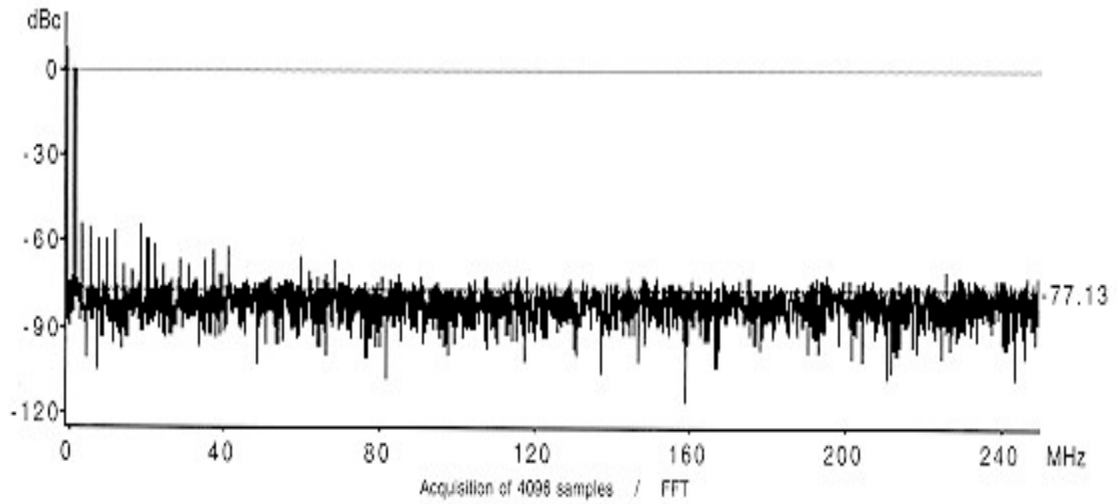
Acquisition of 4096 points
Fs = 500 MSPS
Fin = 498 MHz
SFSR = -0.94 dB
SNR = 45.39 dB

THD = -49.67 dBc
SINAD = 44.01 dB
SFDR = -54.31 dBc
ENOB = 7.13 bits

5.3.2. RECONSTRUCTED SIGNAL FOR Fs = 500 MSPS, Fin = 498 MHz (FULL SCALE INPUT)
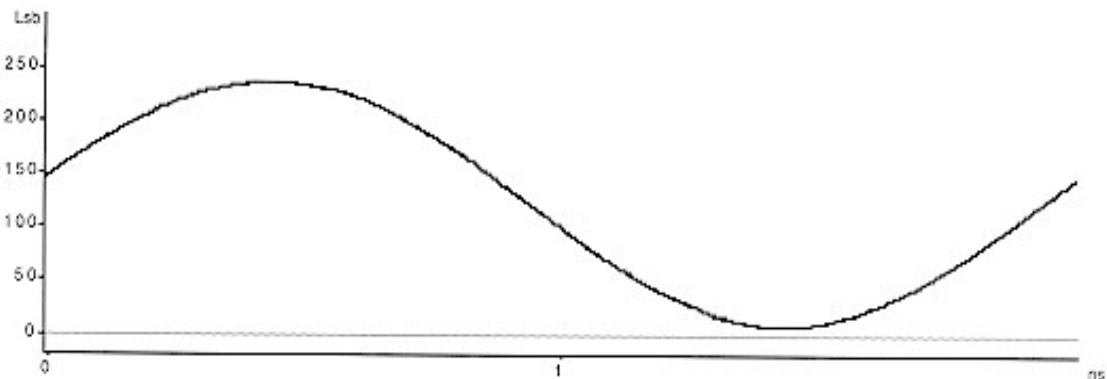
Acquisition of 4096 samples
Fs = 500 MSPS
Fin = 498 MHz

Amplitude: 0.221V (114.5 LSB)
Offset: 0V (122.5 LSB)

5.3.1. SPECTRUM FOR FS = 500 MSPS, FIN = 250 MHZ (FULL SCALE INPUT)
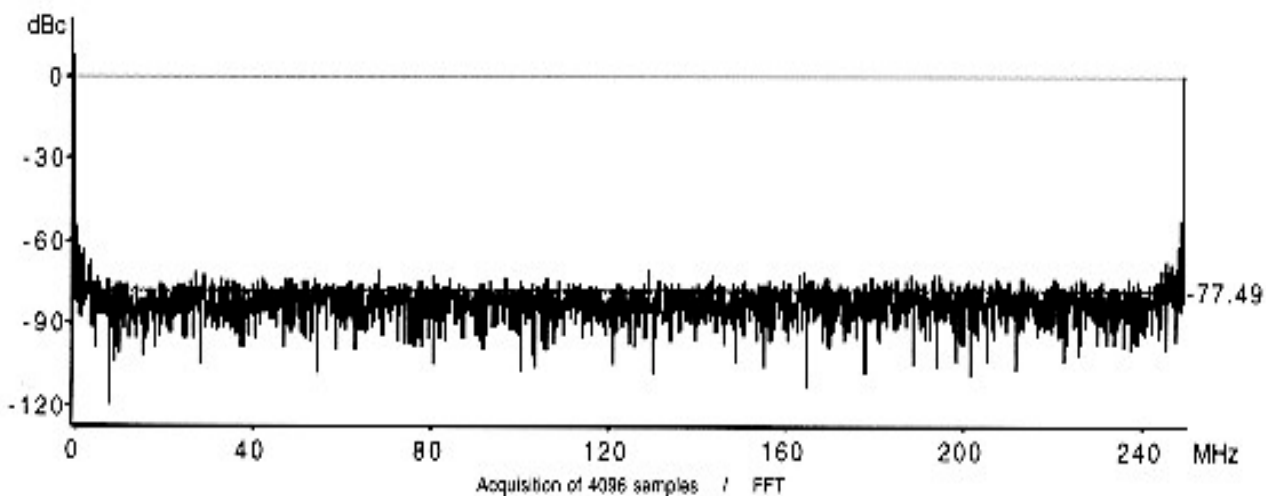
Acquisition of 4096 points
Fs = 500 MSPS
Fin = 250 MHz
SFSR = -1.02 dB
SNR = 45.84 dB

THD = -49.81 dBc
SINAD = 44.38 dB
SFDR = -52.78 dBc
ENOB = 7.19 bits

5.3.2. RECONSTRUCTED SIGNAL FOR FS = 500 MSPS; FIN = 250 MHZ (FULL SCALE INPUT)
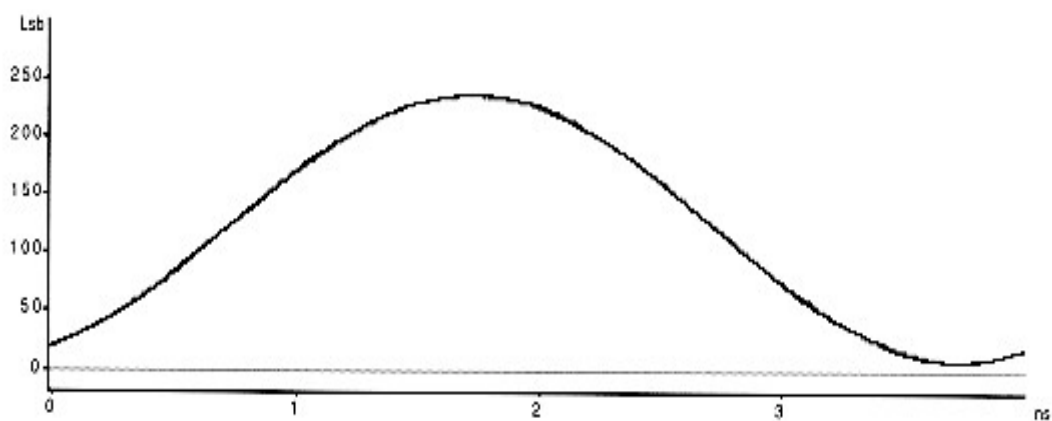
Acquisition of 4096 samples
Fs = 500 MSPS
Fin = 250 MHz

Amplitude: 0.189V (113.5 LSB)
Offset: 0V (122.5 LSB)

5.4. DYNAMIC PERFORMANCE VERSUS ANALOG INPUT FREQUENCY

Fs=500 Msps, Fin = 20MHz up to 1000 MHz, -1dB Full Scale input,

To be completed: ENOB, SNR and SFDR plots

5.5. EFFECTIVE NUMBER OF BITS (ENOB) VERSUS SAMPLING FREQUENCY

Analog Input Frequency : Fin = 250 MHz and Fs = 20 Msps to 1300 Msps

To Be Completed

5.6. SFDR VERSUS SAMPLING FREQUENCY

Analog Input Frequency : Fin = 250 MHz and Fs = 20 Msps to 1300 Msps

To Be Completed

5.7. TS8308500 ADC PERFORMANCES VERSUS JUNCTION TEMPERATURE

Fs = 500 Msps, Fin = 250 MHz, -1dB Full Scale Input, Tj = 0°C to 120°C.

ENOB, SNR and THD plots to be completed

Power consumption versus junction temperature
Fs = 500MSPS ; Fin = 250 MHz ; Duty cycle = 50%
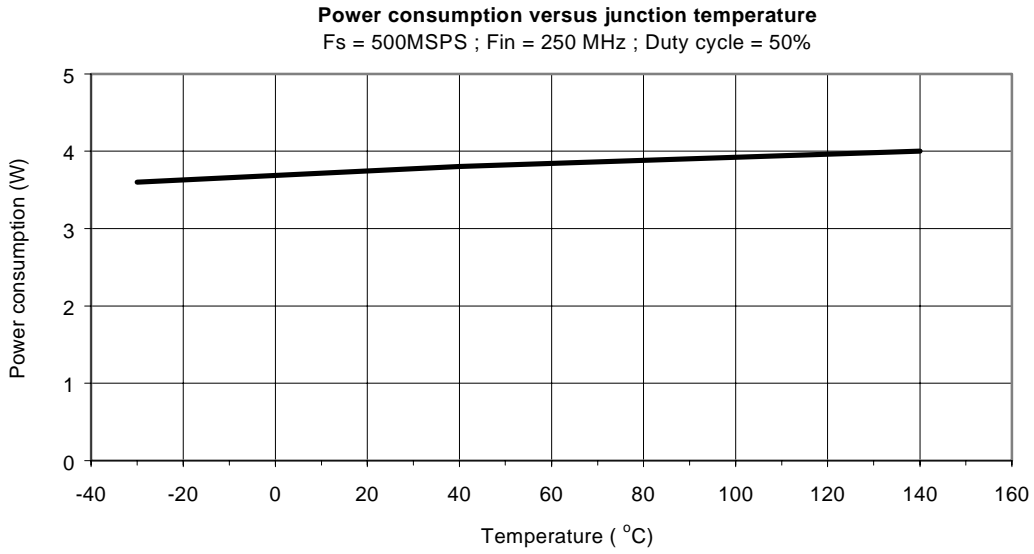
5.8. TYPICAL FULL POWER INPUT BANDWIDTH

1.3 GHz at -3 dB (-2dBm full power input)

Band Flatness / 8Bit 500Msps (-1 dB FS)
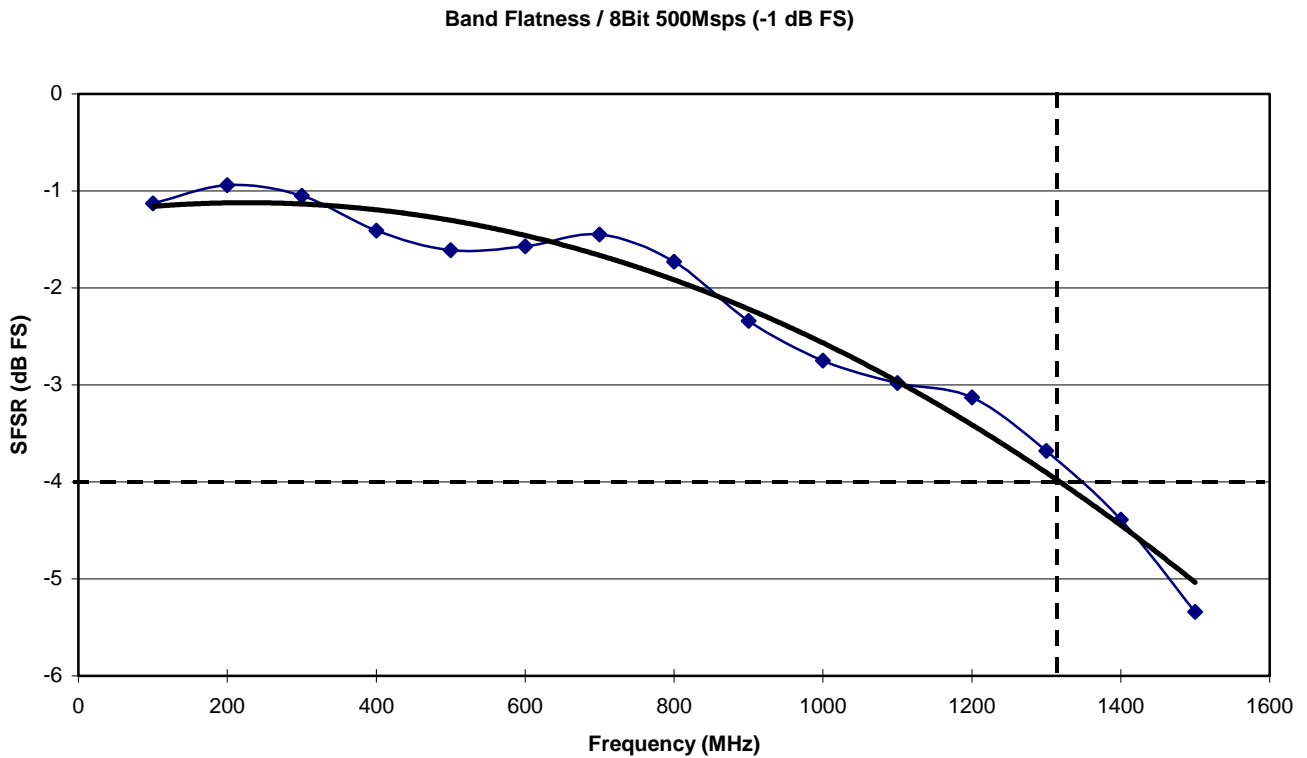
5.9. ADC STEP RESPONSE

Test pulse input characteristics : 20% to 80% input full scale and rise time ~ 200ps.
Note : This step response was obtained with the TSEV8308500 on board (device in die form).

5.9.1. TEST PULSE DIGITIZED WITH 20 GHz DSO

Vpp ~ 260 mV
Tr ~ 270 ps
50 mV/div
600 ps/div

time (ns)
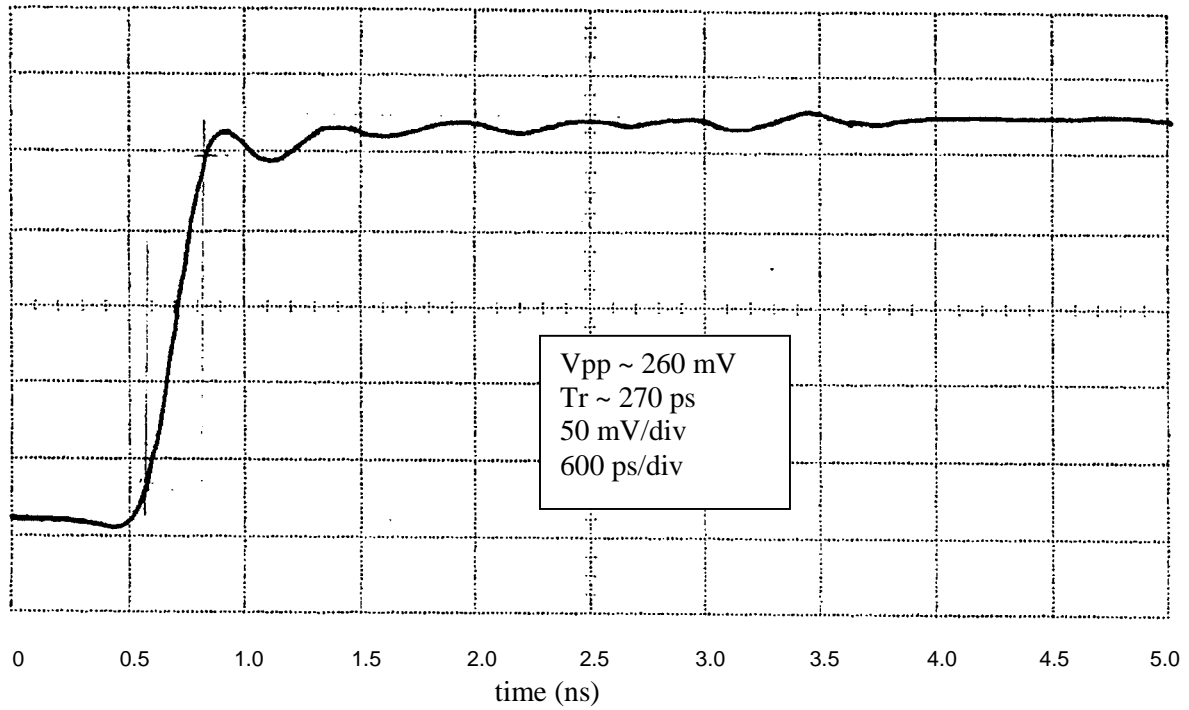
5.9.2. SAME TEST PULSE DIGITIZED WITH TS8308500 ADC

Tr ~ 330 ps
50 codes/div (Vpp ~260 mV)
600 ps/div

ADC code

time (ns)

6. DEFINITION OF TERMS

(BER)	*Bit Error Rate*	Probability to exceed a specified error threshold for a sample. An error code is a code that differs by more than +/- 4 LSB from the correct code.
(BW)	*Full power input bandwidth*	Analog input frequency at which the fundamental component in the digitally reconstructed output has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for input at Full Scale.
(SINAD)	*Signal to noise and distortion ratio*	Ratio expressed in dB of the RMS signal amplitude, set to 1dB below Full Scale, to the RMS sum of all other spectral components, including the harmonics except DC.
(SNR)	*Signal to noise ratio*	Ratio expressed in dB of the RMS signal amplitude, set to 1dB below Full Scale, to the RMS sum of all other spectral components excluding the five first harmonics.
(THD)	*Total harmonic distorsion*	Ratio expressed in dBc of the RMS sum of the first five harmonic components, to the RMS value of the measured fundamental spectral component.
(SFDR)	*Spurious free dynamic range*	Ratio expressed in dB of the RMS signal amplitude, set at 1dB below Full Scale, to the RMS value of the next highest spectral component (peak spurious spectral component). SFDR is the key parameter for selecting a converter to be used in a frequency domain application (Radar systems, digital receiver, network analyzer ….). It may be reported in dBc (i.e., degrades as signal levels is lowered), or in dBfs (i.e. always related back to converter full scale).
(ENOB)	*Effective Number Of Bits*	$ENOB = \dfrac{SINAD - 1.76 + 20 \log (A/V/2)}{6.02}$ Where A is the actual input amplitude and V is the full scale range of the ADC under test
(DNL)	*Differential non linearity*	The Differential Non Linearity for an output code i is the difference between the measured step size of code i and the ideal LSB step size. DNL (i) is expressed in LSBs. DNL is the maximum value of all DNL (i). DNL error specification of less than 1 LSB guarantees that there are no missing output codes and that the transfer function is monotonic.
(INL)	*Integral non linearity*	The Integral Non Linearity for an output code i is the difference between the measured input voltage at which the transition occurs and the ideal value of this transition. INL (i) is expressed in LSBs, and is the maximum value of all |INL (i)|.
(DG)	*Differential gain*	The peak gain variation (in percent) at five different DC levels for an AC signal of 20% Full Scale peak to peak amplitude. F_{IN} = 5 MHz. (TBC)
(DP)	*Differential phase*	Peak Phase variation (in degrees) at five different DC levels for an AC signal of 20% Full Scale peak to peak amplitude. F_{IN} = 5 MHz. (TBC)
(TA)	*Aperture delay*	Delay between the rising edge of the differential clock inputs (CLK,CLKB) (zero crossing point), and the time at which (V_{IN}, V_{INB}) is sampled.
(JITTER)	*Aperture uncertainty*	Sample to sample variation in aperture delay. The voltage error due to jitter depends on the slew rate of the signal at the sampling point.
(TS)	*Settling time*	Time delay to achieve 0.2 % accuracy at the converter output when a 80% Full Scale step function is applied to the differential analog input.
(ORT)	*Overvoltage recovery time*	Time to recover 0.2 % accuracy at the output, after a 150 % full scale step applied on the input is reduced to midscale.
(TOD)	*Digital data Output delay*	Delay from the falling edge of the differential clock inputs (CLK,CLKB) (zero crossing point) to the next point of change in the differential output data (zero crossing) with specified load.
(TD1)	*Time delay from Data to Data Ready*	Time delay from Data transition to Data ready.
(TD2)	*Time delay from Data Ready to Data*	General expression is TD1 = TC1 + TDR – TOD with TC = TC1 + TC2 = 1 encoding clock period.
(TC)	*Encoding clock period*	TC1 = Minimum clock pulse width (high) TC = TC1 + TC2 TC2 = Minimum clock pulse width (low)
(TPD)	*Pipeline Delay*	Number of clock cycles between the sampling edge of an input data and the associated output data being made available, (not taking in account the TOD). For the TS8308500 the TPD is 4 clock periods.
(TRDR)	*Data Ready reset delay*	Delay between the falling edge of the Data Ready output asynchronous Reset signal (DDRB) and the reset to digital zero transition of the Data Ready output signal (DR).

(TR)	*Rise time*	Time delay for the output DATA signals to rise from 20% to 80% of delta between low level and high level.
(TF)	*Fall time*	Time delay for the output DATA signals to fall from 80% to 20% of delta between low level and high level.
(PSRR)	*Power supply rejection ratio*	Ratio of input offset variation to a change in power supply voltage.
(NRZ)	*Non return to zero*	When the input signal is larger than the upper bound of the ADC input range, the output code is identical to the maximum code and the Out of Range bit is set to logic one. When the input signal is smaller than the lower bound of the ADC input range, the output code is identical to the minimum code, and the Out of range bit is set to logic one. (It is assumed that the input signal amplitude remains within the absolute maximum ratings).
(IMD)	*InterModulation Distortion*	The two tones intermodulation distortion (IMD) rejection is the ratio of either input tone to the worst third order intermodulation products. The input tones levels are at – 7dB Full Scale.
(NPR)	*Noise Power Ratio*	The NPR is measured to characterize the ADC performance in response to broad bandwidth signals. When using a notch-filtered broadband white-noise generator as the input to the ADC under test, the Noise Power Ratio is defined as the ratio of the average out-of-notch to the average in-notch power spectral density magnitudes for the FFT spectrum of the ADC output sample test.

7. TS8308500 MAIN FEATURES

7.1. TIMING INFORMATIONS

7.1.1. TIMING VALUE FOR TS8308500

Timing values as defined in 3.3 are advanced data, issuing from electric simulations and first characterization results fitted with measurements.

Timing values are given for CBGA72 package inputs/outputs, taking into account package internal controlled impedance traces propagation delays, and specified termination loads.
Propagation delays in 50/75 ohms impedance traces are NOT taken into account for TOD and TDR.
Apply proper derating values corresponding to termination topology.

The min/max timing values are valid over the full temperature range in the following conditions :

Note 1 : Specified Termination Load (Differential output Data and Data Ready) :

50 ohms resistor in parallel with 1 standard ECLinPS register from Motorola, (e.g : 10E452)
(Typical ECLinPS inputs shows a typical input capacitance of 1.5 pF (including package and ESD protections)
If addressing an output Dmux, take care if some Digital outputs do not have the same termination load and apply corresponding derating value given below.

Note 2 : Output Termination Load derating values for TOD and TDR :
~ 35 ps/pF or 50 ps per additional ECLinPS load.

Note 3 :Propagation time delay derating values have also to be applied for TOD and TDR :
~ 6 ps/mm (155 ps/inch) for TSEV8308500 Evaluation Board.
Apply proper time delay derating value if a different dielectric layer is used.

7.1.2. PROPAGATION TIME CONSIDERATIONS

TOD and TDR Timing values are given from pin to pin and DO NOT include the additional propagation times between device pins and input/output termination loads. For the TSEV8308500 Evaluation Board, the propagation time delay is 6ps/mm (155ps/inch) corresponding to 3.4 (@10GHz) dielectric constant of the RO4003 used for the Board.

If a different dielectric layer is used (for instance Teflon), please use appropriate propagation time values.

TD does NOT depend on propagation times because it is a differential data.
(TD is the time difference between Data Ready output delay and digital Data output delay)
TD is also the most straightforward data to measure, again because it is differential :
TD can be measured directly onto termination loads, with matched Oscilloscopes probes.

7.1.3. TOD - TDR VARIATION OVER TEMPERATURE

Values for TOD and TDR track each other over temperature (1 percent variation for TOD - TDR per 100 degrees Celsius temperature variation).

Therefore TOD - TDR variation over temperature is negligible. Moreover, the internal (on-chip) and package skews between each Data TODs and TDR effect can be considered as negligible.

Consequently, minimum values for TOD and TDR are never more than 100 ps apart. The same is true for the TOD and TDR maximum values.

In other terms :
If TOD is at 1150 ps, TDR will not be at 1620 ps (maximum time delay for TDR).
If TOD is at 1660 ps, TDR will not be at 1110 ps (minimum time delay for TDR) However, external TOD - TDR values may be dictated by total digital data skews between every TODs (each digital data) and TDR :
MCM Board , bonding wires and output lines lengths differences, and output termination impedance mismatches.

The external (on board) skew effect has NOT been taken into account for the specification of the minimum and maximum values for TOD-TDR.

7.1.4. PRINCIPLE OF OPERATION

The Analog input is sampled on the rising edge of external clock input (CLK,CLKB) after TA (aperture delay) of typically 250ps .
The digitized data is available after 4 clock periods latency (pipeline delay (TPD)), on clock rising edge, after 1360 ps typical propagation delay TOD.

The Data Ready differential output signal frequency (DR,DRB) is half the external clock frequency, that is it switches at the same rate as the digital outputs.

The Data Ready output signal (DR,DRB) switches on external clock falling edge after a propagation delay TDR of typically 1320 ps.

A Master Asynchronous Reset input command DRRB (ECL compatible single-ended input) is available for initializing the differential Data Ready output signal (DR,DRB) .This feature is mandatory in certain applications using interleaved ADCs or using a single ADC with demultiplexed outputs. Actually, without Data Ready signal initialization, it is impossible to store the output digital data in a defined order.

7.2.   PRINCIPLE OF DATA READY SIGNAL CONTROL BY DRRB INPUT COMMAND

7.2.1.   DATA READY OUTPUT SIGNAL RESET

The Data Ready signal is reset on falling edge of DRRB input command, on ECL logical low level (-1.8V). DRRB may also be tied to VEE = - 5V for Data Ready output signal Master Reset. So long DRRB remains at logical low level, (or tied to VEE = - 5V), the Data Ready output remains at logical zero and is independent of the external free running encoding clock.

The Data Ready output signal (DR,DRB) is reset to logical zero after TRDR= 720 ps typical.

TRDR is measured between the -1.3V point of the falling edge of DRRB input command and the zero crossing point of the differential Data Ready output signal (DR,DRB).

The Data Ready Reset command may be a pulse of 1 ns minimum time width.

7.2.2.   DATA READY OUTPUT SIGNAL RESTART

The Data Ready output signal restarts on DRRB command rising edge, ECL logical high levels (-0.8V).
DRRB may also be Grounded, or is allowed to float, for normal free running Data Ready output signal.

The Data Ready signal restart sequence depends on the logical level of the external encoding clock, at DRRB rising edge instant :

1)   The DRRB rising edge occurs when external encoding clock input (CLK,CLKB) is LOW :
      The Data Ready output first rising edge occurs after half a clock period on the clock falling edge, after a delay time TDR = 1320 ps already defined hereabove.
2)   The DRRB rising edge occurs when external encoding clock input (CLK,CLKB) is HIGH :
      The Data Ready output first rising edge occurs after one clock period on the clock falling edge, and a delay TDR = 1320ps.

Consequently, as the analog input is sampled on clock rising edge, the first digitized data corresponding to the first acquisition (N) after Data Ready signal restart (rising edge) is always strobed by the third rising edge of the data ready signal.
The time delay (TD1) is specified between the last point of a change in the differential output data (zero crossing point) to the rising or falling edge of the differential Data Ready signal (DR,DRB) (zero crossing point).

Note 1 : For normal initialization of Data Ready output signal, the external encoding clock signal frequency and level must be controlled.
It is reminded that the minimum encoding clock sampling rate for the ADC is 10 MSPS and consequently the clock cannot be stopped.

Note 2 : One single pin is used for both DRRB input command and die junction temperature monitoring.
Pin denomination will be DRRB/DIOD.(On former version denomination was DIOD.)
Temperature monitoring and Data Ready control by DRRB is not possible simultaneously.

7.3.   ANALOG INPUTS (VIN) (VINB)

The analog input Full Scale range is 0.5 Volts peak to peak (Vpp), or -2 dBm into the 50 ohms termination resistor.

In differential mode input configuration, that means 0.25 Volt on each input, or +/- 125 mV around zero volt. The input common mode is GROUND.

The typical input capacitance is 3 pF for TS8308500 in CBGA package.

Differential inputs voltage span

(VIN,VINB) = +/- 250 mV = 500 mV diff
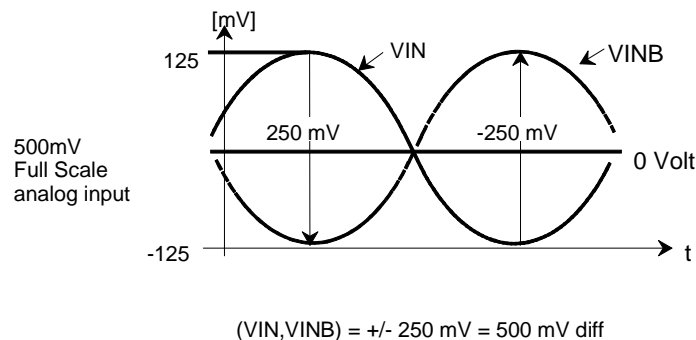
Differential versus single ended analog input operation
The TS8308500 can operate at full speed in either differential or single ended configuration.
This is explained by the fact the ADC uses a high input impedance differential preamplifier stage, (preceding the Sample and hold stage), which has been designed in order to be entered either in differential mode or single–ended mode.

This is true so long as the out of phase analog input pin VINB is 50 ohms terminated very closely to one of the neighboring shield ground pins (52, 53, 58, 59) which constitute the local ground reference for the inphase analog input pin (VIN).

Thus the differential analog input preamplifier will fully reject the local ground noise (and any capacitively and inductively coupled noise) as common mode effects.

In typical single–ended configuration, enter on the (VIN) input pin, with the inverted phase input pin (VINB) grounded through the 50 ohms termination resistor.

In single–ended input configuration, the in-phase input amplitude is 0.5 Volt peak to peak, centered on 0V. (or -2 dBm into 50 ohms.)
The inverted phase input is at ground potential through the 50 ohms termination resistor.

However, dynamic performances can be somewhat improved by entering either analog or clock inputs in differential mode.

Typical Single ended analog input configuration

$V_{IN} = +/- 250$ mV $\Leftrightarrow$ 500 mV diff

50 Ω reverse termination
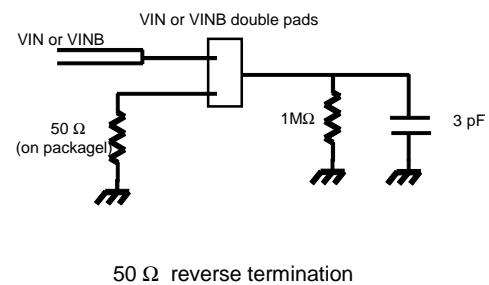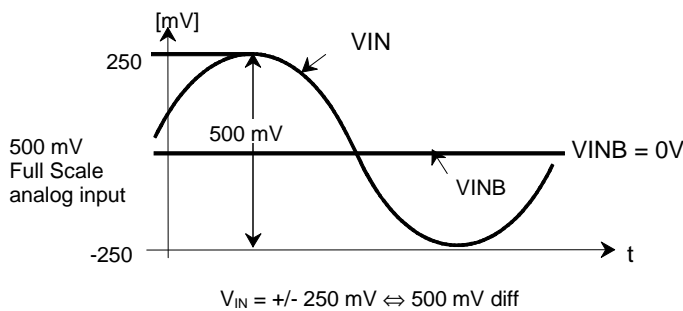
7.4. CLOCK INPUTS (CLK) (CLKB)

The TS8308500 can be clocked at full speed without noticeable performance degradation in either differential or single ended configuration.
This is explained by the fact the ADC uses a differential preamplifier stage for the clock buffer, which has been designed in order to be entered either in differential or single–ended mode.
Recommended sinewave generator characteristics are typically -120 dBc/Hz phase noise floor spectral density, @ 1 KHz from carrier , assuming a single tone 4 dBm input for the clock signal.

7.4.1. SINGLE ENDED CLOCK INPUT (GROUND COMMON MODE)

Although the clock inputs were intended to be driven differentially with nominal -0.8V / -1.8V ECL levels, the TS8308500 clock buffer can manage a single–ended sinewave clock signal centered around 0 Volt. This is the most convenient clock input configuration as it does not require the use of a power splitter.

No performance degradation (e.g. : due to timing jitter) is observed in this particular single–ended configuration up to 500 MSPS Nyquist conditions (Fin = 250 MHz).

This is all the more so true since the inverted phase clock input pin is 50 ohms terminated on the package (that is very close to one of the neighboring shield ground pin, which constitutes the local Ground reference for the inphase clock input).

Thus the TS8308500 differential clock input buffer will fully reject the local ground noise (and any capacitively and inductively coupled noise) as common mode effects.
Moreover, a very low phase noise sinewave generator must be used for enhanced jitter performance.

The typical inphase clock input amplitude is 1 Volt peak to peak, centered on 0 Volt (ground) common mode.
This corresponds to a typical clock input power level of 4 dBm into the 50 ohms termination resistor.
Do not exceed 10 dBm to avoid saturation of the preamplifier input transistors.

Single ended Clock input (Ground common mode)

VCLK common mode = 0 Volt
VCLKB=0 Volt
4 dBm typical clock input power level
(into 50 ohms termination resistor)
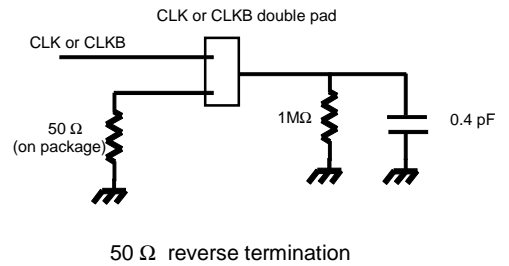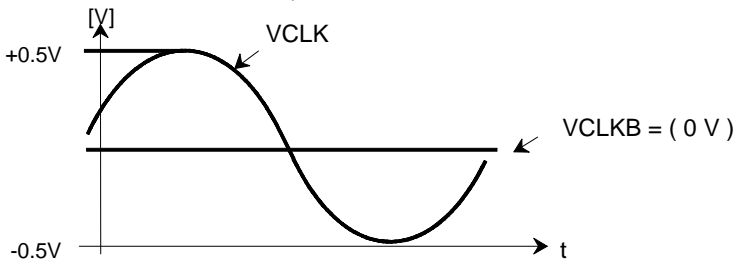
Note 1 : Do not exceed 10 dBm into the 50 ohms termination resistor for single clock input power level.

7.4.2.   DIFFERENTIAL ECL CLOCK INPUT

The clock inputs can be driven differentially with nominal –0.8V / -1.8V ECL levels.

In this mode, a low phase noise sinewave generator can be used to drive the clock inputs, followed by a power splitter (hybrid junction) in order to obtain 180 degrees out of phase sinewave signals. Biasing tees can be used for offsetting the common mode voltage to ECL levels.

Note: As the biasing tees propagation times are not matching, a tunable delay line is required in order to ensure the signals to be 180 degrees out of phase especially at fast clock rates in the 500 MSPS range.

Differential Clock inputs (ECL Levels)
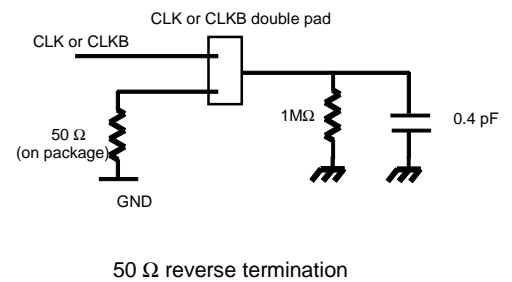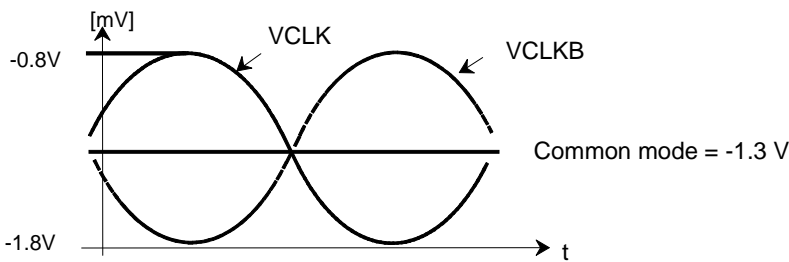
7.4.3.   SINGLE ENDED ECL CLOCK INPUT

In single–ended configuration enter on CLK (resp. CLKB) pin , with the inverted phase Clock input pin CLKB (respectively CLK) connected to -1.3V through the 50 ohms termination resistor (on package).
The inphase input amplitude is 1 Volt peak to peak, centered on -1.3 Volt common mode.

Single ended Clock input (ECL):
VCLK common mode = -1.3 Volt.
VCLKB = -1.3 Volt
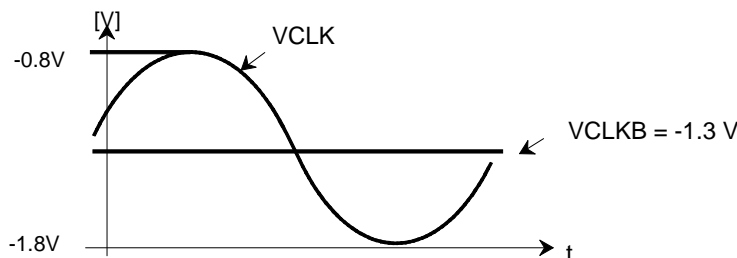
7.5.   NOISE IMMUNITY INFORMATIONS

Circuit noise immunity performance begins at design level.
Efforts have been made on the design in order to make the device as insensitive as possible to chip environment perturbations resulting from the circuit itself or induced by external circuitry.
(Cascode stages isolation, internal damping resistors, clamps, internal (onchip) decoupling capacitors.)

Furthermore, the fully differential operation from analog input up to the digital outputs provides enhanced noise immunity by common mode noise rejection.
Common mode noise voltage induced on the differential analog and clock inputs will be canceled out by these balanced differential amplifiers.

Moreover, proper active signals shielding has been provided on the chip to reduce the amount of coupled noise on the active inputs :
The analog inputs and clock inputs of the TS8308500 device have been surrounded by ground pins, which must be directly connected to the external ground plane.

7.6.   DIGITAL OUTPUTS

The TS8308500 differential output buffers are internally 75 ohms loaded. The 75 ohms resistors are connected to the digital ground pins through a -0.8v level shift diode (see Figures 3,4,5 on next page).

The TS8308500 output buffers are designed for driving 75 ohms (default) or 50 ohms properly terminated impedance lines or coaxial cables.
An 11 mA bias current flowing alternately into one of the 75 ohms resistors when switching ensures a 0.825 V voltage drop across the resistor (unterminated outputs).
The VPLUSD positive supply voltage allows the adjustment of the output common mode level from -1.2V (VPLUSD=0V for ECL output compatibility) to +1.2V (VPLUSD=2.4V for LVDS output compatibility).
Therefore, the single ended output voltages vary approximately between -0.8V and -1.625V, (outputs unterminated), around -1.2V common mode voltage.

Three possible line driving and back-termination scenarios are proposed (assuming VPLUSD=0V) :

        1) 75 Ohms impedance transmission lines, 75 ohms differentially terminated (Fig. 3) :
Each output voltage varies between -1V and -1.42V (respectively +1.4V and +1V), leading to +/- 0.41V =0.825 V in differential, around -1.21 V (respectively +1.21V) common mode for VPLUSD=0V (respectively 2.4V).

        2) 50 ohms impedance transmission lines, 50 ohms differentially termination (Fig. 4) :
Each output voltage varies between -1.02V and -1.35V (respectively +1.38V and +1.05V), leading to +/- 0.33V=660 mV in differential, around -1.18V (respectively +1.21V) common mode for VPLUSD=0V (respectively 2.4V).

        3) 75 ohms impedance open transmission lines (Fig. 5) :
Each output voltage varies between -1.6 V and -0.8 V (respectively +0.8V and +1.6V), which are true ECL levels, leading to +/- 0.8V=1.6V in differential, around -1.2V (respectively +1.2V) common mode for VPLUSD=0V (respectively 2.4V).
Therefore, it is possible to drive directly high input impedance storing registers, without terminating the 75 ohms transmission lines.
In time domain, that means that the incident wave will reflect at the 75 ohms transmission line output and travel back to the generator (i.e. the 75 ohms data output buffer). As the buffer output impedance is 75 ohms, no back reflection will occur.

Note : This is no longer true if a 50 ohms transmission line is used, as the latter is not matching the buffer 75 ohms output impedance.

Each differential output termination length must be kept identical .
It is recommended to decouple the midpoint of the differential termination with a 10 nF capacitor to avoid common mode perturbation in case of slight mismatch in the differential output line lengths.

Too large mismatches (keep < a few mm) in the differential line lengths will lead to switching currents flowing into the decoupling capacitor leading to switching ground noise.

The differential output voltage levels (75 or 50 ohms termination) are not ECL standard voltage levels, however it is possible to drive standard logic ECL circuitry like the ECLinPS logic line from MOTOROLA.

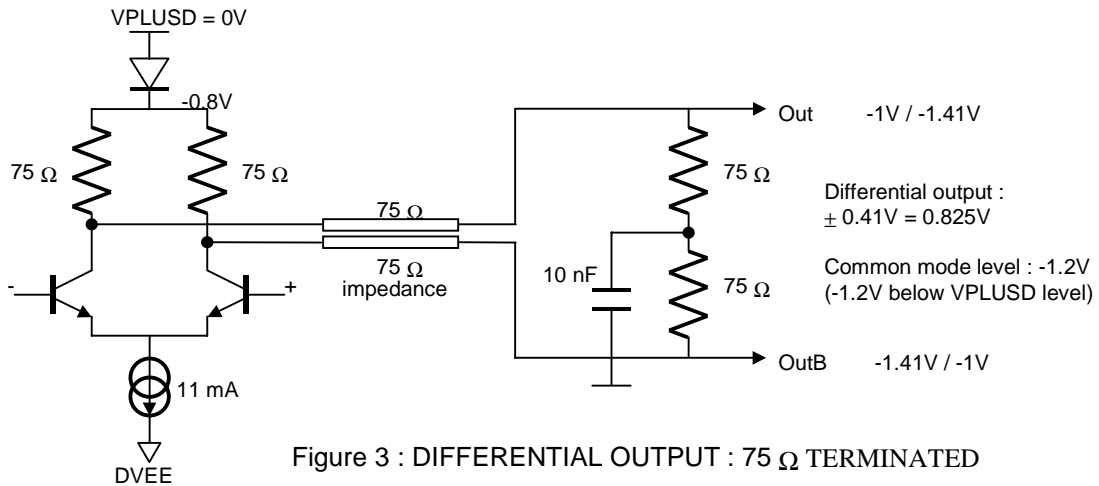**DIFFERENTIAL OUTPUT LOADING CONFIGURATIONS (LEVELS FOR ECL COMPATIBILITY)**
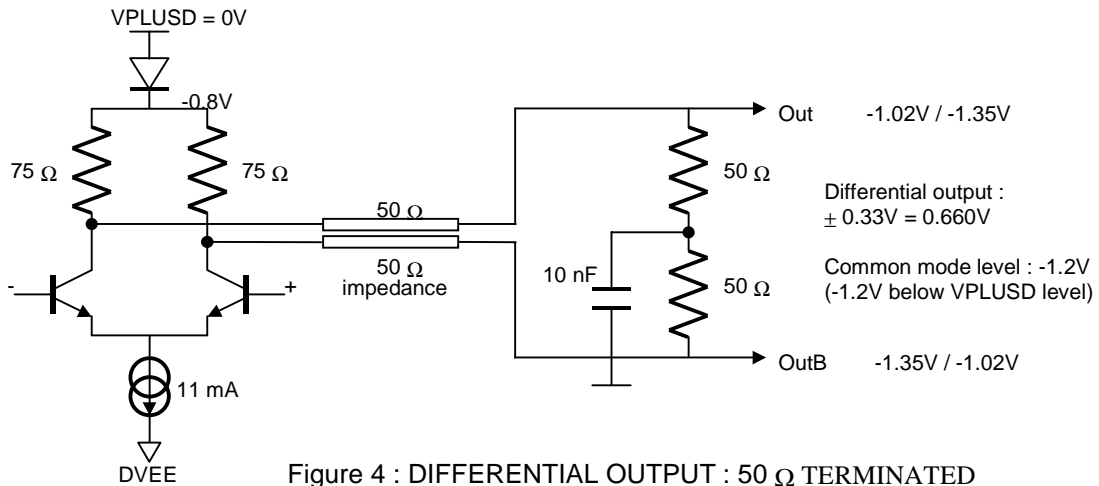

Figure 3 : DIFFERENTIAL OUTPUT : 75 Ω TERMINATED
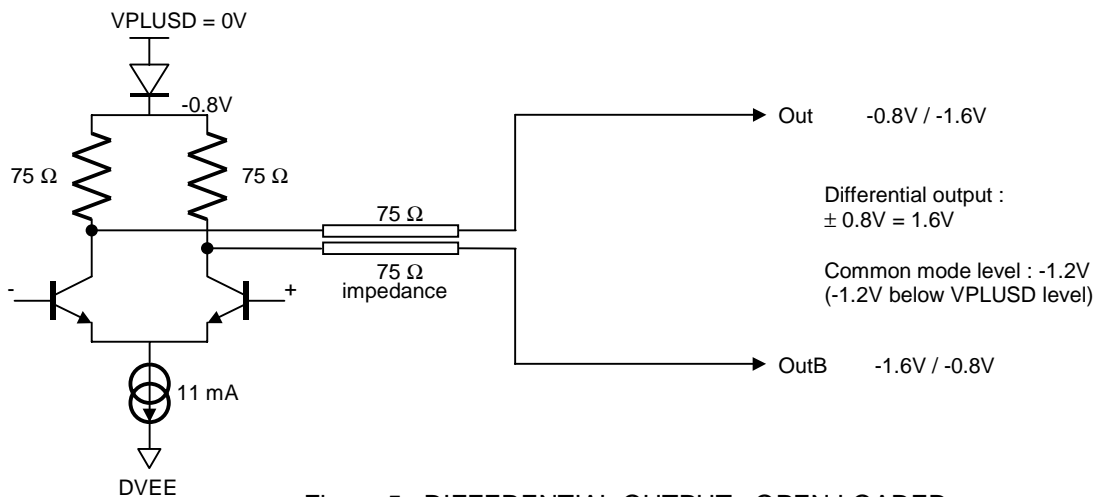

Figure 4 : DIFFERENTIAL OUTPUT : 50 Ω TERMINATED

Figure 5 : DIFFERENTIAL OUTPUT : OPEN LOADED

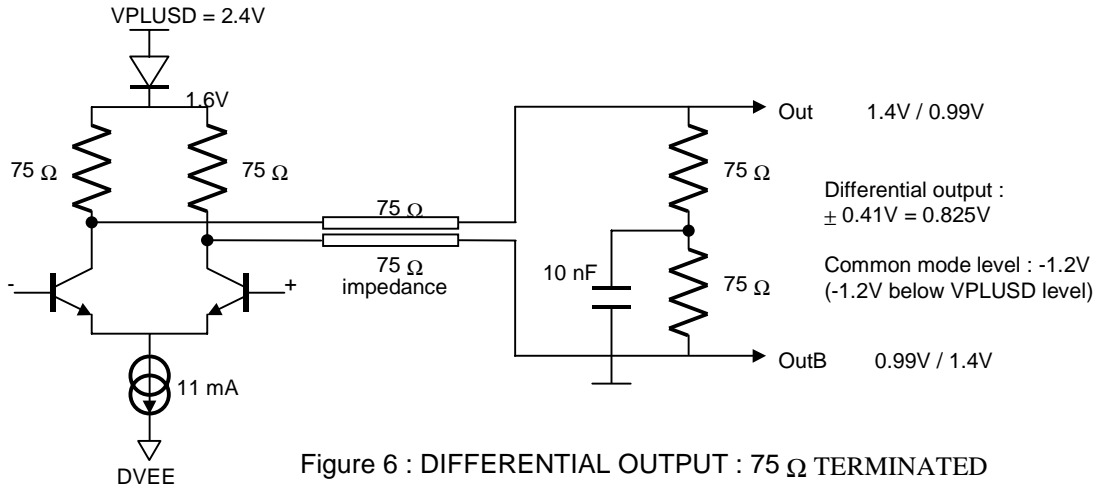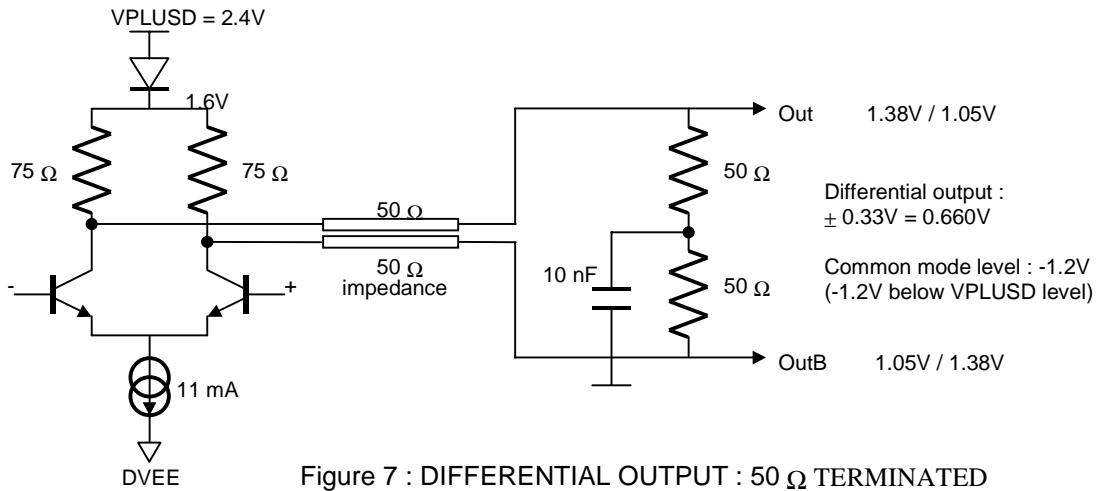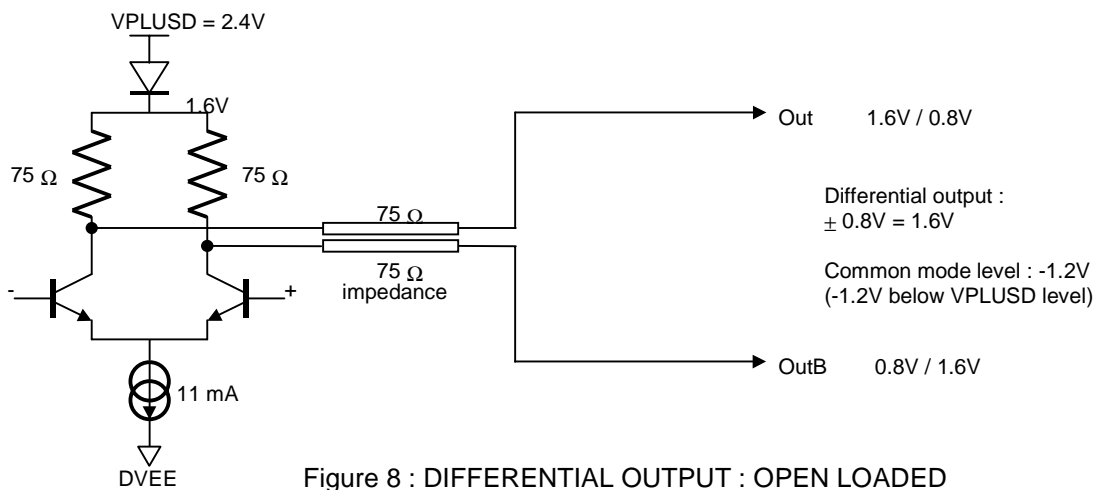**DIFFERENTIAL OUTPUT LOADING CONFIGURATIONS (LEVELS FOR LVDS COMPATIBILITY)**

VPLUSD = 2.4V

1.6V

75 Ω   75 Ω

75 Ω
75 Ω impedance

-        +

11 mA

DVEE

Out   1.4V / 0.99V

75 Ω

Differential output :
± 0.41V = 0.825V

10 nF   75 Ω

Common mode level : -1.2V
(-1.2V below VPLUSD level)

OutB   0.99V / 1.4V

Figure 6 : DIFFERENTIAL OUTPUT : 75 Ω TERMINATED

VPLUSD = 2.4V

1.6V

75 Ω   75 Ω

50 Ω
50 Ω impedance

-        +

11 mA

DVEE

Out   1.38V / 1.05V

50 Ω

Differential output :
± 0.33V = 0.660V

10 nF   50 Ω

Common mode level : -1.2V
(-1.2V below VPLUSD level)

OutB   1.05V / 1.38V

Figure 7 : DIFFERENTIAL OUTPUT : 50 Ω TERMINATED

VPLUSD = 2.4V

1.6V

75 Ω   75 Ω

75 Ω
75 Ω impedance

-        +

11 mA

DVEE

Out   1.6V / 0.8V

Differential output :
± 0.8V = 1.6V

Common mode level : -1.2V
(-1.2V below VPLUSD level)

OutB   0.8V / 1.6V

Figure 8 : DIFFERENTIAL OUTPUT : OPEN LOADED

7.7. OUT OF RANGE BIT

An Out of Range (OR,ORB) bit is provided that goes to logical high state when the input exceeds the positive full scale or falls below the negative full scale.
When the analog input exceeds the positive full scale, the digital output data remain at high logical state, with (OR,ORB) at logical one.
When the analog input falls below the negative full scale, the digital outputs remain at logical low state, with (OR,ORB) at logical one again.

7.8. GRAY OR BINARY OUTPUT DATA FORMAT SELECT

The TS8308500 internal regeneration latches indecision (for inputs very close to latches threshold) may produce errors in the logic encoding circuitry and leading to large amplitude output errors.

This is due to the fact that the latches are regenerating the internal analog residues into logical states with a finite voltage gain value (Av) within a given positive amount of time $\Delta(t)$:
 $Av= \exp(\Delta(t)/\tau)$, with τ the positive feedback regeneration time constant.

The TS8308500 has been designed for reducing the probability of occurrence of such errors to approximately 10^{-13} (targeted for the TS8308500 at 500 MSPS).

A standard technique for reducing the amplitude of such errors down to +/-1 LSB consists to output the digital data in Gray code format. Though the TS8308500 has been designed for featuring a Bit Error Rate of 10^{-13} with a binary output format, it is possible for the user to select between the Binary or Gray output data format, in order to reduce the amplitude of such errors when occurring, by storing Gray output codes.

Digital Data format selection :
        BINARY output format if GORB is floating or VCC.
        GRAY output format if GORB is connected to ground (0V).

7.9. DIODE PIN K1

One single pin is used for both DRRB input command and die junction monitoring. The pin denomination is DRRB/DIOD. Temperature monitoring and Data Ready control by DRRB is not possible simultaneously.

(See section 7.2 for Data Ready Reset input command).

The operating die junction temperature must be kept below145°C, therefore an adequate cooling system has to be set up.
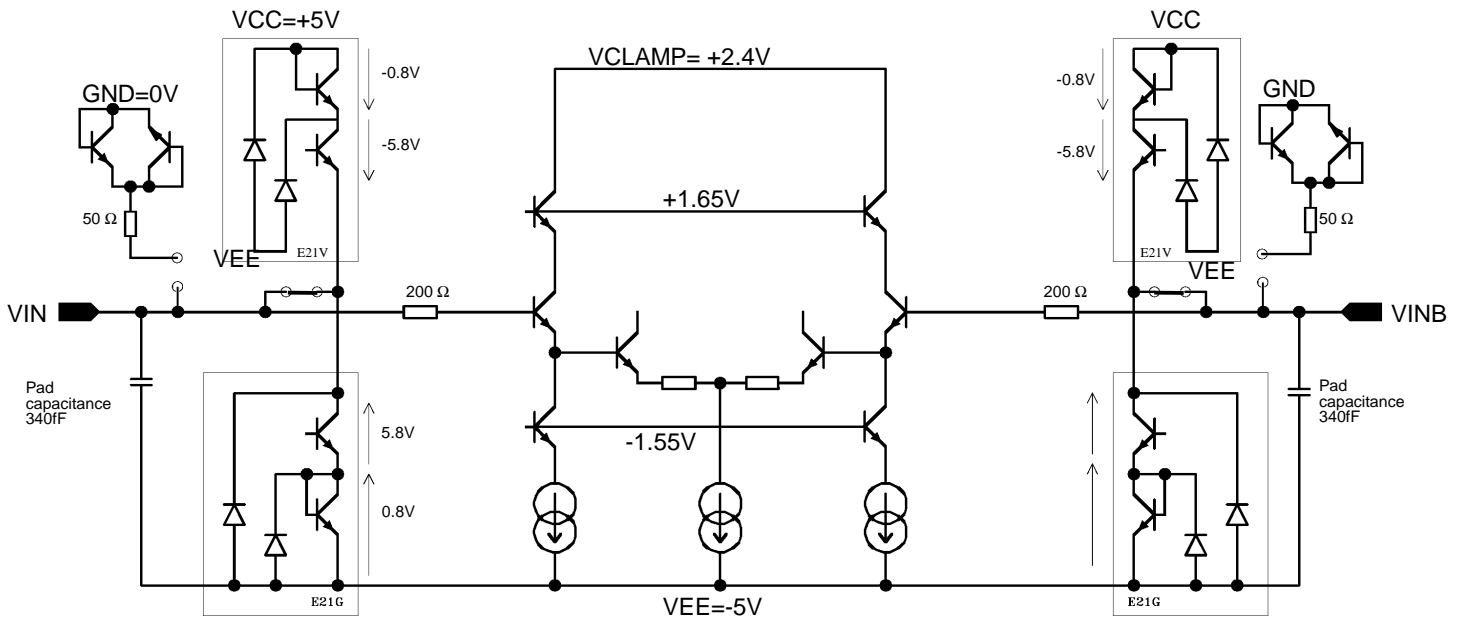The diode mounted transistor measured Vbe value versus junction temperature is given below.
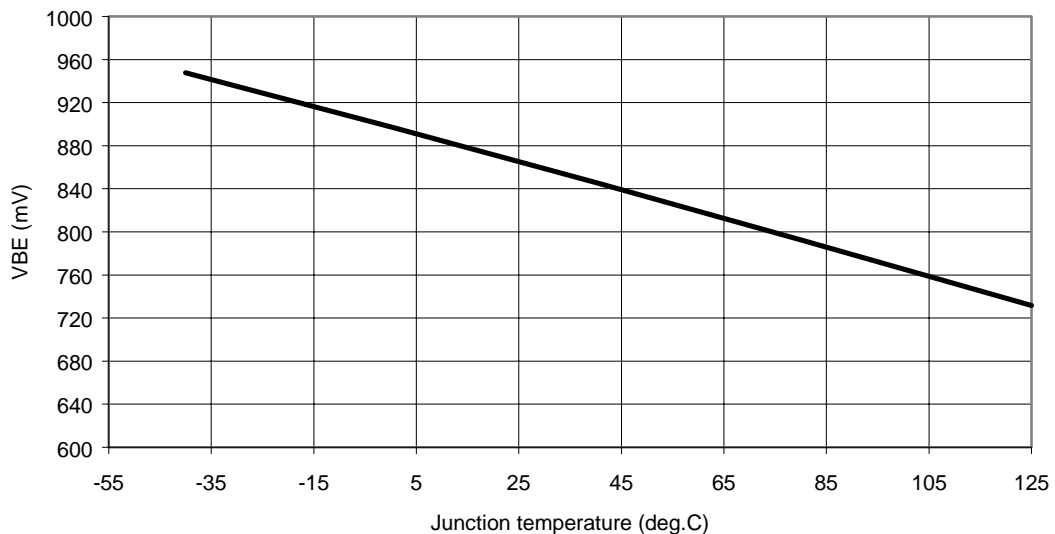
7.10. ADC GAIN CONTROL PIN K6

The ADC gain is adjustable by the means of the pin K6 (input impedance is 1MΩ in parallel with 2pF)
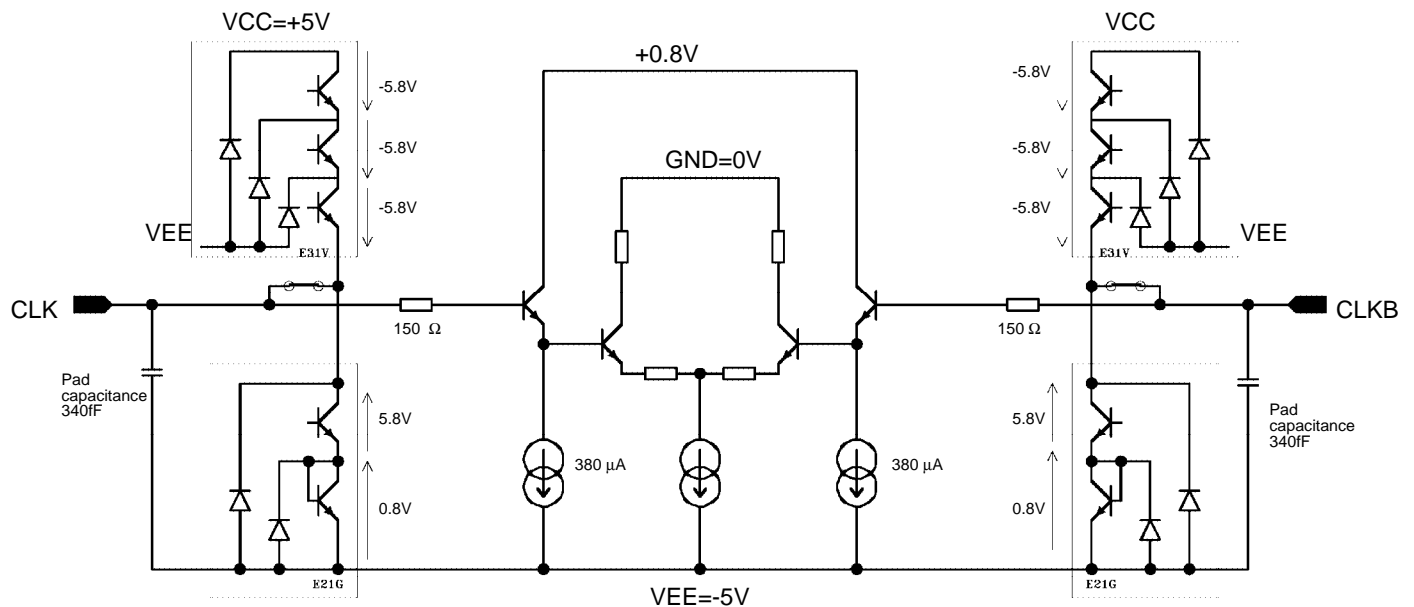The gain adjust transfer function is given below :
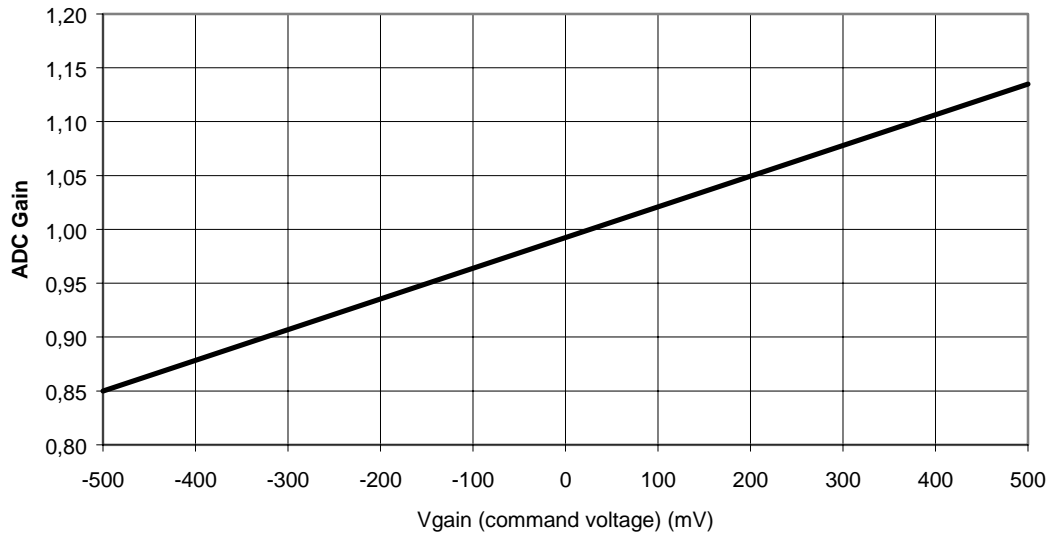
8. EQUIVALENT INPUT / OUTPUT SCHEMATICS

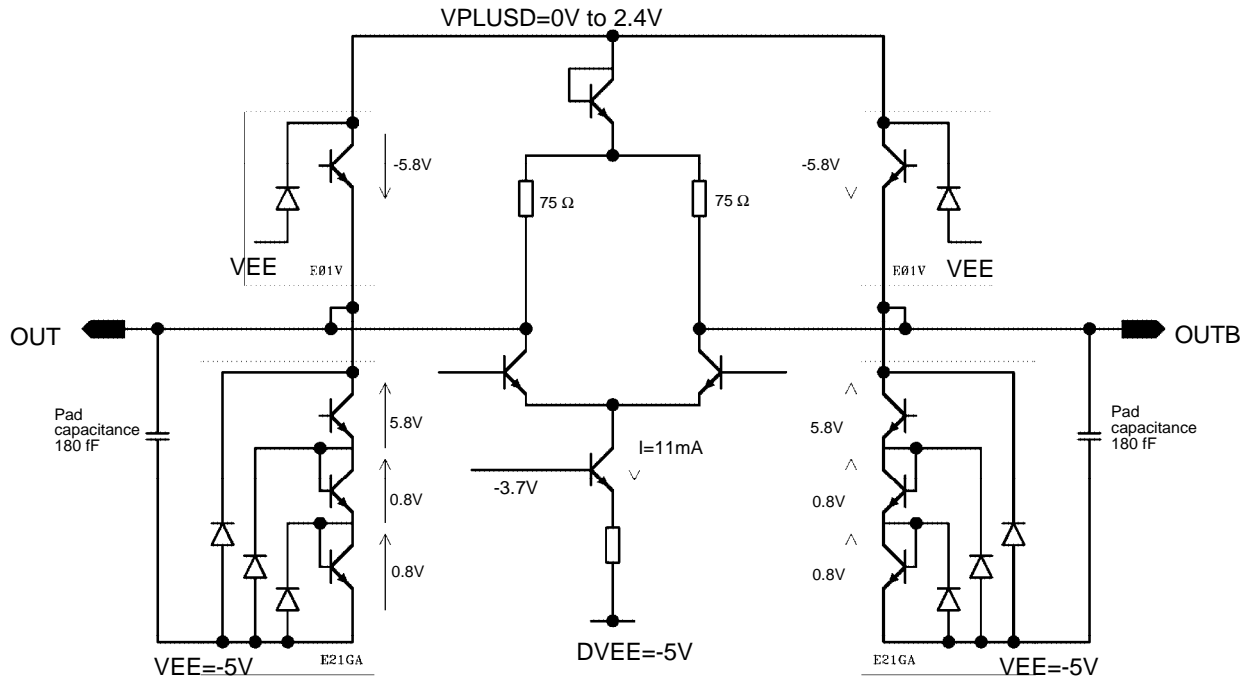### 8.1. EQUIVALENT ANALOG INPUT CIRCUIT AND ESD PROTECTIONS

Note : the ESD protection equivalent capacitance is 150 fF.

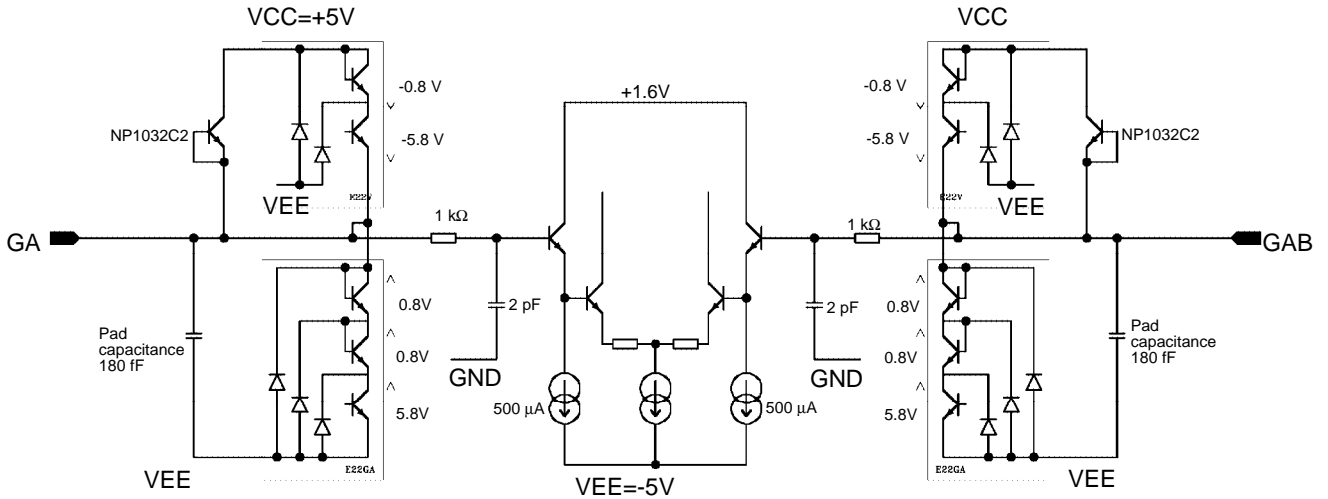### 8.2. EQUIVALENT ANALOG CLOCK INPUT CIRCUIT AND ESD PROTECTIONS

Note : the ESD protection equivalent capacitance is 150 fF.

8.3.   EQUIVALENT DATA OUTPUT BUFFER CIRCUIT AND ESD PROTECTIONS

Note : the ESD protection equivalent capacitance is 150 fF.

8.4.   ADC GAIN ADJUST EQUIVALENT INPUT CIRCUITS AND ESD PROTECTIONS

Note : the ESD protection equivalent capacitance is 150 fF.

8.5. GORB EQUIVALENT INPUT SCHEMATIC AND ESD PROTECTIONS

GORB: gray or binary select input; floating or tied to VCC -> binary
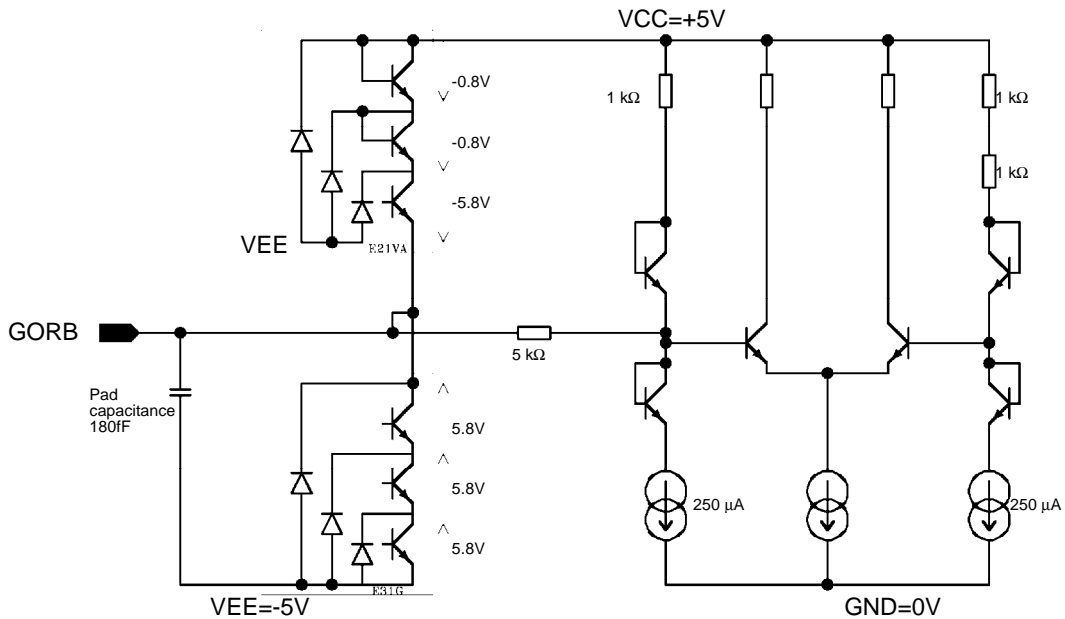
Note : the ESD protection equivalent capacitance is 150 fF.

8.6. DRRB EQUIVALENT INPUT SCHEMATIC AND ESD PROTECTIONS

Actual protection range: 6.6V above VEE,
In fact stress above GND are clipped by
the CB diode used for Tj monitoring
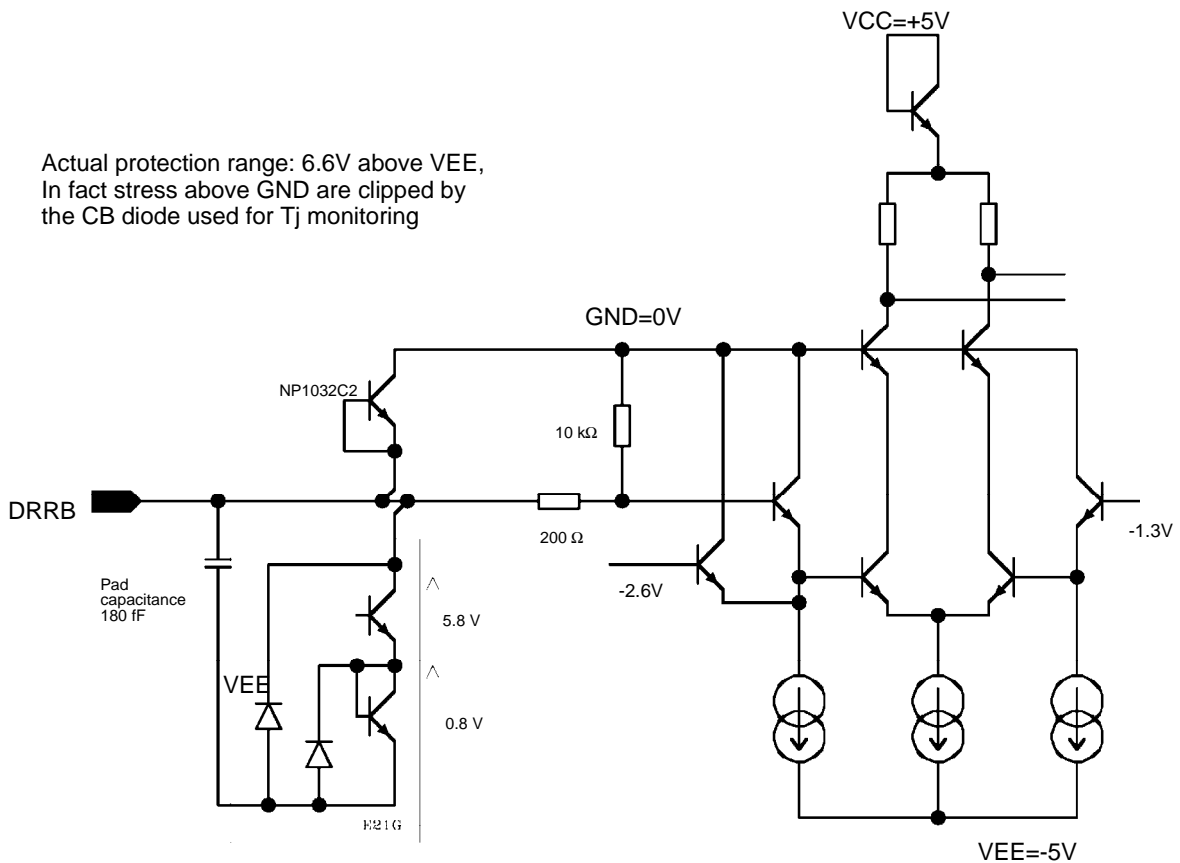
Note : the ESD protection equivalent capacitance is 150 fF.

9. TSEV8308500G : DEVICE EVALUATION BOARD

For complete specification, see separate TSEV8308500 document.
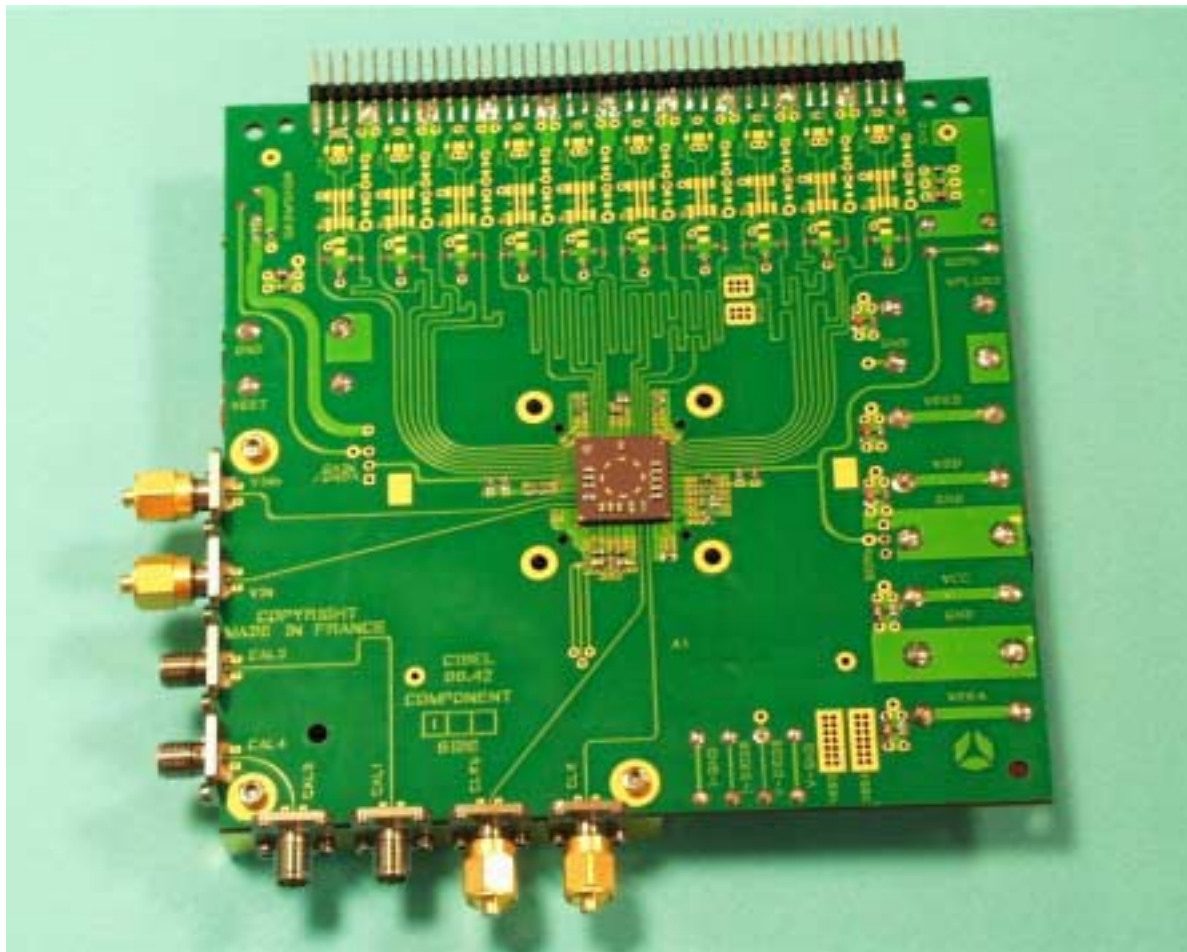
GENERAL DESCRIPTION

The TSEV8308500 Evaluation Board (CEB) is a board which has been designed in order to facilitate the evaluation and the characterization of the TS8308500 device up to its 1.3 GHz full power bandwidth at up to 500 Msps in the commercial temperature range.

The high speed of the TS8308500 requires careful attention to circuit design and layout to achieve optimal performance.

This four metal layer board with internal ground plane has the adequate functions in order to allow a quick and simple evaluation of the TS8308500 ADC performances over the temperature range.

The TSEV8308500 Evaluation Board is very straightforward as it only implements the TS8308500 ADC, SMA connectors for input / output accesses and a 2.54 mm pitch connector compatible with HP16500C high frequency probes.

The board also implements a de–embedding fixture in order to facilitate the evaluation of the high frequency insertion loss of the input microstrip lines, and a die junction temperature measurement setting.
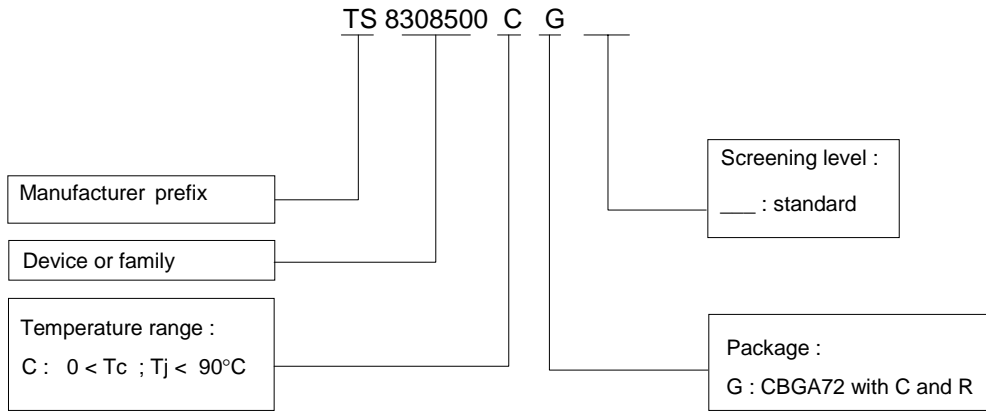
The board is constituted by a sandwich of two dielectric layers, featuring low insertion loss and enhanced thermal characteristics for operation in the high frequency domain and extended temperature range.
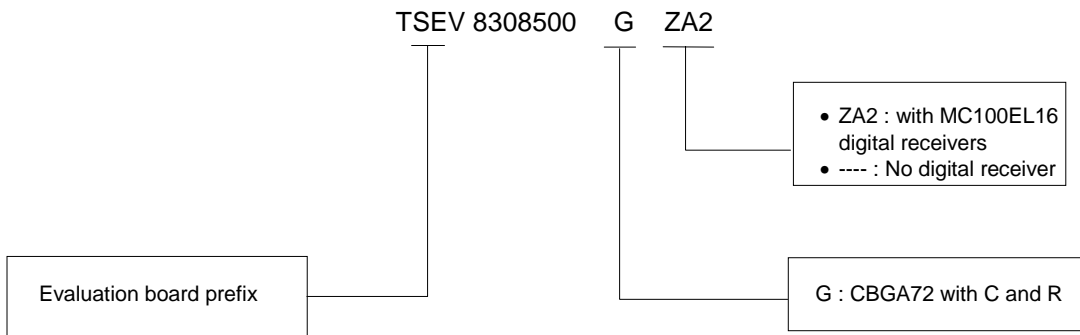
The board dimensions are 130 mm x 130 mm.

The board set comes fully assembled and tested, with the TS8308500 and its heatsink installed.

10. ORDERING INFORMATION

10.1. PACKAGE DEVICE

TS 8308500 C G

Manufacturer prefix

Device or family

Temperature range :
C : 0 < Tc ; Tj < 90°C

Screening level :
___ : standard

Package :
G : CBGA72 with C and R

10.2. EVALUATION BOARD

TSEV 8308500 G ZA2

Evaluation board prefix

- ZA2 : with MC100EL16 digital receivers
- ---- : No digital receiver

G : CBGA72 with C and R

The evaluation board is delivered with an ADC and includes the heat sink.

Atmel Headquarters

Corporate Headquarters

2325 Orchard Parkway
San Jose, CA 95131
TEL (408) 441-0311
FAX (408) 487-2600

Europe

Atmel SarL
Route des Arsenaux 41
Casa Postale 80
CH-1705 Fribourg
Switzerland
TEL (41) 26-426-5555
FAX (41) 26-426-5500

Asia

Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan

Atmel Japan K.K.
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Atmel Colorado Springs

1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Rousset

Zone Industrielle
13106 Rousset Cedex
France
TEL (33) 4-4253-6000
FAX (33) 4-4253-6001

Atmel Smart Card ICs

Scottish Enterprise Technology Park
East Kilbride, Scotland G75 0QR
TEL (44) 1355-357-000
FAX (44) 1355-242-743

Atmel Grenoble

Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex
France
TEL (33) 4-7658-3000
FAX (33) 4-7658-3480

Fax-on-Demand
North America:
1-(800) 292-8635
International:
1-(408) 441-0732

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

BBS
1-(408) 436-4309

This product is manufactured and commercialized by Atmel Grenoble.
For further information, please contact :

Atmel Grenoble – Route Departementale 128 – BP 46 – 91901 Orsay Cedex – France
Phone +33 (0) 1 69 33 03 24 – Fax +33 (0) 1 69 33 03 21
Email monique.lafrique@gfo.atmel.com – Web site http://www.atmel-grenoble.com

For further technical information, please contact the technical support :
Email HOTLINE-BDC@gfo.atmel.com