DATA SHEET

TSA5523M
1.4 GHz I^2C-bus controlled multimedia synthesizer

Product specification
File under Integrated Circuits, IC02

1996 Dec 17

Philips Semiconductors

PHILIPS

1.4 GHz I²C-bus controlled multimedia synthesizer

TSA5523M

FEATURES

- Complete 1.4 GHz single-chip system
- Adaptive DC/DC converter driver output
- On-board tuning amplifier output
- Varicap drive disable
- Four NPN open-collector output ports (10 mA)
- Four bus-controlled bidirectional ports (NPN open-collector outputs)
- In-lock detector
- 5-step Analog-to-Digital Converter (ADC)
- Mixer/Oscillator (M/O) band-switch output
- 15-bit programmable divider
- Programmable reference divider ratio (512, 640 or 1024)
- Programmable charge-pump current (50 or 250 μA)
- I²C-bus format
  - Address plus four data bytes transmission (write mode)
  - Address plus one status byte transmission (read mode)
  - Four independent addresses
- Low power, low radiation.

GENERAL DESCRIPTION

The device is a single chip PLL frequency synthesizer designed for TV and VCR tuning systems. The circuit consists of a divide-by-eight prescaler with its own preamplifier, a 15-bit programmable divider, a crystal oscillator and its programmable reference divider, a phase/frequency detector combined with a charge-pump which drives the tuning amplifier, including 33 V output. Three NPN open-collector outputs are provided for band switching together with five open-collector NPN outputs. Four of these ports can also be used as input ports (one ADC and three general purpose I/O ports).

An output is provided to control a Philips mixer/oscillator IC controlled by bits P7, P5 and P4. Depending on the reference divider ratio (512, 640 or 1024), the phase comparator operates at 3.90625, 6.25 or 7.8125 kHz with a 4 MHz crystal.

The lock detector bit FL is set to logic 1 when the loop is locked and is read on the SDA line (status byte) during a read operation. The ADC is available for digital AFC control. The ADC code is read during a read operation on the I²C-bus. The ADC input is combined with the port P6. In the test mode, this port is also used as a test output for f_{ref} and $f_{div/2}$ (see Table 4). In addition, the circuit includes a DC/DC converter driver connected to the IDC pin to control the amplitude of an external oscillator followed by a voltage rectifier.

The voltage rectifier is used to generate the correct tuning supply voltage to maintain a constant current into the tuning amplifier. The DC/DC converter driver can be disabled by setting the IDC pin to V_{CC1} in this event the tuning supply voltage is delivered by a fixed 33 V supply.

Five serial bytes (including address byte) are required to address the device, select the VCO frequency, program the ports, set the charge-pump current and set the reference divider ratio. The device has four independent I²C-bus addresses which can be selected by applying a specific voltage on the AS input (see Table 3).

APPLICATIONS

- Multimedia TV tuners and front-ends
- VCR tuners.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TSA5523M/C1	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC1}	supply voltage		4.5	–	5.5	V
I_{CC1}	supply current		–	22	30	mA
f_{RF}	RF frequency range		64	–	1400	MHz
V_{iRF}	RF input voltage level	80 to 150 MHz	–25	–	+3	dBm
		150 MHz to 1 GHz	–28	–	+3	dBm
		1 to 1.4 GHz	–26	–	+3	dBm
f_{XTAL}	crystal oscillator frequency		–	4	–	MHz
I_{NPN}	NPN open-collector output current		–	10	15	mA
T_{amb}	operating ambient temperature		–20	–	+85	°C
T_{stg}	IC storage temperature		–40	–	+150	°C

BLOCK DIAGRAM

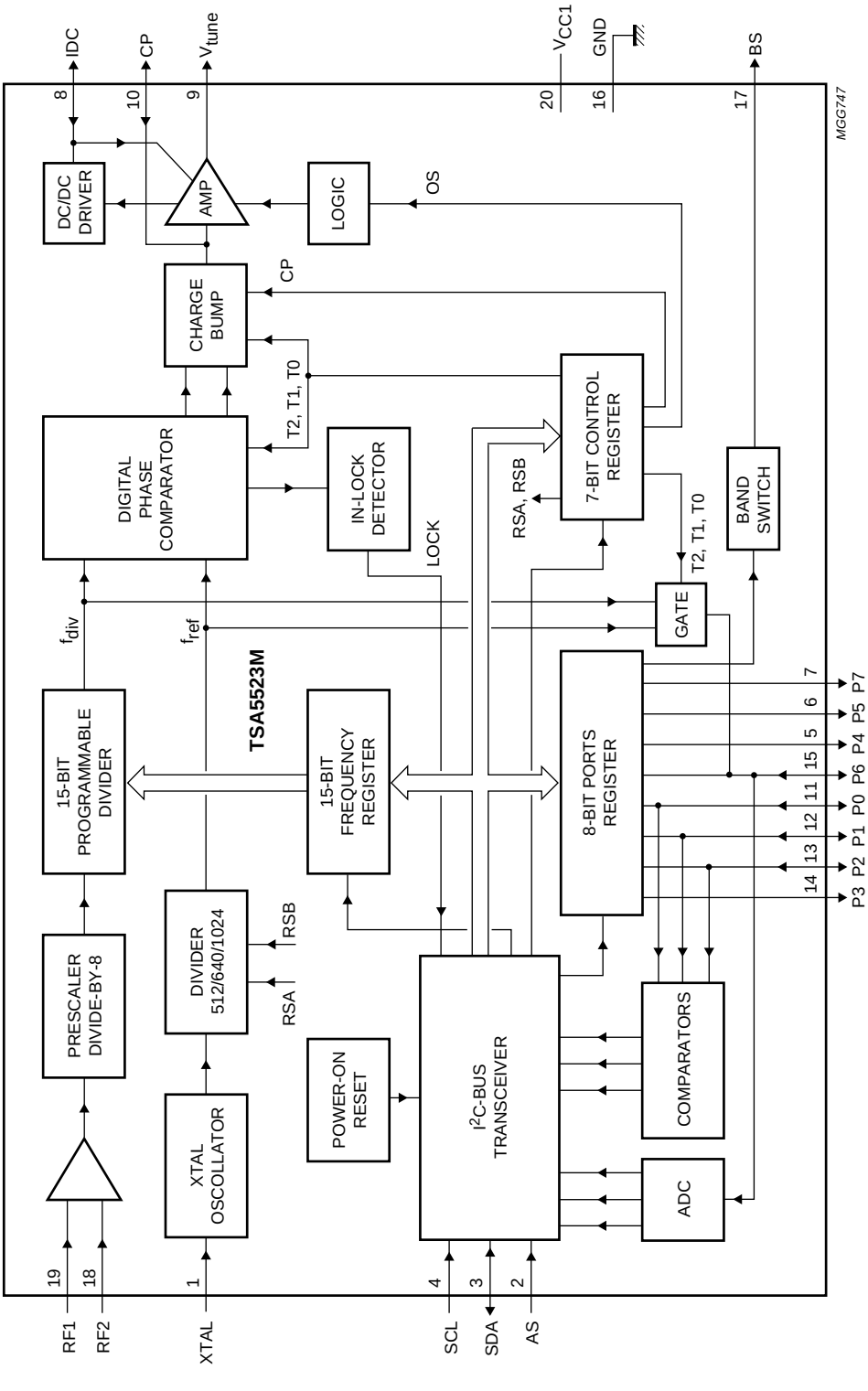


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
XTAL	1	crystal oscillator input
AS	2	address selection input
SDA	3	serial data input/output
SCL	4	serial clock input
P4	5	Port 4 NPN open-collector band-switch output
P5	6	Port 5 NPN open-collector band-switch output
P7	7	Port 7 NPN open-collector band-switch output
IDC	8	DC/DC converter control I/O terminal
V_{tune}	9	tuning voltage output
CP	10	NPN open-collector I/O port
P0	11	Port 0 NPN open-collector I/O port
P1	12	Port 1 NPN open-collector I/O port
P2	13	Port 2 NPN open-collector I/O port
P3	14	Port 3 NPN open-collector output
P6	15	Port 6 NPN open-collector output/ADC input
GND	16	ground
BS	17	band-switch output to mixer/oscillator driver
RF2	18	RF signal input 2
RF1	19	RF signal input 1
V_{CC1}	20	supply voltage (+5 V)

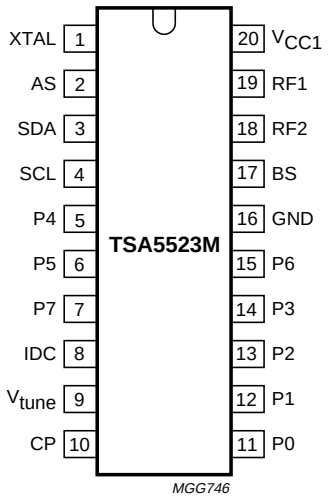


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The device is controlled via the two-wire I²C-bus.
For programming, there is one module address (7 bits) and the R/$\overline{W}$ bit for selecting the read or the write mode.

Write mode: R/$\overline{W}$ = 0 (see Table 1)

After the address transmission (first byte), data bytes can be sent to the device. Four data bytes are needed to fully program the device. The bus transceiver has an auto-increment facility which permits the programming of the device within one single transmission (address + 4 data bytes).

The device can also be partially programmed providing that the first data byte following the address is Divider Byte 1 (DB1) or Control Byte (CB). The meaning of the bits in the data bytes is given in Table 1.

The first bit of the first data byte transmitted indicates whether frequency data (first bit = 0) or control and ports data (first bit = 1) will follow. Until an I²C-bus STOP condition is sent by the controller, additional data bytes can be entered without the need to re-address the device. The frequency register is loaded after the 8th clock pulse of the second Divider Byte (DB2), the control register is loaded after the 8th clock pulse of the control byte and the ports register is loaded after the 8th clock pulse of the Ports Byte (PB).

I²C-bus address selection

The module address contains programmable address bits (MA1 and MA0) which offer the possibility of having several synthesizers (up to 4) in one system by applying a specific voltage to the AS input. The relationship between MA1 and MA0 and the input voltage on the AS input is given in Table 2.

Table 1 I²C-bus data format

DATA BYTES	MSB							LSB	ACK
Address Byte (ADR)	1	1	0	0	0	MA1	MA0	0	A(1)
Divider Byte 1 (DB1)	0	N14	N13	N12	N11	N10	N9	N8	A(1)
Divider Byte 2 (DB2)	N7	N6	N5	N4	N3	N2	N1	N0	A(1)
Control Byte (CB)	1	CP	T2	T1	T0	RSA	RSB	OS	A(1)
Ports Byte (PB)	P7	P6	P5	P4	P3	P2	P1	P0	A(1)

Note

1. A = Acknowledge.

Table 2 Explanation to Table 1

SYMBOL	DESCRIPTION
MA1 and MA0	programmable address bits (see Table 3)
N14 to N0	programmable divider bits N = N14 × 2^{14} + 2^{13} + ... + N1 × 2 + N0
CP	charge-pump current
CP = 0	50 μA
CP = 1	250 μA
T2, T1 and T0	test bits; normal operation; T2 = 0, T1 = 0, T0 = 1 (see Table 4)
RSA and RSB	reference divider ratio select bits (see Table 5)
OS	tuning amplifier control bit
OS = 0	normal operation; tuning voltage is ON
OS = 1	tuning voltage is OFF (high impedance), IDC output voltage is LOW
P7 to P0	NPN open-collector control bits
Pn = 0	output n is OFF
Pn = 1	output n is ON

Table 3 Address selection

INPUT VOLTAGE APPLIED TO PIN AS	MA1	MA0
0 V to $0.1V_{CC1}$	0	0
open-circuit or $0.2V_{CC1}$ to $0.3V_{CC1}$	0	1
$0.4V_{CC1}$ to $0.6V_{CC1}$	1	0
$0.9V_{CC1}$ to V_{CC1}	1	1

Table 4 Test bits

T2	T1	T0	DEVICE OPERATION
0	0	1	normal mode
0	1	X	charge-pump is OFF
1	1	0	charge-pump is sinking current
1	1	1	charge-pump is sourcing current
1	0	0	f_{ref} is available on P6 output
1	0	1	$f_{div/2}$ is available on P6 output

Table 5 Ratio select bits

RSA	RSB	REFERENCE DIVIDER
X	0	640
0	1	1024
1	1	512

Table 6 Band-switch output levels

P7	P5	P4	OUTPUT VOLTAGE ON PIN BS	PHILIPS M/O IC's BAND
1	1	0	0.25 V	band A
1	0	1	$0.4V_{CC1}$	band B
0	1	1	$0.8V_{CC1}$	band C
1	1	1	V_{CC1}	band C
all other codes			V_{CC1}	band C

Read mode: R/$\overline{W}$ = 1 (see Table 7)

Data can be read out of the device by setting the R/$\overline{W}$ bit to logic 1. After the slave address has been recognized, the device generates an acknowledge pulse and the first data byte (status byte) is transferred on the SDA line (MSB first). Data is valid on the SDA line during a HIGH level of the SCL clock signal. A second data byte can be read out of the device if the processor generates an acknowledge on the SDA line (master acknowledge).

End of transmission will occur if no master acknowledge occurs. The device will then release the data line to allow the processor to generate a STOP condition. When Ports P0 to P2 are used as inputs, the corresponding bits **must** be logic 0 (high-impedance state). The Power-On Reset flag (POR) is set to logic 1 at power-on. It is reset when an end-of-data is detected by the device (end of a read sequence). Control of the loop is made possible with the in-lock flag FL (FL = 1) which indicates when the loop is locked. The bits I2, I1 and I0 represent the status of the I/O Ports P2, P1 and P0 respectively.

A logic 0 indicates a LOW level and a logic 1 indicates a HIGH level (see threshold level in the "Characteristics"). A built-in ADC is available on pin P6. This converter can be used to feed AFC information to the controller from the IF section of the television. The relationship between bits A2, A1 and A0 is given in Table 9.

At power-on, the device is reset as follows: all ports are set to the high-impedance state, except P4, P5 and P7 which are set to logic 1. The tuning amplifier is in the high-impedance state (OS = 1). The POR level is fixed to $3 \times V_{BE}$ (2.1 V typ.). If V_{CC1} goes below the POR level the circuit is reset.

Table 7 Read data format

BYTE	MSB (1)							LSB	ACK
Address Byte (ADB)	1	1	0	0	0	MA1	MA0	1	A(2)
Status Byte (SB)	POR	FL	I2	I1	I0	A2	A1	A0	–

Notes

1. MSB is transmitted first.
2. A: Acknowledge.

Table 8 Explanation to Table 7

SYMBOL	DESCRIPTION
POR	power-on reset flag (POR = 1 at power-on)
FL	in-lock flag (FL = 1 when the loop is phase-locked)
I2, I1 and I0	digital levels for I/O ports P2, P1 and P0 respectively
A2, A1 and A0	digital outputs of the 5-level ADC

Table 9 Analog-to-digital converter levels; note 1

VOLTAGE APPLIED ON PORT P6	A2	A1	A0
$0.6V_{CC1}$ to V_{CC1}	1	0	0
$0.45V_{CC1}$ to $0.6V_{CC1}$	0	1	1
$0.3V_{CC1}$ to $0.45V_{CC1}$	0	1	0
$0.15V_{CC1}$ to $0.3V_{CC1}$	0	0	1
0 to $0.15V_{CC1}$	0	0	0

Note

1. Accuracy is $0.03V_{CC1}$.

LIMITING VALUES

In according with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{iRF}	prescaler input voltage		–0.3	V_{CC1}	V
V_{CC1}	supply voltage (+5 V)		–0.3	+6	V
V_{oIDC}	IDC output voltage		–0.3	V_{CC1}	V
V_{oNPN}	NPN open-collector output voltage		–0.3	+16	V
I_{oNPN}	NPN open-collector output current		–1	+15	mA
V_{oCP}	charge-pump output voltage		–0.3	V_{CC1}	V
$V_{o(tune)}$	tuning voltage output	see Fig.3	–0.3	+40	V
V_{oBS}	band-switch output voltage		–0.3	V_{CC1}	V
V_{iSCL}	serial clock input voltage		–0.3	+6	V
$V_{i/oSDA}$	serial data input/output voltage		–0.3	+6	V
I_{oSDA}	data output current		–1	+5	mA
V_{iAS}	address selection input voltage		–0.3	V_{CC1}	V
V_{iXTAL}	crystal input voltage		–0.3	V_{CC1}	V
T_{stg}	IC storage temperature		–40	+150	°C
$T_{j(max)}$	maximum junction temperature		–	+150	°C
t_{sc}	short-circuit time every pin to V_{CC1} or GND		–	10	s

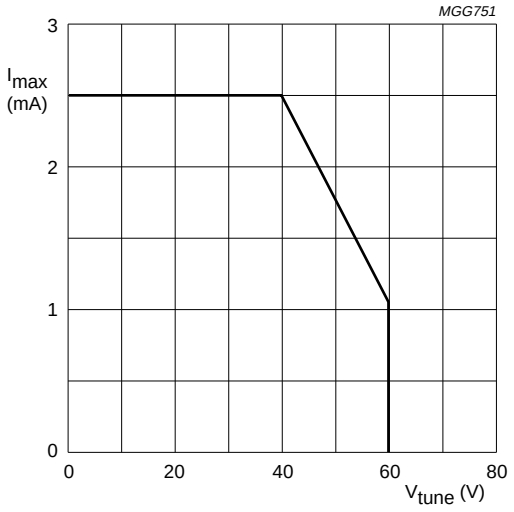


Fig.3 Rating power on V_{tune} output pin.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling bipolar devices.
Every pin withstands the ESD test in accordance with *"MIL-STD-883C* category B*"* (2000 V).
Every pin withstands the EDS test in accordance with Philips Semiconductors Machine Model 0 Ω, 200 pF (200 V).

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

CHARACTERISTICS

V_{CC1} = 4.5 to 5.5 V; T_{amb} = –20 to +85 °C; see note 1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
General						
V_{CC1}	supply voltage		4.5	–	5.5	V
I_{CC1}	supply current	V_{CC1} = 5 V	–	22	30	mA
V_{PORth}	power-on reset threshold voltage	T_{amb} = 25 °C slope is –6 mV/°C	1.5	2.0	–	V
T_{amb}	operating ambient temperature		–20	–	+85	°C
f_{iRF}	RF input frequency		64	–	1400	MHz
N	divider ratio	15-bit frequency word	256	–	32767	–
XTAL oscillator						
f_{XTAL}	frequency range	R_{XTAL} = 25 to 200 Ω	3.2	4.0	4.48	MHz
Z_{XTAL}	input impedance	f = 4 MHz	600	1200	–	Ω
$DL_{XTAL(p\text{-}p)}$	drive level on pin XTAL (peak-to-peak value)	series capacitor = 18 pF; crystal Philips 4333 1430 4881	–	110	–	mV
Prescaler						
V_{RFin}	input level	V_{CC1} = 4.5 to 5.5 V; T_{amb} = –20 to +85 °C; see Fig.4				
		f = 80 to 150 MHz	–25	–	+3	dBm
		f = 150 to 1000 MHz	–28	–	+3	dBm
		f = 1000 to 1400 MHz	–26	–	+3	dBm
Z_{iRF}	input impedance	see Fig.5	–	–	–	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
NPN open-collector outputs P7 to P0; note 2						
I_{LI}	leakage current	V_{CC1} = 5.5 V; V_o = 13.5 V	–	–	10	µA
	leakage current P4, P5, P7	V_{CC1} = 5.5 V; V_o = 1.5 V	–	–	1	µA
V_{cesatN}	output saturation voltage on Ports P4, P5 and P7	I_{sink} = 100 µA	–	–	0.2	V
	output saturation voltage	I_{sink} = 10 mA	–	0.2	0.4	V
		I_{sink} = 2 mA	–	0.2	0.3	V
C_{Pn}	allowed capacitive loading on output pins	V_{Pn} = 5.5 V	–	–	10	nF
Input ports P2, P1 and P0; note 3						
V_{IL}	LOW level input voltage		–	–	1.5	V
V_{IH}	HIGH level input voltage		3	–	–	V
I_{IL}	LOW level input current	V_i = 0 V	–10	–	–	µA
I_{IH}	HIGH level input current	V_{CC1} = 5.5 V; V_o = 13.5 V	–	–	10	µA
AS input (Address Selection)						
I_{IH}	HIGH level input current	$V_{IH} = V_{CC1}$	–	–	50	µA
I_{IL}	LOW level input current	V_{IL} = 0 V	–50	–	–	µA
SCL and SDA inputs						
V_{IL}	LOW level input voltage		–	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	5.5	V
I_{IH}	HIGH level input current	V_{IH} = 5.5 V; V_{CC1} = 0 V	–	–	10	µA
		V_{IH} = 5.5 V; V_{CC1} = 5.5 V	–	–	10	µA
I_{IL}	LOW level input current	V_{IL} = 0 V; V_{CC1} = 5.5 V	–10	–	–	µA
f_{CLK}	clock frequency		–	100	400	kHz
SDA output (I²C-bus mode)						
I_{LI}	leakage current	V_{SDA} = 5.5 V	–	–	10	µA
V_{oSDA}	output voltage	I_{sink} = 3 mA	–	–	0.4	V
BS output (mixer/oscillator IC band selection)						
V_{oBSA}	output voltage for band A	I_L = 20 µA	–	0.25	0.5	V
V_{oBSB}	output voltage for band B	I_L = 20 µA	$0.36V_{CC1}$	$0.4V_{CC1}$	$0.43V_{CC1}$	V
V_{oBSC}	output voltage for band C	I_L = 20 µA	$0.7V_{CC1}$	$0.8V_{CC1}$	$0.9V_{CC1}$	V
		I_L = 50 µA	3.1	–	–	V
IDC output						
V_{IDCoff}	voltage to switch-off DC/DC converter driver		V_{CC1} – 0.5	–	V_{CC1}	V
I_{oIDC}	IDC output current	R_{ext} = 100 kΩ	–10	–	+100	µA
G_t	transfer gain	I_9 = 100 µA	–	1000	–	µA/V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Charge-pump output CP						
$\|I_{IH}\|$	HIGH level input current (absolute value)	CP = 1	–	250	–	µA
$\|I_{IL}\|$	LOW level input current (absolute value)	CP = 0	–	50	–	µA
V_{oCP}	output voltage	in-lock; T_{amb} = 25 °C	–	1.95	–	V
I_{LIos}	off-state leakage current	T2 = 0; T1 = 1	–5	+1	+15	nA
Tuning voltage output; V_{tune}						
$I_{9(off)}$	leakage current when switched-off	OS = 1; V_{tune} = 33 V	–	–	10	µA
V_{o9}	output voltage when the loop is closed	OS = 0; T2 = 0; T1 = 0; T0 = 1; R_L = 27 kΩ; V_{tune} = 33 V	0.3	–	32.7	V
I_{bias}	tuning amplifier bias current	DC/DC converter loop is active	70	100	130	µA
$V_{ripple(p-p)}$	acceptable ripple voltage on V_{CC1} (peak-to-peak value)	f_{ripple} = 20 Hz to 500 kHz; note 4	–	–	30	mV

Notes

1. When a port is active, the collector voltage must not exceed 6 V.
2. All other ports are switched ON with 10 mA during test.
3. When a port is used as input port, the corresponding bit must be programmed to the high-impedance state.
4. FM deviation is 2 kHz (max).

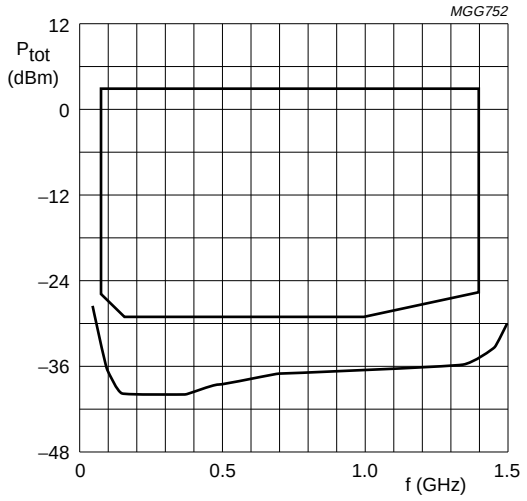


Fig.4 Prescaler typical input sensitivity curve (pin 2).

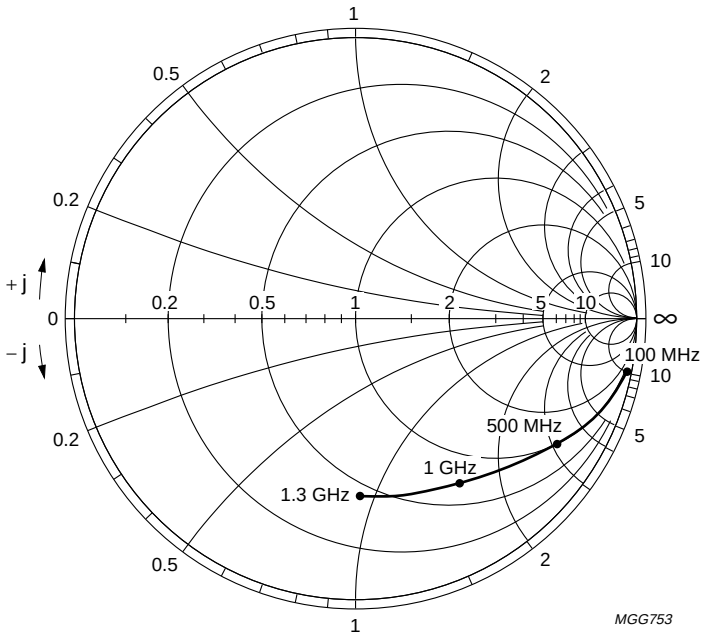


Fig.5 Prescaler Smith chart (S11) of typical input impedance (Z_L = 50 Ω; pin 2).

APPLICATION INFORMATION

Tuning amplifier

The tuning amplifier is able to drive the varicap voltage without an external transistor. The V_{tune} output must be connected to an external load of 27 kΩ connected to the tuning voltage supply. Figures 6 and 7 illustrate a possible loop filter. The component values depend on the oscillator characteristics and the selected reference frequency.

Crystal oscillator

The crystal oscillator uses a 4.0 MHz crystal in series with an 18 pF capacitor. The crystal operates in the series resonance mode. The connection to V_{CC1} is preferred, but it can also be connected to GND.

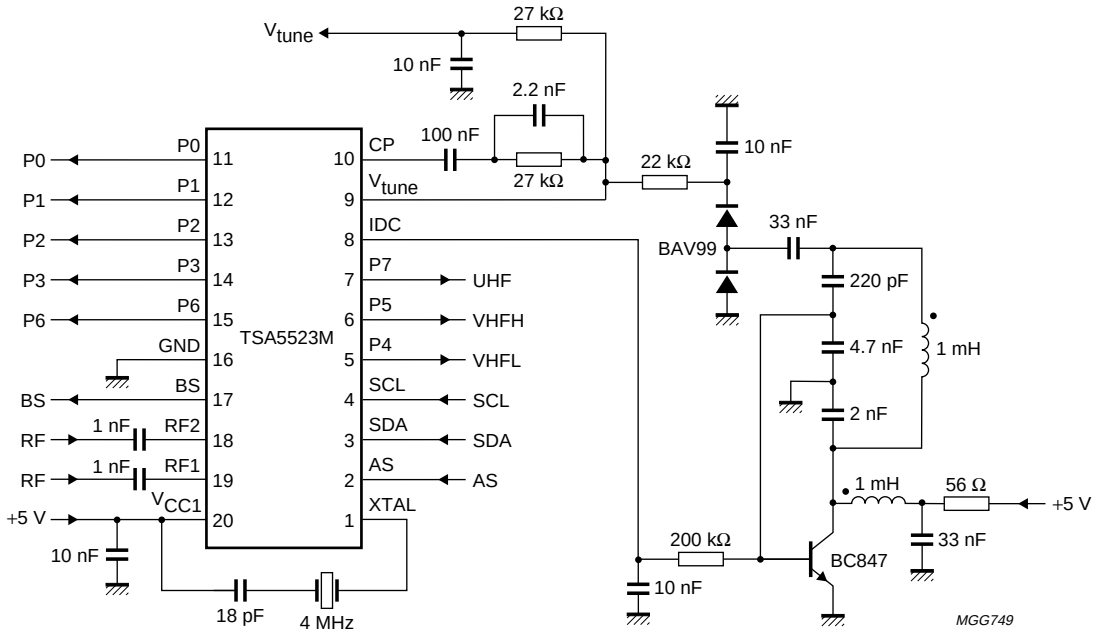


Fig.6 Typical application with DC/DC converter.

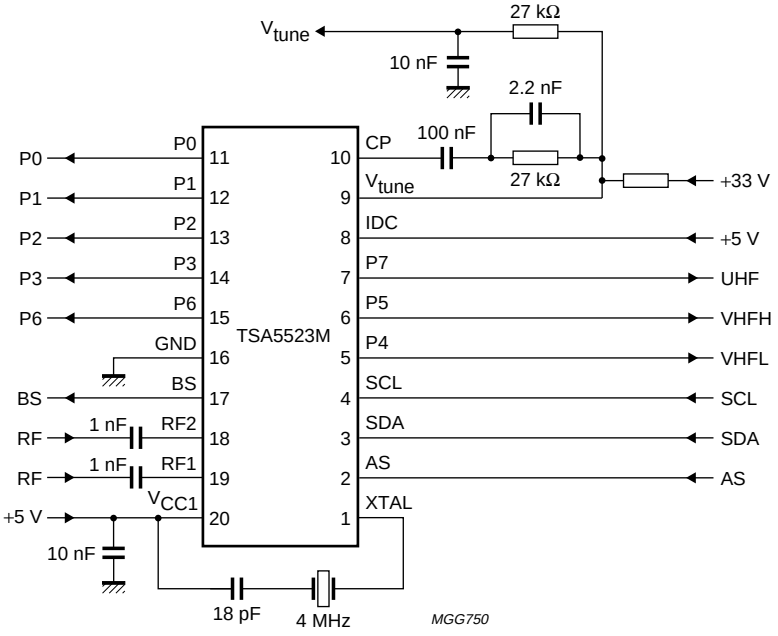


Fig.7 Standard application.

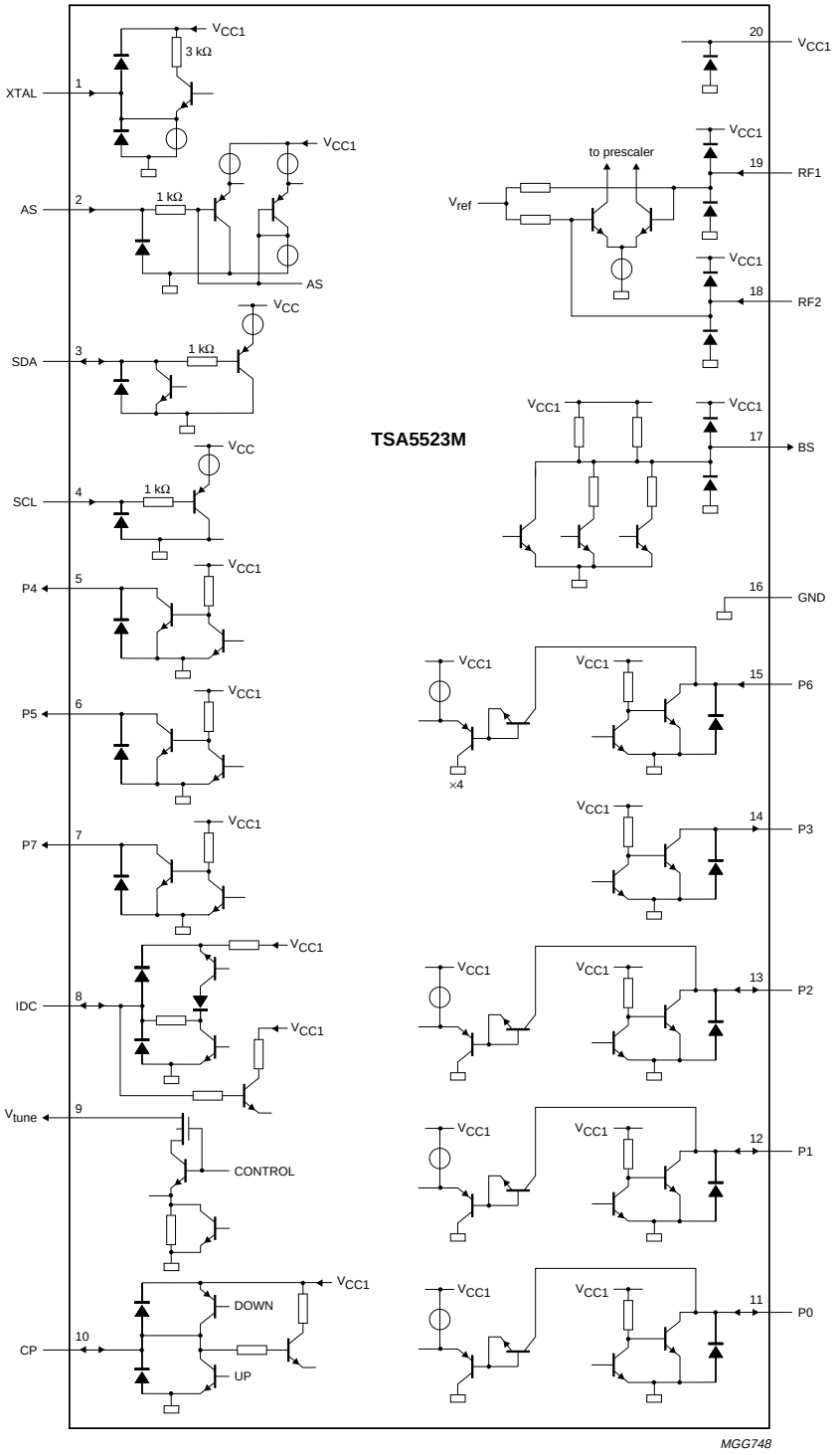
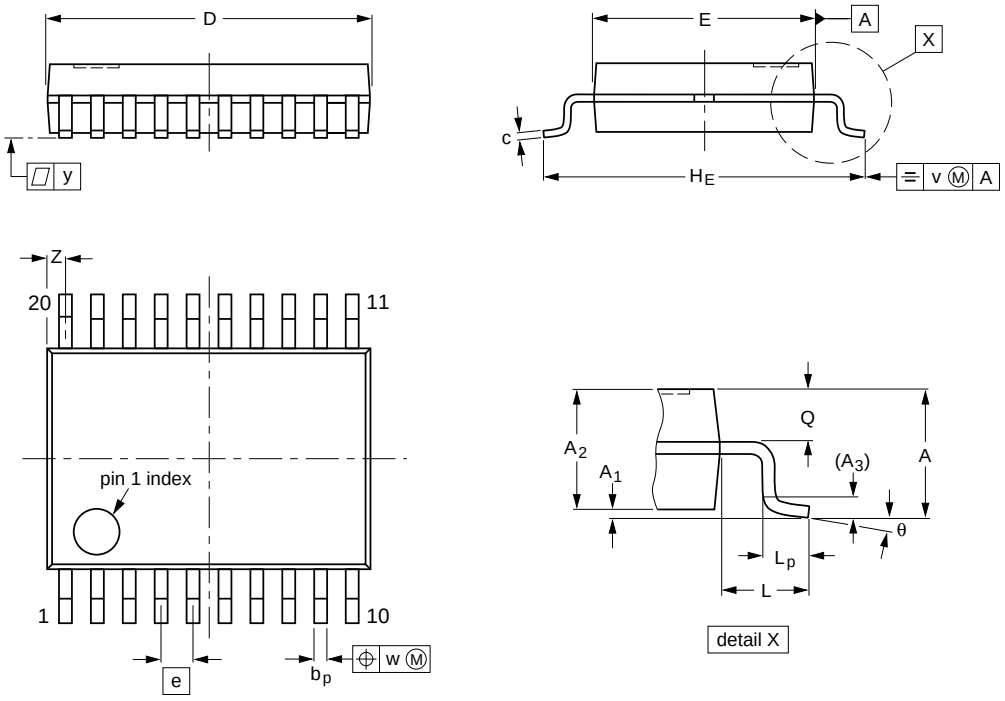
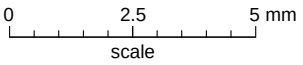


Fig.8 Input/output pin schematic.

PACKAGE OUTLINE

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm **SOT266-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0	1.4 1.2	0.25	0.32 0.20	0.20 0.13	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT266-1							~~90-04-05~~ 95-02-25

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for SSOP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.**

Even with these conditions, only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 1949

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580/xxx

France: 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Shivsagar Estate, A Block, Dr. Annie Besant Rd.
Worli, MUMBAI 400 018, Tel. +91 22 4938 541, Fax. +91 22 4938 722

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, TEL AVIV 61180,
Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 247 9145, Fax. +7 095 247 9144

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Rua do Rocio 220, 5th floor, Suite 51,
04552-903 São Paulo, SÃO PAULO - SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 829 1849

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 632 2000, Fax. +46 8 632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2686, Fax. +41 1 481 7730

Taiwan: PHILIPS TAIWAN Ltd., 23-30F, 66,
Chung Hsiao West Road, Sec. 1, P.O. Box 22978,
TAIPEI 100, Tel. +886 2 382 4443, Fax. +886 2 382 4444

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 625 344, Fax.+381 11 635 777

For all other countries apply to: Philips Semiconductors, Marketing & Sales Communications,
Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: http://www.semiconductors.philips.com

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