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TSB42AA4
TSB42AA4I
TSB42AB4, TSB42AB4I
SLLA217−JUNE 2006

(ceLynx) IEEE 1394-a Consumer Electronics Link Layer Controller

FEATURES

- **DTCP content protection (TSB42AA4 only). A separate document explains the DTCP hardware errata for TSB42AA4. It is available upon request to DTLA licensees only.**
- **Interfaces directly to industry standard 400-, 200-, and 100-Mbps physical layer devices, including Texas Instruments TSB41LV0X and TSB41AXX family of physical layer devices**
- **Compliant with IEEE 1394-1995 and IEEE 1394a–2000 standards**
- **MPEG2 time stamp-based release, as described in IEC 61883-4**
- **High-speed data interface (HSDI):**
  - **Byte-wide or serial mode**
  - **Two independent HSDI ports**
  - **Bidirectional**
  - **Several control modes for a variety of applications**
  - **Connects seamlessly to common MPEG2 decoder chipsets**
- **16-bit microprocessor interface supports Motorola 68000/68020-style bus**
- **Large 8K-byte FIFO can be configured up to eight independent Tx or Rx FIFOs**

- **8K-byte FIFO supports the following data types:**
  - **DVB MPEG2 transport streams (IEC 61883-4)**
  - **DirecTV™ transport streams**
  - **DV program streams (IEC 61883-2)**
  - **Asynchronous streams**
  - **Support for external processor DMA**
- **Programmable data-/space-available indications for flow control; *almost full* and *almost empty* indicators**
- **Supports bus manager functions and automatic 1394 self-ID verification**
- **Interrupt driven to minimize host polling**
- **Single 3.3-V supply**
- **Separate async acknowledge buffer decreases the ack-tracking burden on host**
- **JTAG interface to support post-assembly scan of device I/O**
- **Bus holder isolation**
- **Embedded support for DTCP content protection:**
  - **Two M6 baseline ciphers (one per HSDI port)**
  - **Random number generator in hardware**
  - **SHA-1 secure hash algorithm in hardware**
  - **Authentication key cipher in hardware**
- **Optional auto-configuration for MPEG2/DV transmit and receive functions**
- **PID filtering and packet insertion for MPEG2 transport stream**

DESCRIPTION

Consumer Electronics Link (ceLynx) is a high-performance 1394 link layer device designed specifically to support advanced consumer electronics applications, particularly those applications which require the transmission of Moving Picture Expert Group 2 (MPEG2) transport streams and encryption/decryption of those streams across a 1394 network. The device supports both digital video broadcasting (DVB) and DirecTV™ type MPEG2 streams using the digital transmission content protection method (DTCP) method of encryption, as well as digital video (DV) encoded streams. The ceLynx supports both the IEC 61883 standard for DVB and DV streams over 1394 and the 1394 Trade Association standard for DirecTV over 1394.

The ceLynx is also versatile enough to handle asynchronous data and asynchronous streams. A key feature of the ceLynx is its ability to handle multiple data type streams simultaneously; the user may transport DVB, DirecTV, DV data streams, and asynchronous data *simultaneously*. The ceLynx can also support multiple streams of the same data type simultaneously, (for example, transmit or receive two DVB transport streams or two DV streams).

The ceLynx is full duplex, allowing simultaneous playback and recording of audio/video data. Full duplex support also includes the capability of using the DTCP method, simultaneously using the two embedded M6 cipher modules. The large internal 8-Kbyte FIFO is very flexible, allowing the user to partition it into eight independent first in first out (FIFOs) and allowing the user to determine the exact configuration of each of these FIFOs to fit the application. Advanced features have been added to support program ID (PID) filtering and packet insertions.

The ceLynx is also designed to interface seamlessly with popular MPEG2 decoder chipsets. This decreases the design-in effort of customers when using these popular chipsets.

NOTE:

This product is for high-volume CE applications only. For a complete datasheet or more information contact support@ti.com.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TSB42AA4IPDT	OBSOLETE	TQFP	PDT	128		TBD	Call TI	Call TI	
TSB42AB4PDT	ACTIVE	TQFP	PDT	128	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
TSB42AB4PDTG4	ACTIVE	TQFP	PDT	128	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)
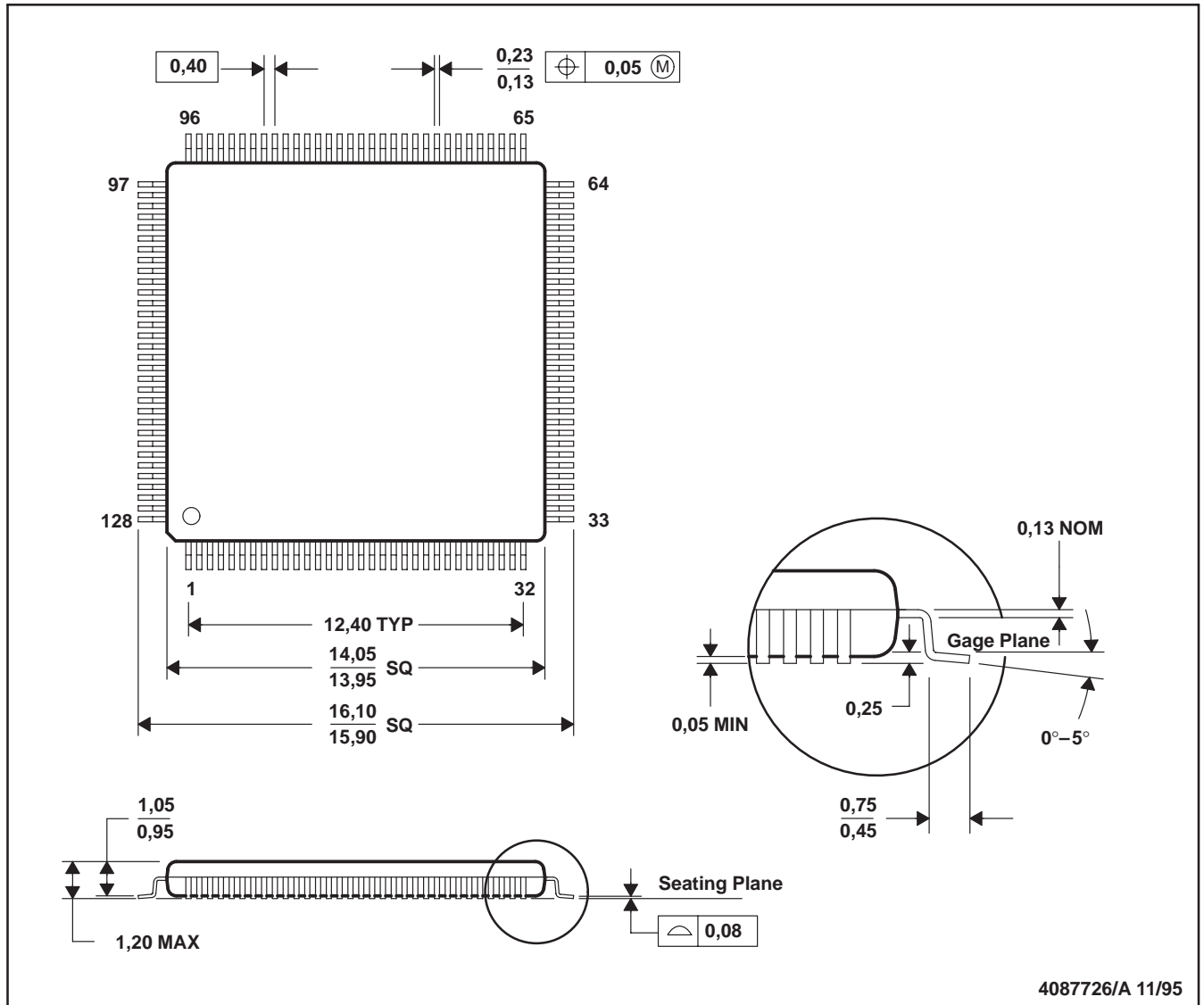
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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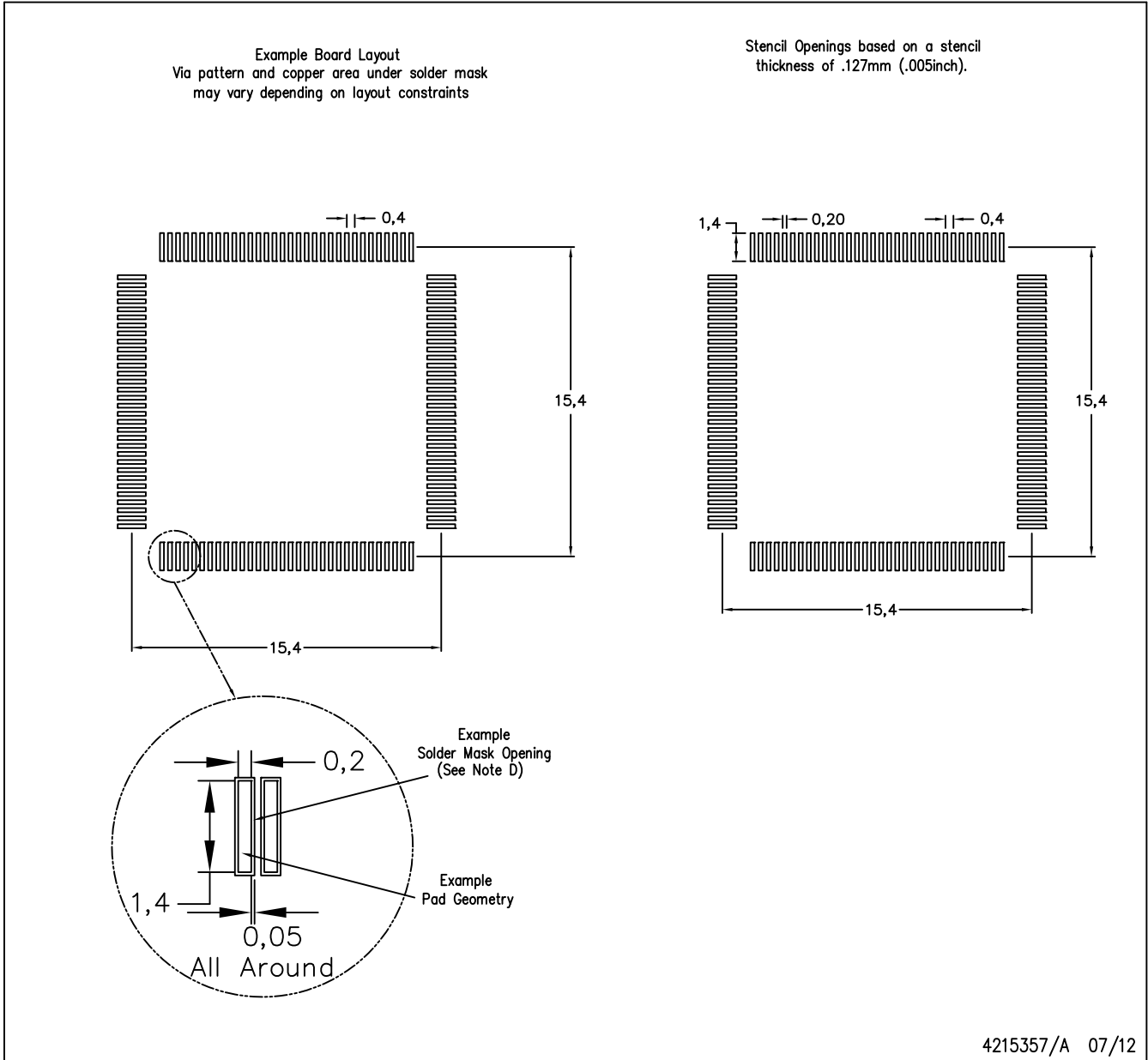**PDT (S-PQFP-G128)**   **PLASTIC QUAD FLATPACK**

0,40	$\dfrac{0,23}{0,13}$ ⊕ 0,05 Ⓜ

96   65

97   64

128   33

1   32

12,40 TYP

$\dfrac{14,05}{13,95}$ SQ

$\dfrac{16,10}{15,90}$ SQ

$\dfrac{1,05}{0,95}$

0,05 MIN

0,25

0,75 / 0,45 → $\dfrac{0,75}{0,45}$

0,13 NOM

Gage Plane

0°−5°

1,20 MAX

Seating Plane

△ 0,08

4087726/A 11/95

NOTES: A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.

PDT (S−PQFP−G128)   PLASTIC QUAD FLAT PACK

Example Board Layout
Via pattern and copper area under solder mask
may vary depending on layout constraints

Stencil Openings based on a stencil
thickness of .127mm (.005inch).

0,4

15,4

15,4

1,4

0,20

0,4

15,4

15,4

15,4

Example
Solder Mask Opening
(See Note D)

0,2

1,4

Example
Pad Geometry

0,05
All Around

4215357/A 07/12

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.
             Customers should contact their board assembly site for stencil design recommendations. Example stencil
             metal load solder paste. Refer to IPC−7525 for other stencil recommendations.
         D. Customers should contact their board fabrication site for solder mask tolerances between and
             around signal pads.

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