CMOS Single chip 8–bit Microcontroller with CAN Controller

Description

The TSC8051A11 is a stand-alone, high performance CMOS microcontroller designed for use in automotive and industrial applications.

The TSC80A11 retains all features of the TSC80C51 with extended EPROM capacity (24K bytes), 256 bytes of internal RAM, a 14-source 2-level interrupt, a full duplex serial port, an on-chip oscillator, and two 16 bits timers.
In addition, the TSC8051A11 has an 8-bit 8-channel A/D converter, a serial synchronous port compatible with SPI and mWire protocols, an advanced 8 channels CCU (Capture & Compare Unit), an additional on-chip XRAM of 256 bytes, a high security Watchdog timer with an embedded oscillator and a CAN network line controller.

The CAN controller is fully compliant with the BOSCH CAN standard rev 2.0 part B. It implements all features of a full CAN controller able to handle all frames of the protocol with 14 predefined messages (channels). It includes 14 sets of channel registers. Each channel has its own identifier tag, its own identifier mask and up to 8 bytes (mailbox) to store the received and transmitted message.

The fully static design of the TSC8051A11 allows to reduce system power consumption by bringing the clock frequency down to any value, even DC, without loss of data.
The design is done with a specific care to reduce EMC emission and susceptibility.

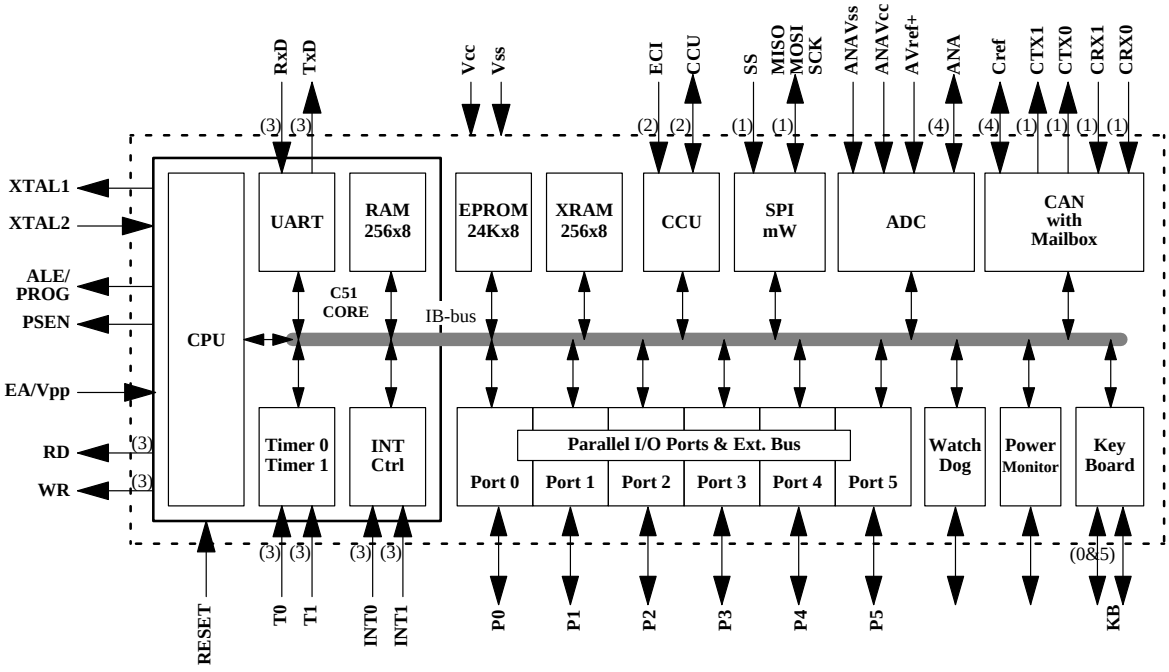
This circuit is manufactured using SCMOS process and is available in commercial, industrial, military and automotive ranges: it runs from 0 up to 20 MHz in the automotive temperature range -40°C to +125°C.

Features

- 80C51 core architecture:
  - 256 bytes of RAM
  - 256 bytes of XRAM
  - 24 Kilobytes of EPROM, OTP or ROM
  - 14-source 2-level interrupt
  - Two 16-bit timer/counter
  - Full duplex UART compatible with standard 80C51 with its own baud rate generator
- 6 8-bit 80C51 I/O Ports bit to bit configurable
- 2 ports with programmable interrupt for keyboard function
- A 8 channels 16-bit CCU with:
  - Rising and/or falling edge capture (pulse measurement capability)
  - Software timer, high speed output and multiple PWM shapes
- A 8-bit resolution analog to digital converter with 8 multiple inputs
- An high security watch-dog timer with an embedded oscillator
- A master/slave synchronous serial peripheral interface (SPI or mWire)
- Full CAN controller:
  - Fully compliant with CAN standard rev 2.0 A and 2.0 B
  - Optimized structure for communication management
  - 14 channels with individual tag and mask filters on 29 identifier-bit
  - Line wake-up capability
  - Automatic reply mode
  - 1 Mbit/s maximum transfer rate
  - Integrated line interface circuitry (output drivers, input comparators, Vcc/2 generator)
- Several power reduction modes with enhanced wake-up capabilities
- PQFP64 or PLCC68 packages

Preview

Block Diagram



(1): Alternate function of Port 1 (2): Alternate function of Port 2 (3): Alternate function of Port 3 (4): Alternate function of Port 4

Figure 1. TSC8051A11 block diagram

Pin-Out

Pin Functions

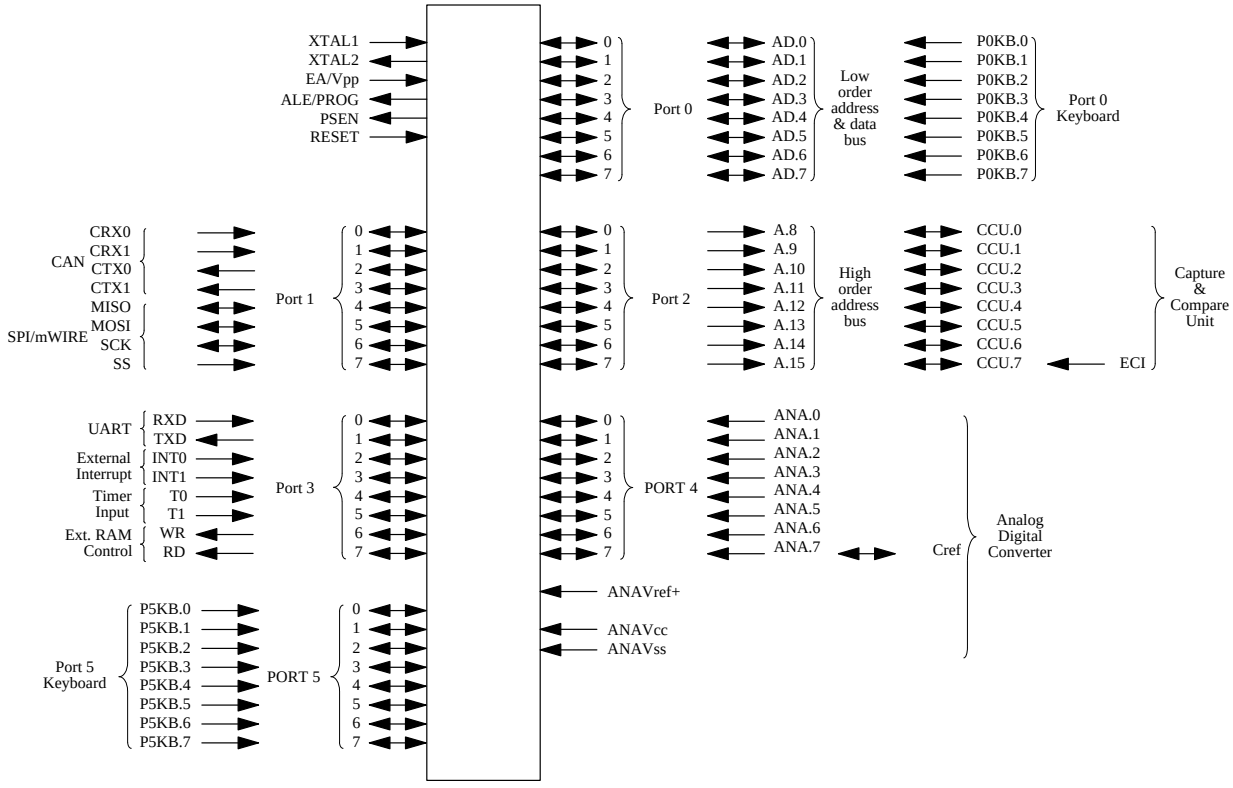


Figure 2. TSC8051A11 pin functions

Pin Configuration

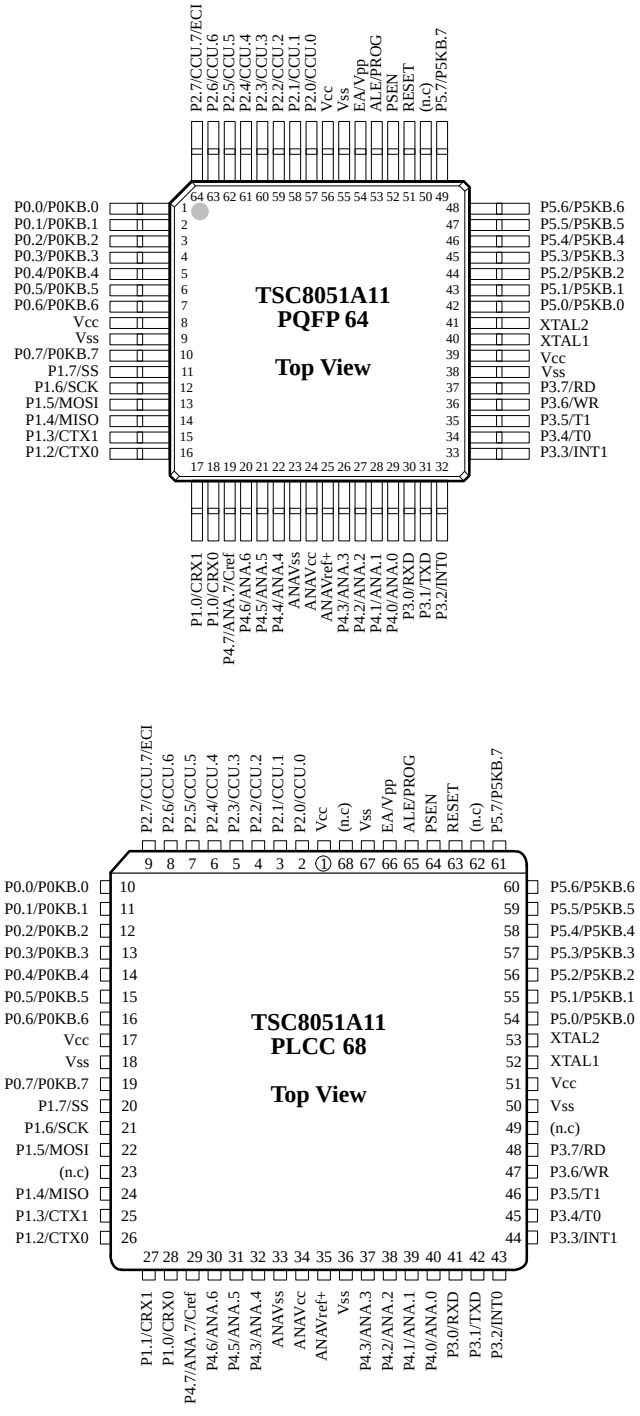


Figure 3. TSC8051A11 pin configuration

Pin Assignment

Table 2. Pin assignment

Pin number		Pin name	Alternate function	Pin number		Pin Name	Alternate function
PQFP 64	PLCC 68			PQFP 64	PLCC 68		
1	10	P0.0	AD.0 / P0KB.0	33	44	P3.3	$\overline{INT1}$
2	11	P0.1	AD.1 / P0KB.1	34	45	P3.4	T0
3	12	P0.2	AD.2 / P0KB.2	35	46	P3.5	T1
4	13	P0.3	AD.3 / P0KB.3	36	47	P3.6	$\overline{WR}$
5	14	P0.4	AD.4 / P0KB.4	37	48	P3.7	RD
6	15	P0.5	AD.5 / P0KB.5		49	(n.c)	-
7	16	P0.6	AD.6 / P0KB.6	38	50	Vss	-
8	17	Vcc	-	39	51	Vcc	-
9	18	Vss	-	40	52	XTAL1	-
10	19	P0.7	AD.7 / P0KB.7	41	53	XTAL2	-
11	20	P1.7	SS	42	54	P5.0	P5KB.0
12	21	P1.6	SCK	43	55	P5.1	P5KB.1
13	22	P1.5	MOSI	44	56	P5.2	P5KB.2
	23	(n.c)		45	57	P5.3	P5KB.3
14	24	P1.2	MISO	46	58	P5.4	P5KB.4
15	25	P1.3	CTX1	47	59	P5.5	P5KB.5
16	26	P1.2	CTX0	48	60	P5.6	P5KB.6
17	27	P1.1	CRX1	49	61	P5.7	P5KB.7
18	28	P1.0	CRX0	50	62	(n.c)	
19	29	P4.7	ANA.7 / Cref	51	63	RESET	-
20	30	P4.6	ANA.6	52	64	PSEN	-
21	31	P4.5	ANA.5	53	65	ALE/$\overline{PROG}$	-
22	32	P4.4	ANA.4	54	66	$\overline{EA}$ / Vpp	-
23	33	ANAVss	-	55	67	Vss	-
24	34	ANAVcc	-		68	(n.c)	
25	35	ANAref+	-	56	1	Vcc	-
	36	Vss	-	57	2	P2.0	A.8 / CCU.0
26	37	P4.3	ANA.3	58	3	P2.1	A.9 / CCU.1
27	38	P4.2	ANA.2	59	4	P2.2	A.10 / CCU.2
28	39	P4.1	ANA.1	60	5	P2.3	A.11 / CCU.3
29	40	P4.0	ANA.0	61	6	P2.4	A.12 / CCU.4
30	41	P3.0	RXD	62	7	P2.5	A.13 / CCU.5
31	42	P3.1	TXD	63	8	P2.6	A.14 / CCU.6
32	43	P3.2	INT0	64	9	P2.7	A.15 / CCU.7 / ECI

General Signal Description

Vss

Digital ground

Vcc

Digital supply voltage

ANAVss

Analog ground

ANAVcc

Analog supply voltage

$\overline{EA}$ / Vpp

External Access enable must be strapped to Vss in order to enable any device plugged on port 0 / port 2 to fetch code from 0 up to 24K. $\overline{EA}$ must be strapped to Vcc for internal program execution.
This pin also receives the 12V programming supply (Vpp input) to program the internal EPROM.

XTAL2

It is the output from the inverting oscillator amplifier.

$\overline{RESET}$

An active level (low) on this pin, while the oscillator is running, resets the device. An internal pull-up resistor permits power-on reset only using only an capacitor connected to Vss.
The active level of the $\overline{RESET}$ pin is the opposite to the one of C51 standard.

ALE / $\overline{PROG}$

The Address Latch Enable output signal is used to latch the low order byte of the address during accesses to external memory. ALE can sink and source 8 LS TTL loads.
If desired, ALE buffer can be disable. Then, ALE is pulled low.
This pin is also used (program pulse input) to program the internal EPROM.

$\overline{PSEN}$

Program Store Enable is the read strobe to external program memory, else it remains high. $\overline{PSEN}$ can sink and source 8 LS TTL loads.

PORT 0

Port 0 can act the part of address/data bus or standard I/O port.
Its dedicated alternate function is a 8-bit keyboard interface.
In the default configuration, port 0 operates the same as it does in the 80C51, with open-drain outputs.

PORT 1

Port 1 can act the part of standard I/O port.
This port has two dedicated alternate functions:

- P.1[0:3] for CAN (Controller Area Network) interface.
- P.1[4:7] are for synchronous serial link (SPI or mWIRE) interface, In the default configuration, port 1 operates the same as it does in the 80C51, with internal pullups. Port 1 type C51 is sometimes called ”quasi-bidirectional” due to the internal pullups.

PORT 2

Port 2 can act the part of address bus or standard I/O port.
Its dedicated alternate function is the CCU (Capture & Compare Unit) interface.

In the default configuration, port 2 operates the same as it does in the 80C51, with internal pull-ups.

PORT 3

Port 3 can act the part of standard I/O port.
Its dedicated alternate functions are those of the C51 standard (RxD, TxD, INT0, INT1, T0, T1, $\overline{WR}$ & $\overline{RD}$).
In the default configuration, port 3 operates the same as it does in the C51, with internal pull-ups. Port 3 type C51 is sometimes called ”quasi-bidirectional” due to the internal pull-ups.

PORT 4

Port 4 can act the part of standard I/O port.
This port has two types of alternate functions:

- The first ones are 8 inputs for ADC module,
- The second type of alternate functions is the reference voltage, Cref for CAN module.
  In the default configuration, port 4 operates as a ”quasi-bidirectional” port type C51 with internal pullups.

ANAref+

Positive voltage for the ADC module.

PORT 5

Port 5 can act the part of standard I/O port.

Its dedicated alternate function is a 8-bit keyboard interface.

In the default configuration, port 5 operates as a ”quasi-bidirectional” port type C51 with internal pull-ups.

Electro-Magnetic Compatibility (EMC)

Primary attention is paid to the reduction of electro-magnetic emission of the TSC8051A11. The following features reduce the electro-magnetic emission and additionally improve the electro-magnetic susceptibility:

- The TSC8051A11 provides one analog supply voltage pin and one analog ground pin. Placed on the middle of one side of the package, this pair (ANAVcc/ ANAVss) has short bounding wires, thus reducing the generated noise.
  In order to reduce the radiation loop area, the two pins are adjacent.
- The TSC8051A11 provides three groups of digital supply voltage and digital ground, in pairs of pins (Vss/Vcc). Placed on the middle of the three other sides of the package, these groups have short bounding wires, thus reduces the generated noise.
  In order to reduce the radiation loop area, pins are adjacent inside group.
- External capacitors should be connected across associated pins (ANAVcc/ANAVss or Vcc/Vss). Lead length should be as short as possible. Ceramic CMS capacitors are recommended, 10nF + 100nF.
- Several internal decoupling capacitors improve the EMC radiation behavior and the EMC immunity.
- In order to reduce the spectrum of the TSC8051A11, many signals has been treated, principally the periodic signals. The current provided for external signals, the period of clocks and the raising/falling edges are the major points which has been nursed.
  - For application that never (or temporarily) requires external memory resources, the ALE buffer can be disable.
  - Once the oscillator is started, the gain is reduce by 2 (6 dB).
  - Peripherals receiving XTAL clock have, each one, their own prescaler to produce the operating clock they need.
  - The output buffers are especially designed to control rising and falling edges.