CMOS Single Chip 8–bit Microcontroller with VAN Controller

Description

The TSC8051A30 is a stand alone, high performance CMOS microcontroller designed for use in automotive and industrial applications.

The TSC8051A30 retains all features of the MHS 80C51 with extended ROM capacity (16K bytes), 256 bytes of RAM, a 10–source 2–level interrupt, a full duplex serial port, an on–chip oscillator and clock and two 16 bits timers.

In addition, the TSC8051A30 has an 8–bit 8–channel A/D converter, a serial peripheral interface compatible with SPI, a high security watchdog, an advanced 8 channel Capture and Compare timer Unit, a VAN network line controller with a 128 bytes extra RAM used to store the VAN messages.

The VAN controller is fully compliant with the ISO standard ISO/11519–3. It implements all features of the TSS461C VAN data link controller, including a 128 bytes data dual port RAM to store the received and transmitted messages.

The fully static design of the TSC8051A30 allows to reduce system power consumption by bringing the clock frequency down to any value, even DC, without loss of data.

The design is done with a specific care to reduce EMC emission and suceptibility.

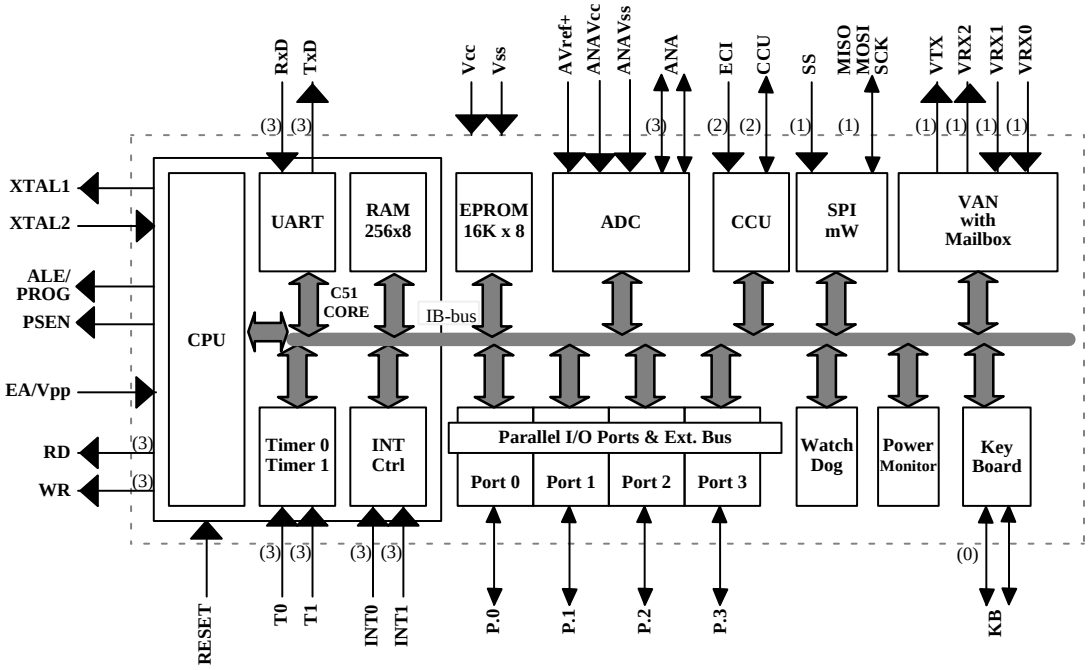
This circuit is manufactured using SCMOS process and is available in commercial, industrial, military and automotive ranges ; it runs from 0 up to 20 MHz in the automotive temperature range –40°C to +125°C.

Features

- 256 bytes of RAM
- 16 K bytes of ROM or OTP
- Four 8–bit I/O ports ; each bit can be:
  - TTL I/O
  - Push–pull output
  - CMOS input trigger with or without pull–down
- Two 16 bit timer/counter
- A programmable window watch–dog with integrated low power RC oscillator; basic period 20 ms typical, maximum period 128 times 20 ms
- A eight channels 16 bits Capture and Compare Unit with:
  - input capture
  - output compare and PWM
- A 8–bit resolution analog to digital converter with eight multiplex inputs ; conversion time 48 machine cycles.
- One port with programmable interrupt for keyboard function
- Several power reduction modes with enhanced wake up capabilities
- Power fail detection, Power on reset bit
- Full duplex UART compatible with standard 80C51
- A serial peripheral interface (SPI+MW)
- VAN controller with 128 bytes data RAM
  - Fully Compliant with VAN standard ISO/11519–3.
  - 14 Identifier Registers with all bits individually maskable
  - 1 Mbits/s Maximum Transfer Rate
  - 3 Separate line inputs with automatic diagnosis and selection
  - Idle and sleep modes
  - Manchester Enhanced or Impulsed Coding
- PQFP, PLCC or SSOP 44 package ; PQFP 64 for emulation

Preview

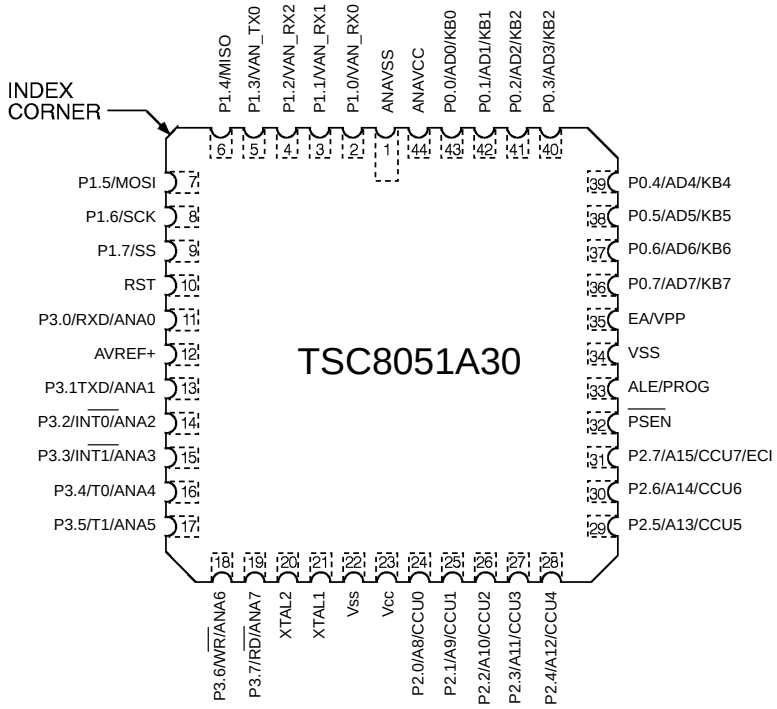
Block Diagram



(1): Alternate function of Port 1 (2): Alternate function of Port 2 (3): Alternate function of Port 3 (0): Alternate function of Port 0

Figure 1. TSC8051A30 Block Diagram

Pin Configuration



Pin PQFP 44	Pin PLCC 44	Name	Function	Pin PQFP 44	Pin PLCC 44	Name	Function
39	1	ANAVSS	VSS Analog	17	23	VCC	VCC
40	2	P1.0/VAN_RX0	VAN RX0	18	24	P2.0/A08/CCU0	Address bus high order or CCU module 1 external I/O
41	3	P1.1/VAN_RX1	VAN RX1	19	25	P2.1/A09/CCU1	Address bus high order or CCU module 1 external I/O
42	4	P1.2/VAN_RX2	VAN RX2	20	26	P2.2/A10/CCU2	Address bus high order or CCU module 2 external I/O
43	5	P1.3/VAN_TX0	VAN TX1	21	27	P2.3/A11/CCU3	Address bus high order or CCU module 3 external I/O
44	6	P1.4/MISO	SPI master in ,slave out	22	28	P2.4/A12/CCU4	Address bus high order or CCU module 4 external I/O
1	7	P1.5/MOSI	SPI master out, slave in	23	29	P2.5/A13/CCU5	Address bus high order or CCU module 5 external I/O
2	8	P1.6/SCK	SPI serial clock I/O	24	30	P2.6/A14/CCU6	Address bus high order or CCU module 6 external I/O
3	9	P1.7/SS	SPI slave select	25	31	P2.7/A15/CCU7/ ECI	Address bus high order or CCU module 7 external I/O or CCU count input
4	10	RST	Reset	26	32	PSEN	Program store enable
5	11	P3.0/RXD/ANA0	Serial receive port or Keyboard	27	33	ALE/PROG	Address latch enable/Program pulse
6	12	AVREF+	Analog positive reference	28	34	VSS	
7	13	P3.1/TXD/ANA1	Serial transmit port or Analog Input 1	29	35	EA/VPP	External access enable/Programming supply voltage
8	14	P3.2/INT0/ANA2	External interrupt 0 or Analog Input 2	30	36	P0.7/AD7/KB7	Mux. low order address & data bus or Keyboard
9	15	P3.3/INT1/ANA3	External interrupt 1 or Analog Input 3	31	37	P0.6/AD6/KB6	Mux. low order address & data bus or Keyboard
10	16	P3.4/T0/ANA4	Timer/counter 0 input or Analog Input 4	32	38	P0.5/AD5/KB5	Mux. low order address & data bus or Keyboard
11	17	P3.5/T1/ANA5	Timer/counter 1 input or Analog Input 5	33	39	P0.4/AD4/KB4	Mux. low order address & data bus or Keyboard
12	18	P3.6/WR/ANA6	External data memory write strobe or Analog Input 6	34	40	P0.3/AD3/KB3	Mux. low order address & data bus or Keyboard
13	19	P3.7/RD/ANA7	External data memory read strobe or Analog Input 7	35	41	P0.2/AD2/KB2	Mux. low order address & data bus or Keyboard
14	20	XTAL2	Crystal output	36	42	P0.1/AD1/KB1	Mux. low order address & data bus or Keyboard
15	21	XTAL1	Crystal input	37	43	P0.0/AD0/KB0	Mux. low order address & data bus or Keyboard
16	22	VSS	VSS	38	44	ANAVCC	VCC Analog

Pin Functions

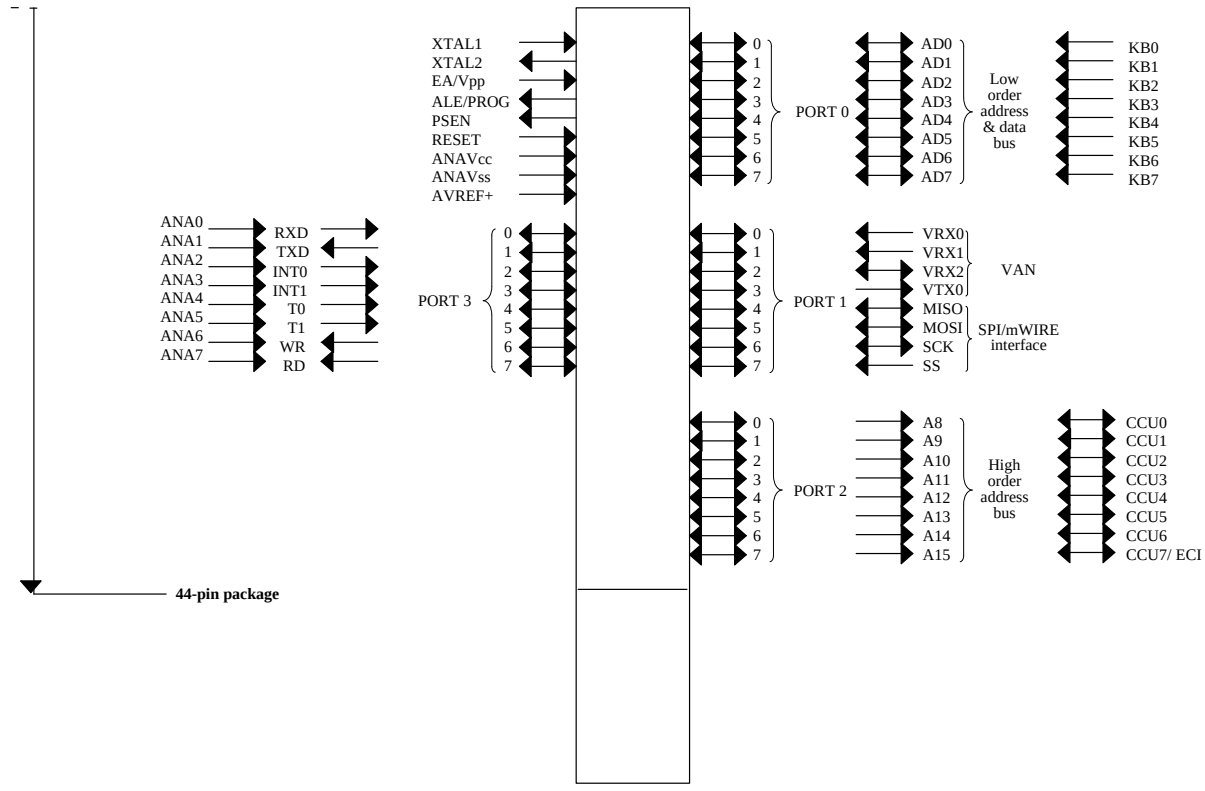


Figure 2. TSC8051A30 pin functions

General Signal Description

Vss

Digital ground

Vcc

Digital supply voltage

ANAVss

Analog groundl

ANAVcc

Analog supply voltage

$\overline{EA}$ / Vpp

External Access enable must be strapped to Vss in order to enable any device plugged on port 0 / port 2 to fetch code from 0 up to 16K. $\overline{EA}$ must be strapped to Vcc for internal program execution.
This pin also receives the 12V programming supply (Vpp input) to program the internal EPROM.

XTAL1

It is the input to the inverting oscillator amplifier and the input for external clock generator.

XTAL2

It is the output from the inverting oscillator amplifier.

$\overline{RESET}$

The active level of the RESET pin is low. An active level on this pin, while the oscillator is running, resets the device. An internal resistor permits power-on reset only using an external capacitor. The reset pin is bidirectional; it acts as an output when a reset is issued by the watch–dog function.

ALE / $\overline{PROG}$

The Address Latch Enable output signal is used to latch the low order byte of the address during accesses to external memory. ALE can sink and source 8 LS TTL loads.If desired, ALE buffer can be disable. Then, ALE is pulled low. This pin is also used (program pulse input) to program the internal EPROM.

$\overline{PSEN}$

Program Store Enable is the read strobe to external program memory, else it remains high. $\overline{PSEN}$ can sink and source 8 LS TTL loads.

PORT 0

Port 0 can act the part of address/data bus or standard I/O port. Its dedicated alternate function are the inputs of the keyboard interrupt. In the default configuration, port 0 operates the same as it does in the 80C51, with open-drain outputs.

PORT 1

Port 1 can act the part of standard I/O port. This port has two dedicated alternate functions:

•P.1[0:3] for VAN (Vehicle Area Network) interface.

•P.1[4:7] are for synchronous serial link (SPI or mWIRE) interface.

In the default configuration, port 1 operates the same as it does in the 80C51, with internal pullups. Port 1 type C51 is sometimes called ”quasi-bidirectional” due to the internal pullups.

PORT 2

Port 2 can act the part of address bus or standard I/O port.Its dedicated alternate function is the CCU (Capture & Compare Unit) interface.In the default configuration, port 2 operates the same as it does in the 80C51, with internal pullups.

PORT 3

Port 3 can act the part of standard I/O port.This port has two types of alternate functions:

- The first ones are the same than in C51 (Rxd, TxD, ..., $\overline{WR}$, $\overline{RD}$),
- The second type of alternate functions are 8 inputs for the 8–bit A/D converter.

In the default configuration, port 3 operates the same as it does in the C51, with internal pullups. Port 3 type C51 is sometimes called ”quasi-bidirectional” due to the internal pullups.

AVREF+

- Positive reference voltage for the ADC module.

Electro-Magnetic Compatibility (EMC)

Primary attention is paid to the reduction of electro-magnetic emission of the TSC8051A30. The following features reduce the electro-magnetic emission and additionally improve the electro-magnetic susceptibility:

- The TSC8051A30 provides one analog supply voltage pin and one analog ground pin. Placed on the middle of one side of the package, this pair (ANAVcc/ ANAVss) has short bounding wires, thus reducing the generated noise.
  In order to reduce the radiation loop area, the two pins are adjacent.
- The TSC8051A30 provides one group of digital supply voltage and digital ground, in pairs of pins (Vss/Vcc). Placed on the middle of the sides of the package, this group have short bounding wires, thus reduces the generated noise. In order to reduce the radiation loop area, pins are adjacent inside group.
- External capacitors should be connected across associated pins (ANAVcc/ANAVss or Vcc/Vss). Lead length should be as short as possible. Ceramic CMS capacitors are recommended, 10nF + 100nF.
- Several internal decoupling capacitors improve the EMC radiation behaviour and the EMC immunity.
- In order to reduce the spectrum of the TSC8051A30, many signals has been treated, principally the periodic signals. The current provided for external signals, the period of clocks and the raising/falling edges are the major points which has been nursed.
  - For application that never (or temporarily) requires external memory resources, the ALE buffer can be disable.
  - Once the oscillator is stable, the gain is reduce by 2 (6 dB).
  - Peripherals receiving XTAL clock have, each one, their own prescaler toproduce the operating clock they need.
  - The output buffers are especially designed to control rising and falling edges.