Image rejecting front-end for GSM applications

UAA2073M

FEATURES

- Low-noise, wide dynamic range amplifier
- Very low noise figure
- Dual balanced mixer for at least 30 dB on-chip image rejection
- IF I/Q combination network for 50 to 90 MHz
- Down-conversion mixer for closed-loop transmitters
- Independent TX/RX fast ON/OFF power-down modes
- Very small outline packaging
- Very small application (no image filter).

APPLICATIONS

- 900 MHz front-end for GSM hand-portable equipment
- Compact digital mobile communication equipment
- TDMA receivers.

GENERAL DESCRIPTION

UAA2073M contains both a receiver front-end and a high frequency transmit mixer intended for GSM (Global System for Mobile communications) cellular telephones. Designed in an advanced BiCMOS process it combines high performance with low power consumption and a high degree of integration, thus reducing external component costs and total front-end size.

The main advantage of the UAA2073M is its ability to provide over 30 dB of image rejection. Consequently, the image filter between the LNA and the mixer is suppressed and the duplexer design is eased, compared with a conventional front-end design.

Image rejection is achieved in the internal architecture by two RF mixers in quadrature and two all-pass filters in I and Q IF channels that phase shift the IF by 45° and 135° respectively. The two phase shifted IFs are recombined and buffered to furnish the IF output signal.

For instance, signals presented at the RF input at LO + IF frequency are rejected through this signal processing while signals at LO – IF frequency can form the IF signal. An internal switch allows the use of infradyne or supradyne reception. Image rejection is at an optimum when the IF is 71 MHz and local oscillator is above the wanted signal.

The receiver section consists of a low-noise amplifier that drives a quadrature mixer pair. The IF amplifier has on-chip 45° and 135° phase shifting and a combining network for image rejection.The IF driver has differential open-collector type outputs.

The LO part consists of an internal all-pass type phase shifter to provide quadrature LO signals to the receive mixers. The all-pass filters outputs are buffered before been fed to the receive mixers.

The transmit section consists of a down-conversion mixer and a transmit IF driver stage. In the transmit mode an internal LO buffer is used to drive the transmit IF down-conversion mixer.

All RF and IF inputs or outputs are balanced to reduce EMC issues.

Fast power-up switching is possible. A synthon mode enables LO buffers independent of the other circuits. When SYNTHON pin is high, all internal buffers on the LO path of the circuit are turned on, thus minimizing LO pulling when remainder of receive chain is powered-up.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	3.6	3.75	5.3	V
I_{CCRX}	receive supply current	22	26	32	mA
I_{CCTX}	transmit supply current	9	12	15	mA
NF	noise figure on demonstration board (including matching and PCB losses)	–	3.35	4.3	dB
G_P	conversion power gain	20	23	26	dB
IR	image frequency rejection	30	-	-	dB
T_{amb}	operating ambient temperature	–30	+25	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA2073M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

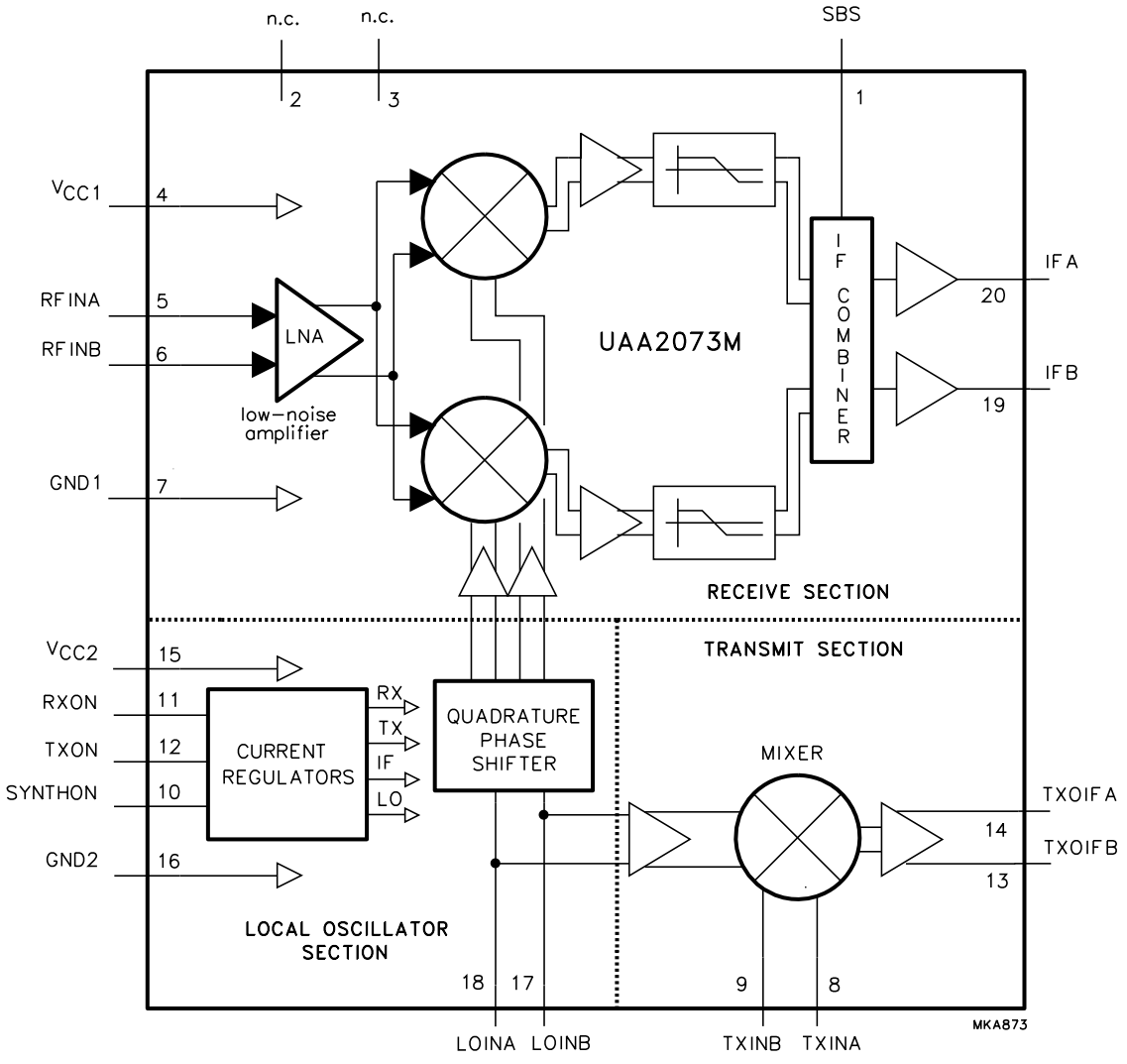

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SBS	1	sideband selection (LOW = LO > RF)
n.c.	2	not connected
n.c.	3	not connected
V_{CC1}	4	supply voltage for LNA, IF parts and TX mixer
RFINA	5	RF balance input A
RFINB	6	RF balance input B
GND1	7	ground 1 for receiver and transmitter mixer
TXINA	8	transmit mixer input A (balanced)
TXINB	9	transmit mixer input B (balanced)
SYNTHON	10	hardware power-on of internal LO buffer
RXON	11	hardware power-on for receive parts
TXON	12	hardware power-on for transmit mixer
TXOIFB	13	transmit mixer IF output B (balanced)
TXOIFA	14	transmit mixer IF output A (balanced)
V_{CC2}	15	supply voltage for LO parts
GND2	16	ground 2 for LO parts
LOINB	17	LO input B (balanced)
LOINA	18	LO input A (balanced)
IFB	19	IF output (balanced)
IFA	20	IF output (balanced)

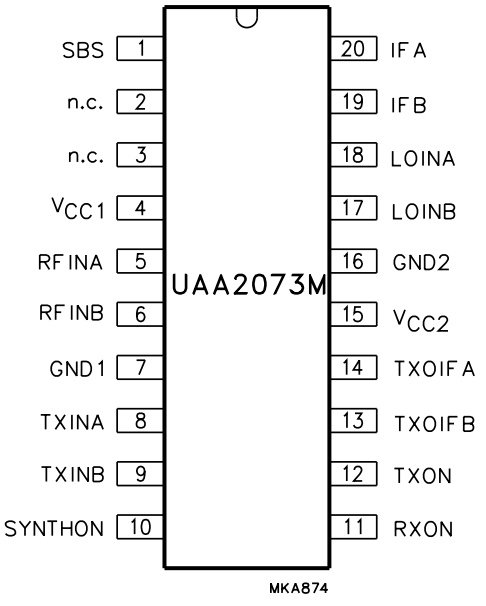

Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Receive section

The circuit contains a low-noise amplifier followed by two high dynamic range mixers. These mixers are of the Gilbert-cell type. The whole internal architecture is fully differential.

The local oscillator, shifted in phase to 45° and 135°, mixes the amplified RF to create I and Q channels. The two I and Q channels are buffered, phase shifted by 45° and 135° respectively, amplified and recombined internally to realize the image rejection.

Pin (SBS) allows selection between infradyne or supradyne reception.

Balanced signal interfaces are used for minimizing crosstalk due to package parasitics. The RF impedance level is 150 Ω, choosen to minimize current consumption at best noise performance.

The IF output is differential and of the open-collector type, tuned for 71.3 MHz. Typical application will load the output with a differential 500 Ω load; i.e. a 500 Ω resistor load at each IF output, plus a 1 kΩ resistor to x Ω narrow band matching network (x Ω being the input impedance of the IF filter). The path to V_{CC} for the DC current is achieved via tuning inductors. The output voltage is limited to $V_{CC} + 3V_{be}$ or 3 diode forward voltage drops.

Fast switching, ON/OFF, of the receive section is controlled by the hardware input RXON.

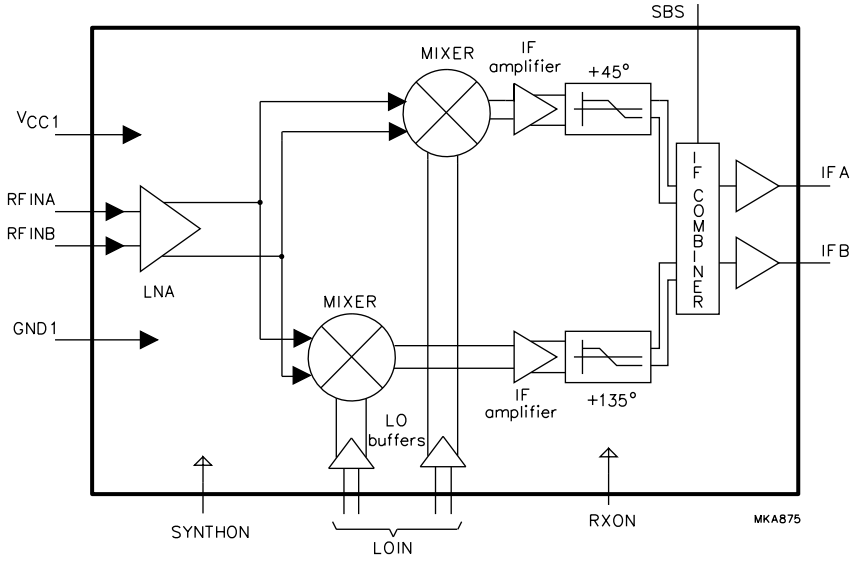

Fig.3 Block diagram, receive section.

Local oscillator section

The local oscillator (LO) input directly drives the two internal all-pass networks to provide quadrature LO to the receive mixers.

The LO input impedance is 50 Ω differential.

A synthon mode is used to power-up the buffering on the LO inputs, minimizing the pulling effect on the external VCO when entering transmit or receive modes.

This mode is active when the SYNTHON input is high. Table 1 shows status of circuit in accordance with TXON, RXON and SYNTHON inputs.

Transmit mixer

This mixer is used for down-conversion to the transmit IF. Its inputs are coupled to the transmit RF and down-convert it to a modulated transmit IF frequency which is phase locked with the baseband modulation.

The transmit mixer provides a differential input at 200 Ω and a differential output driver buffer for a 1 kΩ load. The IF outputs are low impedance (emitter followers).

Fast switching, ON/OFF, of the transmit section is controlled by the hardware input TXON.

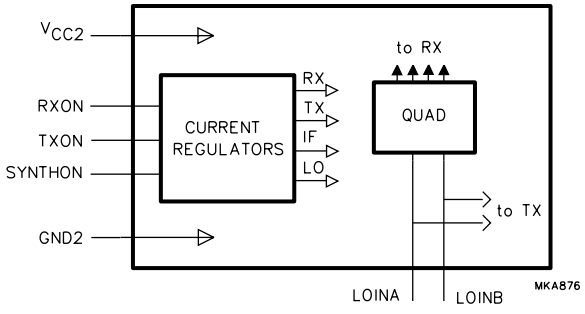

Fig.4 Block diagram, LO section.

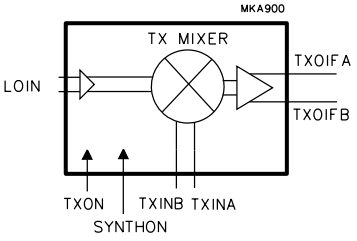

Fig.5 Block diagram, transmit mixer.

Table 1 Control of power status

EXTERNAL PIN LEVEL			CIRCUIT MODE OF OPERATION
TXON	RXON	SYNTHON	
LOW	LOW	LOW	power-down mode
LOW	HIGH	LOW	receive section on
HIGH	LOW	LOW	transmit section on
LOW	LOW	HIGH	synthon on mode, transmit and receive LO buffers enabled
LOW	HIGH	HIGH	receive section on and synthon mode active
HIGH	LOW	HIGH	transmit section on and synthon mode active
HIGH	HIGH	LOW	receive and transmit sections on; specification not guaranteed
HIGH	HIGH	HIGH	receive and transmit sections on; specification not guaranteed

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–	9	V
ΔGND	difference in ground supply voltage applied between GND1 and GND2	–	0.6	V
$P_{I(max)}$	maximum power input	–	+20	dBm
$T_{j(max)}$	maximum operating junction temperature	–	+150	°C
$P_{dis(max)}$	maximum power dissipation in quiet air	–	250	mW
T_{stg}	storage temperature	–65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

HANDLING

Every pin withstands the ESD test in accordance with MIL-STD-883C class 2 (method 3015.5).

DC CHARACTERISTICS

V_{CC} = 3.75 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins: V_{CC1}, V_{CC2}, LOINA and LOINB						
V_{CC}	supply voltage	over full temperature range	3.6	3.75	5.3	V
I_{CCRX}	supply current	receive mode active; DC tested	21	26	32	mA
I_{CCTX}	supply current	transmit mode active; DC tested	9.3	12	14.7	mA
I_{CCSX}	supply current	synthon mode only	4.4	5.6	6.6	mA
I_{CCSRX}	supply current	receive and synthon mode active	22	28	34	mA
I_{CCSTX}	supply current	transmit and synthon mode active	12.5	15.0	19.5	mA
I_{CCPD}	supply current in power-down mode	DC tested	–	0.01	50	µA
Pins: SYNTHON, RXON, TXON and SBS						
V_{th}	CMOS threshold voltage	note 1	–	1.25	–	V
V_{IH}	HIGH level input voltage		3	–	V_{CC}	V
V_{IL}	LOW level input voltage		–0.3	–	0.8	V
I_{IH}	HIGH level static input current	pin at V_{CC} – 0.4 V	–1	–	+1	µA
I_{IL}	LOW level static input current	pin at 0.4 V	–1	–	+1	µA
Pins: RFINA and RFINB						
V_I	DC input voltage level	receive mode enabled	2.0	2.2	2.4	V
Pins: IFA and IFB						
I_O	DC output current	receive mode enabled	2.4	3.0	3.6	mA
Pins: TXINA and TXINB						
V_I	DC input voltage level	transmit section enabled	2.1	2.4	2.6	V
Pins: TXOIFA and TXOIFB						
V_O	DC output voltage level	transmit section enabled	1.8	1.9	2.1	V
Pins: LOINA and LOINB						
V_I	DC input voltage level	receive section enabled	2.3	2.5	2.8	V
		transmit section enabled	2.3	2.5	2.8	V

Note

1. The referenced inputs should be connected to a valid CMOS input level.

AC CHARACTERISTICS

V_{CC} = 3.75 V; T_{amb} = –30 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receive section (receive section enabled)						
Z_{RF}	RF input impedance	balanced	–	150	–	Ω
f_{RF}	RF input frequency		925	–	960	MHz
RL_{RF}	return loss on matched RF input	note 1	15	20	–	dB
G_{CP}	conversion power gain	differential RF input to differential IF output matched to 1 kΩ differential	20	23	26	dB
G_{rip}	gain ripple as a function of RF frequency	note 2	–	0.2	0.5	dB
ΔG/T	gain variation with temperature	note 2	–20	–15	–10	mdB/K
DES_1	1 dB desensitization input power		–	–30	–	dBm
$CP1_{RX}$	1 dB input compression point	note 1	–24.5	–23.0	–	dBm
$IP2D_{RX}$	2nd order intercept point referenced to the RF input differential	differential output; note 2	+30	+40	–	dBm
$IP3_{RX}$	3rd order intercept point referenced to the RF input	note 2	–18	–15	–	dBm
NF_{RX}	overall noise figure	RF input to differential IF output; notes 2 and 3	–	3.25	4.30	dB
$Z_{L(IF)}$	typical application IF output load impedance	balanced	–	1	–	kΩ
$C_{L(IF)}$	IF output load capacitance	unbalanced	–	–	2	pF
f_{IF}	IF frequency range	RF < LO	50	71	100	MHz
		RF > LO	50	71	100	MHz
IR	image frequency rejection		30	37	–	dB
Local oscillator section (transmit and receive section enabled, SYNTHON = 1)						
f_{LO}	LO input frequency		850	–	1100	MHz
Z_{LO}	LO input impedance	balanced	–	50	–	Ω
ΔZ_{LO}	impedance change when switching from synthon mode to transmit or receive	mUnits measured on Smith chart	–	20	–	
RL_{LO}	return loss on matched input (including standby mode)	note 2	10	15	–	dB
$P_{i(LO)}$	LO input power level		–7	–4	0	dBm
RI_{LO}	reverse isolation	LOIN to RFIN at LO frequency; note 1	40	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transmit section (transmit section enabled)						
Z_O	TX IF output impedance		–	–	200	Ω
Z_L	TX IF load impedance		–	1	–	kΩ
C_L	maximum TX IF load capacitance		–	–	2	pF
$Z_{i(RF)}$	TX RF input impedance	balanced	–	200	–	Ω
f_{TXmix}	TX mixer input frequency		890	–	915	MHz
RL_{TX}	return loss on matched TX input	note 2	15	20	–	dB
G_{CP}	conversion power gain	from 200 Ω to 1 kΩ output	5	7.4	10	dB
$f_{o(TX)}$	TX mixer output frequency		40	–	200	MHz
$CP1_{TX}$	1 dB input compression point		–22	–17.5	–	dBm
$IP2_{TX}$	2nd order intercept point		–	+20	–	dBm
$IP3_{TX}$	3rd order intercept point		–12	–9	–	dBm
NF_{TX}	noise figure	double sideband; note 2	–	9.8	12	dB
RI_{TX}	reverse isolation	TXIN to LOIN; note 2	40	–	–	dB
I_{TX}	isolation	LOIN to TXIN; note 2	40	–	–	dB
Timing						
t_{start}	start-up time of each block		1	5	20	µs

Notes

1. Measured and guaranteed only on UAA2073M demonstration board at T_{amb} = +25 °C.
2. Measured and guaranteed only on UAA2073M demonstration board.
3. This value includes printed-circuit board and balun losses on Philips UAA2073M demonstration board over full temperature range.

APPLICATION INFORMATION

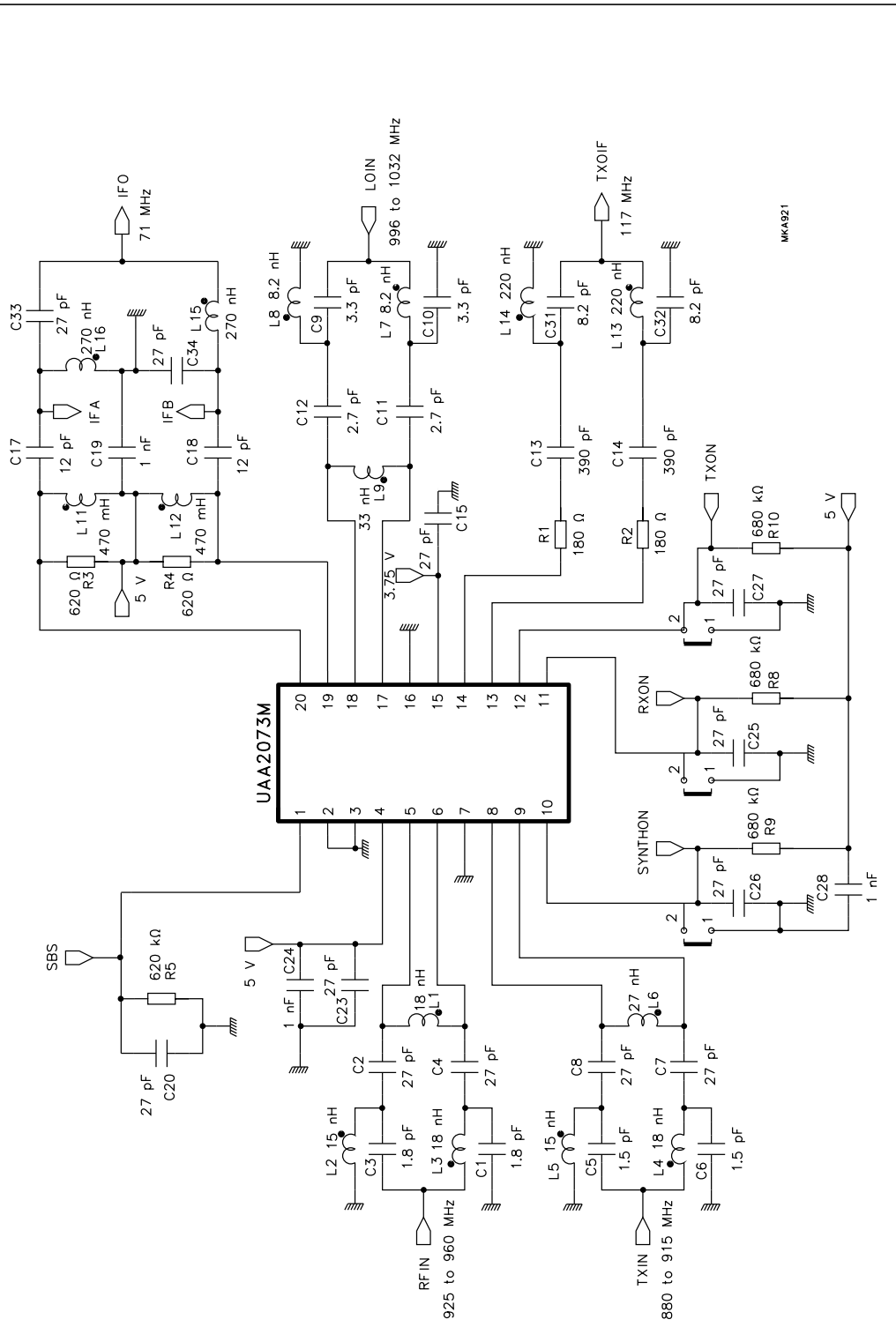

Fig.6 Application diagram.

Table 2 UAA2073M demonstration board parts list

PART	VALUE	SIZE	LOCATION
Resistors			
R1	180 Ω	0805	TXOIF
R2	180 Ω	0805	TXOIF
R3	620 Ω	0805	IF
R4	620 Ω	0805	IF
R5	620 Ω	0805	SBS
R8	680 kΩ	0805	RXON
R9	680 kΩ	0805	SYNTHON
R10	680 kΩ	0805	TXON
Capacitors			
C1	1.8 pF	0805	RFIN
C2	27 pF	0805	RFIN
C3	1.8 pF	0805	RFIN
C4	27 pF	0805	RFIN
C5	1.5 pF	0805	TXIN
C6	1.5 pF	0805	TXIN
C7	27 pF	0805	TXIN
C8	27 pF	0805	TXIN
C9	3.3 pF	0805	LOIN
C10	3.3 pF	0805	LOIN
C11	27 pF	0805	LOIN
C12	27 pF	0805	LOIN
C13	390 pF	0805	TXOIF
C14	390 pF	0805	TXOIF
C15	27 pF	0805	V_{CCLO}
C16	120 pF	0805	V_{CCLO}
C17	12 pF	0805	IF
C18	12 pF	0805	IF
C19	1 nF	0805	IF/V_{CC}
C20	27 pF	0805	SBS
C23	27 pF	0805	V_{CCLNA}
C24	1 nF	0805	V_{CCLNA}
C25	27 pF	0805	RXON
C26	27 pF	0805	SYNTHON
C27	27 pF	0805	TXON
C28	1 nF	0805	V_{CC}
C29	100 nF	1206	V_{CCREG}
C30	100 nF	1206	V_{CCREG}
C31	8.2 pF	0805	TXOIF
C32	8.2 pF	0805	TXOIF
C33	27 pF	0805	IF
C34	27 pF	0805	IF
C35	link	0805	IF/not used
C36	link	0805	IF/not used
Inductors			
L1	18 nH	0805	RFIN
L2	15 nH	0805	RFIN
L3	15 nH	0805	RFIN
L4	15 nH	0805	TXIN
L5	15 nH	0805	TXIN
L6	27 nH	0805	TXIN
L7	8.2 nH	0805	LOIN
L8	8.2 nH	0805	LOIN
L9	33 nH	0805	LOIN/ optional
L10	–	1008	TXOIF/ not required
L11	470 nH	1008	IF
L12	470 nH	1008	IF
L13	220 nH	1008	TXOIF
L14	220 nH	1008	TXOIF
L15	270 nH	0805	IF
L16	270 nH	0805	IF

Other components

COMPONENT	DESCRIPTIONS
IC1	UAA2073M
SMA/RIM	sockets for RF and IF inputs/outputs
SMB	V_{CC} socket (optional in place of IC2)
025 connect	various 2.54 mm (0.1 inch) connectors

Component manufacturers

All surface mounted resistors and capacitors are from Philips Components. The small value capacitors are multilayer ceramic with NPO dielectric. The inductors are from Coilcraft UK.