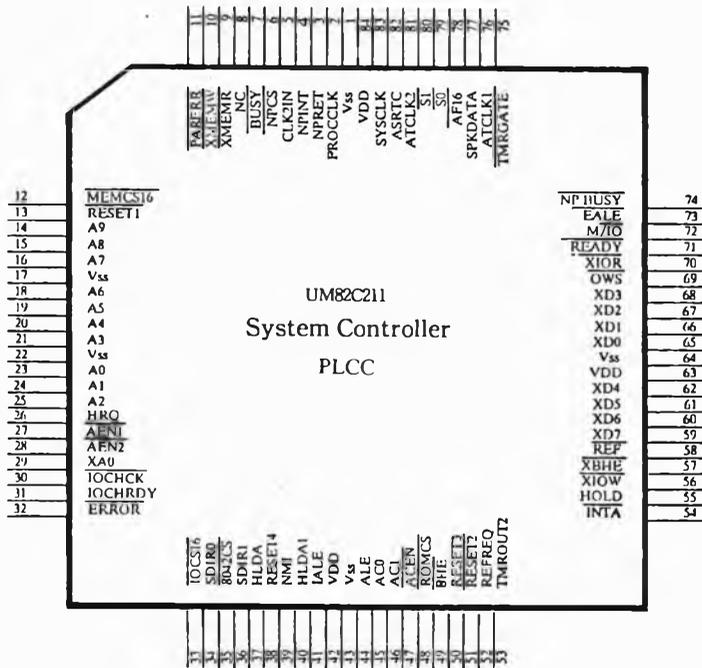


## 1. UM82C211 SYSTEM CONTROLLER

The UM82C211 highly integrates CPU interface and bus control logic. Most of the system functions, except memory access, are taken care of by the UM82C211. The main functions of the UM82C211 are reset and shutdown, clock generation, clock speed selection, CPU state machine, AT bus state machine, bus arbitration, action code generation, Port B and NMI generation, DMA, refresh, numeric coprocessor interface, etc.



## 1.1 Operation Modes of the UM82C211

There are 4 operation modes provided by the UM82C211 for different CPU and AT bus clock selections. These 4 modes are Normal mode, Quick mode, Delayed mode, and External mode.

### 1.1.1 Normal Mode

The clock selections in Normal Mode are:

$$\begin{aligned}\text{PROCCLK} &= \text{CLK2IN} \text{ and} \\ \text{SYSCLK} &= \text{CLK2IN} / 4\end{aligned}$$

Because the PROCCLK and SYSCLK are both derived from the CLK2IN, the Normal Mode is a synchronous mode. In the Normal Mode, the ALE and commands ( $\overline{\text{XMEMR}}$ ,  $\overline{\text{XMEMW}}$ ,  $\overline{\text{XIOR}}$ ,  $\overline{\text{XIOW}}$ ) are issued for AT bus cycle only, and have nothing to do with the local cycles.

### 1.1.2 Quick Mode

The clock selections in Quick Mode are:

$$\begin{aligned}\text{PROCCLK} &= \text{CLK2IN} \text{ and} \\ \text{SYSCLK} &= \text{CLK2IN} / 2\end{aligned}$$

Since the PROCCLK and SYSCLK are both derived from the CLK2IN, the Quick Mode is a synchronous mode also. One of the differences between the Normal Mode and the Quick Mode is that the ALE signal is generated on the AT bus for both AT bus cycle and local bus cycle in the Quick Mode while the ALE is generated for only AT bus cycle in the Normal Mode. However, the commands ( $\overline{\text{XMEMR}}$ ,  $\overline{\text{XMEMW}}$ ,  $\overline{\text{XIOR}}$ ,  $\overline{\text{XIOW}}$ ) are still not issued for local bus cycles in the Quick Mode.

### 1.1.3 Delayed Mode

The clock selections in Delayed Mode are :

$$\begin{aligned}\text{PROCCLK} &= \text{CLK2IN} \text{ and} \\ \text{SYSCLK} &= \text{CLK2IN} / 2\end{aligned}$$

This mode is a synchronous mode also. The clock selections for the Delayed Mode are the same as the selections for the Quick Mode. However, this mode is enabled when the Quick Mode is disabled. In the Delayed Mode, the ALE and commands are generated for AT bus cycle only, and not generated for any local bus cycle.

### 1.1.4 External Mode

The clock selections in External Mode are :

PROCCLK = CLK2IN and  
SYSCLK = ATCLK / 2

Since the ATCLK is running asynchronously to CLK2IN and the SYSCLK is derived from ATCLK, the External Mode is an asynchronous mode.

## 1.2 Configuration Registers

There are three 8-bit registers provided in the UM82C211 for configuration purposes. In order to reduce the number of I/O ports required to access all the registers used in the UM82C210 chip set, the index access is used. To access a particular register, the index address is placed at address port and data is located at data port.

The first register, R11, is used for PROCCLK selections, time out enable, NMI enable, and CPU software reset. The second register, R12, is used for command delay selections, hold time delay, and Quick Mode enable. The third register, R13, is used for SYSCLK selections, and wait state selections.

**R11 : (Index Address 60H)**

Bits	Function
7,6	UM82C211 revision number.
5	CPU reset.
4	Processor clock selection.
3	Reserved.
2	$\overline{\text{READY}}$ timeout NMI enable.
1	Reserved.
0	$\overline{\text{READY}}$ timeout.

**R12 : (Index Address 61H)**

Bits	Function
7	Address hold time delay.
6	Quick Mode enable.
5,4	AT Bus 16 bit memory command delay.
3,2	AT Bus 8 bit memory command delay.
1,0	AT Bus I/O cycle command delay.

**R13 : (Index Address 62H)**

Bits	Function
7,6	Reserved.
5,4	Wait state selection for 16 bit AT cycle.
3,2	Wait state selection for 8 bit AT cycle.
1,0	Bus clock selection.

### 1.3 Action Codes

In order to convert 16-bit operations to 8-bit operations for CPU to access 8-bit AT bus devices, the UM82C211 generates Action Code Enable and action codes to control the buffers in the UM82C215 for the bus conversion. Table 1.1 defines the Action Code Enable and Action Codes.

Operation	$\overline{\text{ACEN}}$	AC1	AC0	Function
DMA/MASTER	0	0	0	16 & 8-bit R/W operations
	0	0	1	Reserved
	0	1	0	Write, MD0-7 to MD8-15
	0	1	1	Read, MD8-15 to MD0-7
CPU(AT BUS)	0	0	0	16 & 8-bit W/O operations
	0	0	1	16 & 8-bit R/O operations
	0	1	0	8-bit write (high byte)
	0	1	1	8-bit read (high byte)
CPU(local)	1	X	X	No conversion

Table 1.1 Functions of Action Codes.

## 1.4. Numeric Coprocessor Interface

The UM82C211 provides necessary interface circuitry between 80286 and its coprocessor 80287. The major functions of the interface circuitry are as follows :

- 1) Numeric Coprocessor chip selection decoding.
- 2) Resetting Numeric Coprocessor.
- 3) Handling  $\overline{\text{NPBUSY}}$  and  $\overline{\text{ERROR}}$  signals from 80287 to the CPU.
- 4) Generating interrupt signals for error conditions.