UM83C002

RAM Buffer Controller

Features

- 3 DMA channels
- Host processor port
- Refresh circuit for dynamic RAM built-in
- RAM access priority network
- Address multiplexing for dynamic RAM
- Multiplexed address and data lines from processor
- Pins arranged for easy integration into 8088/8086 systems
- No lost RAM cycles for DMA break-in
- DMA carry output permits DMA across 64K boundaries
- 24 bit timer or baud rate generator
- TTL compatible inputs and outputs. Outputs drive 8 LSTTL loads

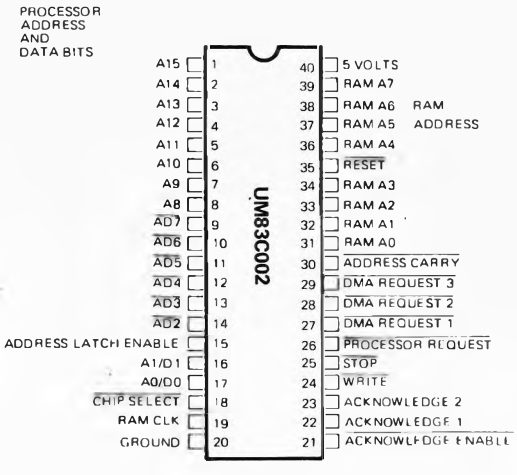
General Description

The RAM BUFFER CONTROLLER contains three high-speed DMA channels: a host computer address port, dynamic RAM refresh circuitry, and RAM access priority logic. One of the DMA address counters points inside the buffer RAM for transferring data between the RAM and the disk. A refresh address counter handles dynamic RAM refreshing. Also on chip is an address multiplexer.

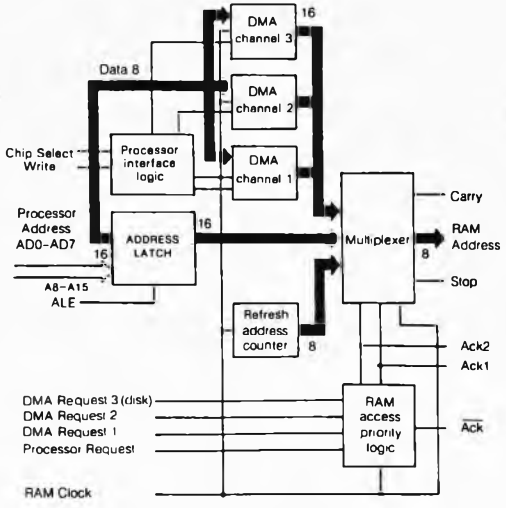
The DISK CONTROLLER UM83C001 connects to one of the RAM controller chip's DMA channels. The two other DMA channels may be used by other high-speed memory-peripheral drives or tape systems — if the chip set is being used with its own on-board processor.

When teamed with the UM83C001, the UM83C002 gives the disk direct access to a buffer RAM array. What's more, it does so at a speed high enough to accommodate 5 Mbit, 10 Mbit and 15 Mbit data transfer rates. The new ST412HP interface, for instance, which operates at 10 Mbits with MFM encoding, would have a 15 Mbit throughput if it employed RLL2, 7 encoding instead.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Power Supply Voltage, V_{DD} . . . . . −0.5 to +7.0 V
Input Voltage, V_I . . . . . −0.5 V to V_{DD} + 0.5 V
Operating Temperature, T_{OPT} . . . . . −40 to +85°C
Storage Temperature, T_{STG} . . . . . −65 to +150°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
Power Supply Voltage	V_{DD}	4.5	5	5.5	V	
Input Voltage	V_I	0		V_{DD}	V	
Low-Level Input Voltage	V_{IL}	0		0.8	V	TTL Level*
High-Level Input Voltage	V_{IH}	2.0		V_{DD}	V	TTL Level*
Input Rise Fall Times	t_R, t_F			10	μS	

Note: (T_A = 0 to +70°C, V_{DD} = 5 V + 5% unless otherwise specified)

DC Electrical Characteristics

Parameter	Symbol	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
Static Current	I_L		0.1	200	μA	$V_I = V_{DD}$ or GND
Dynamic Current	I_{DD}		4		μA	1 MHz/cell
Input Current	I_I		0.1	10	μA	$V_I = V_{DD}$ or GND
Low-Level Output Current	I_{OL}	3.2	9		mA	V_{OL} = 0.4 V
High-Level Output Current	I_{OH}	1	3		mA	$V_{OH} = (V_{DD}-0.4)$ V
Low-Level Output Voltage	V_{OL}			0.1	V	I_O = 0
High-Level Output Voltage	V_{OH}	$V_{DD}-0.1$			V	I_O = 0

AC Characteristics

Parameter	Symbol	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
Maximum Operating Frequency	f_{MAX}	DC		50	MHz	
Output Rise Time	t_R		8		ns	C_L = 15 pF
Output Fall Time	t_F		4		ns	C_L = 15 pF

Pin Description

Pin No.	Symbol	Description
1 THRU 14, 16, AND 17	PROCESSOR ADDRESS AND DATA BITS	These 16 pins are time multiplexed to provide a 16 bit CPU Address and an 8 bit CPU data bus to the UM83C001
15	ADDRESS LATCH ENABLE (ALE)	When the ADDRESS LATCH ENABLE signal is high, the address on the AD0 to AD15 lines is enabled into the ADDRESS LATCH in the UM83C002. When the ALE signal goes low, this address is held in the latch to be used for addressing the RAM. After ALE goes low, data may be placed on the AD0 to AD7 lines.
18	$\overline{\text{CHIP SELECT}}$ ($\overline{\text{CSEL}}$)	The CHIP SELECT lines are driven low by the processor to read from or write to the registers inside the UM83C002. This signal is not intended to be gated by the processor's acknowledge signal. When the processor does a read of registers within the UM83C002, the read data will be held on the data lines until the $\overline{\text{CSEL}}$ line goes back high.
19	RAM CLOCK	This line is an input that serves two purposes. It provides the timing for multiplexing the RAS and CAS addresses to the dynamic RAM and its trailing or rising edge provides the clock to define all memory cycles. When this line is high the RAS addresses are output at RAM A0 to RAM A7. When it is low, the CAS addresses are output at RAM A0 to RAM A7. The input lines $\overline{\text{REQ1}}$, $\overline{\text{REQ2}}$, $\overline{\text{REQ3}}$ and $\overline{\text{REQH}}$ are sampled at the rising edge of this clock to determine who will be granted access to memory during the next memory cycle.
20	GROUND	Negative supply.
21	$\overline{\text{ACKNOWLEDGE ENABLE}}$	A low on this line indicates that one of the REQUEST lines has been granted access to RAM. The REQUEST lines are sampled on the rising edge of RAM CLOCK..
22	ACKNOWLEDGE 1	When the $\overline{\text{ACKNOWLEDGE}}$ line is low, these two lines are encoded to indicate which request has been granted access to RAM.
23	ACKNOWLEDGE 2	

$\overline{\text{ACK}}$	ACK2	ACK1	Request Granted
L	H	H	REQUEST 3
L	H	L	REQUEST 2
L	L	H	REQUEST 1
L	L	L	CPU REQUEST

Pin Description (Continued)

Pin No.	Symbol	Description
24	$\overline{\text{WRITE}}$ ($\overline{\text{WRT}}$)	This line indicates whether a read or a write is to be performed. A low indicates a write and a high indicates a read. During processor cycles, it is driven by the processor. During DMA cycles, it is normally driven by the UM83C002. However, the UM 83C002 may be programmed to allow the I/O device to drive this line. During unused cycles and refresh cycles, the UM83C002 drives this line high to eliminate the need for an external pull-up resistor.
25	$\overline{\text{STOP}}$	This line goes low to indicate the last cycle of a DMA transfer. It is normally driven low by the UM83C002 when the byte counter of the active DMA channel has reached zero. The DMA channel becomes disabled after this last cycle and it will ignore any further requests until it has been restarted by writing to its command register. Each channel can be programmed to allow the external I/O device to drive this line. However, internal byte counts are always active so that transfer will stop when $\overline{\text{STOP}}$ goes low or when the byte count reaches zero, whichever comes first. This line is driven by the UM83C002 during unused cycles (cycles during which $\overline{\text{ACKNOWLEDGE}}$ is high). It is normally driven low. However, a refresh cycle is indicated when $\overline{\text{STOP}}$ $\overline{\text{ACKNOWLEDGE}}$ and $\overline{\text{WRITE}}$ are high at the same time. A timer cycle is indicated by $\overline{\text{WRITE}}$ being low when $\overline{\text{ACKNOWLEDGE}}$ and $\overline{\text{STOP}}$ are high.
26	$\overline{\text{PROCESSOR REQUEST}}$	The processor requests access to RAM by placing a low on this line. This line is sampled by the rising edge of the RAM CLOCK. The processor has lowest priority. It will be granted access to RAM only if all three DMA requests are HIGH.
27	$\overline{\text{DMA REQUEST 1}}$	This is the lowest priority DMA REQUEST. It samples on the rising edge of RAM CLOCK. DMA CHANNEL 1 will be granted access to RAM, If DMA REQUEST 2 and DMA REQUEST 3 are high.
28	$\overline{\text{DMA REQUEST 2}}$	This is the middle priority DMA REQUEST. This channel will be granted access to RAM only if DMA REQUEST 3 is high.
29	$\overline{\text{DMA REQUEST 3}}$	This is the highest priority DMA REQUEST. If this line is low when the rising edge of RAM CLOCK occurs, DMA CHANNEL 3 will control the next memory cycle.
30	$\overline{\text{ADDRESS CARRY}}$	This output goes low to indicate that the memory address of the DMA channel that is acknowledged is at its maximum count of 65,535 and will roll over to 0 at the end of this memory cycle. This line also goes low on a refresh cycle when the refresh address counter is at its maximum count of 255. This line also goes low on a timer cycle when the timer is at its maximum count. When operating in the address decrement mode, that line goes low to indicate that the DMA channel address is 0000 and this it is going to roll over to FFFF at the end of the current memory cycle. This line is provided so that DMA transfers can be performed across 64K boundaries if desired. This line would be used to increment an external counter containing the higher order address bits. This line can also be used to increment additional external refresh address counter bits if more than 8 bits of refresh address are required. This line can also be used to extend the timer beyond 24 bits.

Pin Description (Continued)

Pin No.	Symbol	Description
31 ~ 34 36 ~ 39	A0 ~ A3 A4 ~ A7 RAM	These are the multiplexed address lines for use with dynamic RAMS. When RAM CLOCK is high, address bits 8 thru 15 are gated to these lines. When RAM CLOCK is low, address bits 0 thru 7 are gated to these lines. During REFRESH cycles, the refresh address is gated to these lines. During TIMER cycles, the timer count is gated to these lines.
35	$\overline{\text{RESET}}$	A low on this $\overline{\text{RESET}}$ line resets the UM83C002 to its initial state. The refresh rate is set to maximum refresh every other memory cycle and all three DMA channels are disabled.
40	+5 VOLTS	Positive supply.

RAM BUS Operation

A combination of pin signals control the BUS OPERATION to and from the UM83C002 chip. These combinations are shown in Table 1.

$\overline{\text{CARRY}}$	$\overline{\text{STOP}}$	$\overline{\text{CSEL}}$	$\overline{\text{WRITE}}$	$\overline{\text{ACK}}$	ACK2	ACK1	RAM BUS Operation
X	X	H	L	L	L	L	CPU WRITE TO MEM/IO
X	X	H	H	L	L	L	CPU READ FROM MEM/IO
X	X	L	L	L	L	L	CPU WRITE TO UM83C002
X	X	L	H	L	L	L	CPU READ FROM UM83C002
X	X	X	L	L	L	H	CH 1 WRITE TO MEMORY
X	X	X	H	L	L	H	CH 1 READ FROM MEMORY
L	X	X	X	L	L	H	CH 1 ADDRESS CARRY
X	L	X	X	L	L	H	CH 1 STOP TRANSFER
X	X	X	L	L	H	L	CH 2 WRITE TO MEMORY
X	X	X	H	L	H	L	CH 2 READ FROM MEMORY
L	X	X	X	L	H	L	CH 2 ADDRESS CARRY
X	L	X	X	L	H	L	CH 2 STOP TRANSFER
X	X	X	L	L	H	H	CH 3 WRITE TO MEMORY
X	X	X	H	L	H	H	CH 3 READ FROM MEMORY
L	X	X	X	L	H	H	CH 3 ADDRESS CARRY
X	L	X	X	L	H	H	CH 3 STOP TRANSFER
X	H	X	L	H	X	X	TIMER COUNT ON BUS
L	H	X	L	H	X	X	TIMER COUNT CARRY
X	H	X	H	H	X	X	REFRESH ADDRESS ON BUS
L	H	X	H	H	X	X	REFRESH ADDRESS CARRY
X	L	X	X	H	X	X	INACTIVE BUS CYCLE

H = HIGH L = LOW X = DON'T CARE

Table 1. Signal Combinations

Register Addressing

The UMC RAM BUFFER CONTROLLER, UM83C002, occupies 2 I/O port locations selected by the ADO pin. ADO driven low selects the REGISTER ADDRESS/ STATUS REGISTER and ADO driven high selects the DATA register.

There are 16 internal registers in the UM83C002. These registers are accessed by writing the register address into the REGISTER ADDRESS register. The selected register can then be accessed by doing a READ or WRITE with ADO high.

		Read	Write
	BIT	STATUS	REGISTER ADDRESS
AO = 0	7	CHANNEL 3 ACTIVE	0
	6	CHANNEL 2 ACTIVE	0
	5	CHANNEL 1 ACTIVE	CHANNEL NO. BIT 1
	4	TIMER ACTIVE	CHANNEL NO. BIT 0
	3	AUTO-INCREMENT	AUTO-INCREMENT
	2	REG A2	REG A2
	1	REG A1	REG A1
	0	REG A0	REG A0
	BIT	REGISTER DATA	REGISTER DATA
AO = 1	7	D7	D7
	6	D6	D6
	5	D5	D5
	4	D4	D4
	3	D3	D3
	2	D2	D2
	1	D1	D1
	0	D0	D0

Table 2. Register Addressing

The following is a list of the WRITE and READ addresses:

Register Address Decimal	HEX	Auto INCR HEX	Function	Read	Write
0	00	08	TIMER/REFRESH	TIMER COUNT	CLK DIVIDER LO
1	01	09		CH 1 STATUS	CLK DIVIDER HI
2	02	0A		CH 2 STATUS	TIMER CONTROL
3	03	0B		CH 3 STATUS	TIMER COUNT
4	04	0C*		TIMER COUNT	REFRESH RATE
16	10	18	DMA CHANNEL 1	ADDRESS LO	
17	11	19		ADDRESS HI	
18	12	1A		BYTE COUNT LO	
19	13	1B		BYTE COUNT HI	
20	14	1C*		CH 1 STATUS	CH 1 COMMAND
32	20	28	DMA CHANNEL 2	ADDRESS LO	
33	21	29		ADDRESS HI	
34	22	2A		BYTE COUNT LO	
35	23	2B		BYTE COUNT HI	
36	24	2C*		CH 2 STATUS	CH 2 COMMAND
48	30	38	DMA CHANNEL 3	ADDRESS LO	
49	31	39		ADDRESS HI	
50	32	3A		BYTE COUNT LO	
51	33	3B		BYTE COUNT HI	
52	34	3C*		CH 3 STATUS	CH 2 COMMAND

* These addresses do not auto-increment.

Table 3. Register Addresses

Write Register Addresses

(HEX 00) CLK DIVIDER LO (AUTO INCR HEX 08)

The timer consists of a 16-bit variable CLOCK DIVIDER which divides the RAM CLOCK rate. The divided down RAM CLOCK is then used to increment the 8-bit TIMER COUNT register.

(HEX 01) CLK DIVIDER HI (AUTO INCR HEX 09)

To divide by "N", the 16 bit CLOCK DIVIDER is set to N-1.

(HEX 02) TIMER CONTROL (AUTO INCR HEX OA)

Writing to this address sets one of several timer modes.

BIT 7 = ENABLE TIMER
- 1 = Timer Run
- 0 = Timer Hold

BIT 6 = OUTPUT ON INCREMENT
- 1 = Timer Byte Output to Bus When it Increments
- 0 = Timer Byte not Output on Increment

BIT 5 = OUTPUT ON CARRY
- 1 = Timer Byte Output to Bus When it Rolls over to 0
- 0 = Timer Byte Not Output on Roll Over

BIT 4 = STOP AT CARRY
- 1 = Timer Stops When it Rolls Over
- 0 = Timer Does Not Stop When it Rolls Over

BIT 3 = 0

BIT 2 = 0

BIT 1 = 0

BIT 0 = 0

(HEX 03) TIMER COUNT (AUTO INCR HEX OB)

Writing to this address sets the initial value of the TIMER COUNT. It also initializes the CLOCK DIVIDER.

(HEX 04) REFRESH RATE (AUTO INCR HEX OO)

An 8–bit register is provided for the setting of the refresh rate. Setting this register to 01 will cause refresh cycles to be inserted at the maximum rate which is one cycle. Setting this register to 00 will cause refresh to be disabled.

(HEX XX) ADDRESS LO (AUTO INCR HEX XX)

(HEX 10) = Channel 1 (AUTO INCR HEX 18)
(HEX 20) = Channel 2 (AUTO INCR HEX 28)
(HEX 30) = Channel 3 (AUTO INCR HEX 38)

Low byte of the initial value for the DMA ADDRESS

(HEX XX) ADDRESS HI (AUTO INCR HEX XX)

(HEX 11) = Channel 1 (AUTO INCR HEX 19)
(HEX 21) = Channel 2 (AUTO INCR HEX 29)
(HEX 31) = Channel 3 (AUTO INCR HEX 39)

High byte of the initial value for DMA ADDRESS

(HEX XX) BYTE COUNT LO (AUTO INCR HEX XX)

(HEX 12) = Channel 1 (AUTO INCR HEX 1A)
(HEX 22) = Channel 2 (AUTO INCR HEX 2A)
(HEX 32) = Channel 3 (AUTO INCR HEX 3A)

Low byte of the initial value for the BYTE COUNT for the transfer. Set this to N-1 to transfer N bytes.

(HEX XX) BYTE COUNT HI (AUTO INCR HEX XX)

(HEX 13) = Channel 1 (AUTO INCR HEX 1C)
(HEX 23) = Channel 2 (AUTO INCR HEX 2C)
(HEX 33) = Channel 3 (AUTO INCR HEX 3C)

High byte for the initial value for the BYTE COUNT

(HEX XX) COMMAND (AUTO INCR HEX XX)

(HEX 14) = Channel 1 (AUTO INCR HEX 1D)
(HEX 24) = Channel 2 (AUTO INCR HEX 2D)
(HEX 34) = Channel 3 (AUTO INCR HEX 3D)

Writing to these addresses STARTS, STOPS or CONTINUES the DMA operation.

BIT 7 = ENABLE CHANNEL
- 1 = Enable Channel to Respond to DMA Request
- 0 = Disable Channel so it Ignores DMA Request

BIT 6 = INITIALIZE ADDRESS
- 1 = Set Address to Initial Value
- 0 = Leave Address at Previous Value

BIT 5 = INITIALIZE COUNT
- 1 = Set Count to Initial Value
- 0 = Leave Count at Previous Value

BIT 4 = AUTO INITIALIZE
- 1 = Address and Byte Count Are Reset to Initial Values When Byte Count Reaches Zero. DMA Operation Continues
- 0 = DMA Operation Stops When Byte Count Reaches Zero.

BIT 3 = WRITE TO MEMORY
1 = DMA Write to Memory
0 = DMA Read from Memory

BIT 2 = EXTERNAL STOP
1 = Stop Line is Driven from External Source
0 = RB1002 Drives Stop Line

BIT 1 = EXTERNAL WRITE CONTROL
1 = Write Line is An Input for This Channel
0 = RB1002 Drives Write Line

BIT 0 = ADDRESS INCREMENT MODE
1 = Increment Address after Every DMA Read Or Write
0 = Decrement Address after Every DMA Read Or Write

Read Registers Addresses

(HEX 00) TIMER COUNT (AUTO INCR HEX 08)

Current value of the TIMER COUNT.

(HEX 01) CH 1 STATUS (AUTO INCR HEX 09)

SEE WRITE UP AT READ ADDRESS 14

(HEX 02) CH 2 STATUS (AUTO INCR HEX 0A)

SEE WRITE UP AT READ ADDRESS 24

(HEX 03) CH 3 STATUS (AUTO INCR HEX 0B)

SEE WRITE UP AT READ ADDRESS 34

(HEX 04) TIMER COUNT (AUTO INCR HEX 00)

Current value of the TIMER COUNT

(HEX XX) ADDRESS LO (AUTO INCR HEX XX)

(HEX 10) = Channel 1 (AUTO INCR HEX 18)
(HEX 20) = Channel 2 (AUTO INCR HEX 28)
(HEX 30) = Channel 3 (AUTO INCR HEX 38)

Current address low byte

(HEX XX) ADDRESS HI (AUTO INCR HEX XX)

(HEX 11) = Channel 1 (AUTO INCR HEX 19)
(HEX 21) = Channel 2 (AUTO INCR HEX 29)
(HEX 31) = Channel 3 (AUTO INCR HEX 39)

Current address high byte

(HEX XX) BYTE COUNT LO (AUTO INCR HEX XX)

(HEX 12) = Channel 1 (AUTO INCR HEX 1A)
(HEX 22) = Channel 2 (AUTO INCR HEX 2A)
(HEX 32) = Channel 3 (AUTO INCR HEX 3A)

Current BYTE COUNT

(HEX XX) BYTE COUNT HI (AUTO INCR HEX XX)

(HEX 13) = Channel 1 (AUTO INCR HEX 1B)
(HEX 23) = Channel 2 (AUTO INCR HEX 2B)
(HEX 33) = Channel 3 (AUTO INCR HEX 3B)

Current BYTE COUNT

(HEX XX) STATUS (AUTO INCR HEX XX)

(HEX 14) = Channel 1 (AUTO INCR HEX 1C)
(HEX 24) = Channel 2 (AUTO INCR HEX 2C)
(HEX 34) = Channel 3 (AUTO INCR HEX 3C)

The following STATUS information is also available at READ addresses 01, 02 and 03

BIT 7 = CHANNEL ENABLE
1 = Channel is Enabled
0 = Channel is Disabled

BIT 6 = ADDRESS CARRY
1 = Address is at FFFF if Counting up; Address is at OOOO if Counting down
0 = Not at Carry

BIT 5 = TERMINAL COUNT
1 = Byte Count is at Zero
0 = Byte Count is Not Zero

BIT 4 = AUTO INITIALIZE
1 = Auto Initialize Mode
0 = Stop at Terminal Count

BIT 3 = WRITE TO MEMORY
1 = DMA Write to Memory Mode
0 = DMA Read from Memory Mode

BIT 2 = EXTERNAL STOP
1 = Stop is Input
0 = Stop is Output

BIT 1 = EXTERNAL WRITE CONTROL
1 = Write is Externally Controlled
0 = Write is Internally Controlled

BIT 0 = ADDRESS INCREMENT MODE
1 = Address Counts up
0 = Address Counts down

Dynamic RAM Refresh

The UM83C002 has built-in refresh circuitry for dynamic RAMs. It provides 8 bits of refresh address so that dynamic RAMs up to 256 K bits can be accommodated.

An 8 bit register is also provided for the setting of the refresh rate. Setting this register to 01 will cause refresh cycles to be inserted at the maximum rate which is one cycle out of two. Activating the $\overline{\text{RESET}}$ line also sets the refresh to its maximum rate. Setting this register to 255 will cause one refresh cycle to be inserted for every 256 memory cycles. Setting this register to 00 will cause refresh to be disabled.

The refresh cycles are inserted into otherwise unused memory cycles whenever possible to maximize system performance. For example: If the rate register is set to 255 and there are any unused cycles during the first 255 cycles of the refresh period, the refresh will be inserted into the first of them and it will be totally invisible to the rest of the system.

During a refresh cycle, the $\overline{\text{ACKNOWLEDGE}}$, $\overline{\text{STOP}}$ and $\overline{\text{WRITE}}$ lines will be high simultaneously. The refresh address will be on the MA0 to MA7 lines. If the refresh address is at hexadecimal FF, then the $\overline{\text{CARRY}}$ line will also be low.

Timing Specifications

This section is devoted to the timings of signals and their relationship to each other in order to make the maximum use of the UM83C002. The following tables and diagrams are to be used as design tools when incorporating the UM83C002 into your system.

Signal	Min.	Typ.	Max.	Units
MCLK		10	20	MHZ

Table 4. Clock Frequency

Signal	LO	HI	Units
MCLK	20	30	ns
ALE		20	ns
RESET	100		ns

Table 5. Signal Widths

Delays From	TO	Typ.	Max.	Units
MCLK HI	WRITE	35	70	ns
	STOP	35	69	ns
	CARRY	37	73	ns
	ACK1, ACK2	26	52	ns
	ACK	29	57	ns
	MA0 TO MA7	40	80	ns
MCLK LO	MA0 TO MA7	39	78	ns
CSEL LO & WRT HI & MCLK LO	AD0-AD7 ACTIVE	36	72	ns

Table 6. Delays

Set-Up and Hold Times	Set-Up	TO	Hold	Units
REQ3, REQ2, REQ1, REQH	15	MCLK HI	15	ns
WRITE	15	MCLK LO		ns
WRITE		MCLK HI	15	ns
CHIP SELECT	15	MCLK LO		ns
CHIP SELECT		MCLK HI	15	ns
AO	15	MCLK LO		ns
AO		MCLK HI	15	ns
STOP	15	MCLK HI	10	ns

Table 7. Set-Up and Hold Times