

# BIPOLAR ANALOG INTEGRATED CIRCUIT

# $\mu$ PC4061

## J-FET INPUT LOW-POWER OPERATIONAL AMPLIFIER

### DESCRIPTION

The  $\mu$ PC4061 is a J-FET input low-power operational amplifier featuring low supply voltage operation from  $\pm 2$  V. Supply current is ten times smaller than  $\mu$ PC4081 type J-FET input op-amp. With very low input bias current characteristics, the  $\mu$ PC4061 is an excellent choice for hand-held measurement equipment and other low-power application circuits.

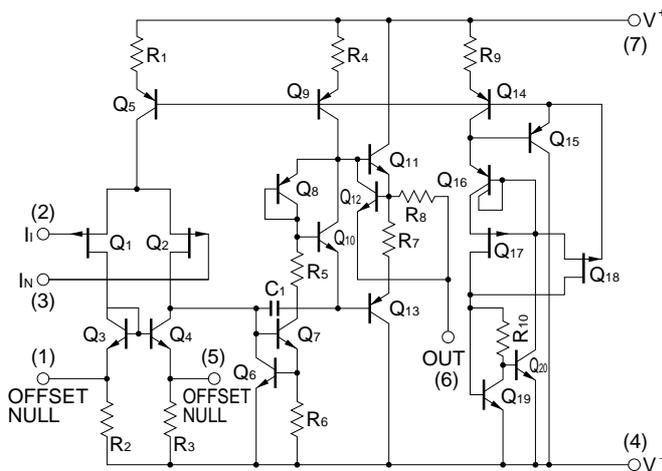
### FEATURES

- Low supply current: 220  $\mu$ A (TYP.)
- Very low input bias and offset currents
- Offset voltage null capability
- High input impedance...J-FET Input Stage
- Low supply voltage operation
- Output short circuit protection
- Internal frequency compensation

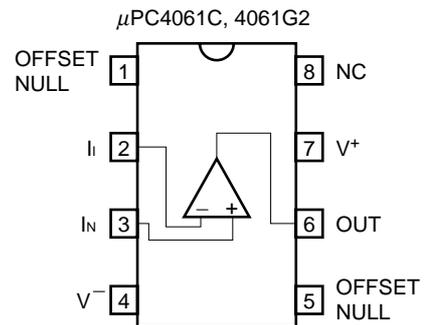
### ORDERING INFORMATION

Part Number	Package
$\mu$ PC4061C	8-pin plastic DIP (7.62 mm (300))
$\mu$ PC4061G2	8-pin plastic SOP (5.72 mm (225))

### EQUIVALENT CIRCUIT



### PIN CONFIGURATION (Top View)



Remark NC : No Connection

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**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25 °C)**

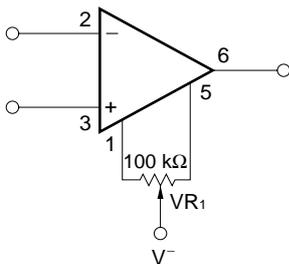
Parameter	Symbol	Ratings	Unit	
Voltage between V <sup>+</sup> and V <sup>-</sup> <sup>Note 1</sup>	V <sup>+</sup> - V <sup>-</sup>	-0.3 to +36	V	
Differential Input Voltage	V <sub>ID</sub>	±30	V	
Input Voltage <sup>Note 2</sup>	V <sub>I</sub>	V <sup>-</sup> -0.3 to V <sup>+</sup> +0.3	V	
Output Voltage <sup>Note 3</sup>	V <sub>O</sub>	V <sup>-</sup> -0.3 to V <sup>+</sup> +0.3	V	
Power Dissipation	C Package <sup>Note 4</sup>	P <sub>T</sub>	350	mW
	G2 Package <sup>Note 5</sup>		440	mW
Output Short Circuit Duration <sup>Note 6</sup>		Indefinite	sec	
Operating Ambient Temperature	T <sub>A</sub>	-20 to +80	°C	
Storage Temperature	T <sub>stg</sub>	-55 to +125	°C	

- Notes**
- Reverse connection of supply voltage can cause destruction.
  - The input voltage should be allowed to input without damage or destruction. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The normal operation will establish when the both inputs are within the Common Mode Input Voltage Range of electrical characteristics.
  - This specification is the voltage which should be allowed to supply to the output terminal from external without damage or destructive. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The output voltage of normal operation will be the Output Voltage Swing of electrical characteristics.
  - Thermal derating factor is -5.0 mW/°C when operating ambient temperature is higher than 55 °C.
  - Thermal derating factor is -4.4 mW/°C when operating ambient temperature is higher than 25 °C.
  - Pay careful attention to the total power dissipation not to exceed the absolute maximum ratings, Note 4 and Note 5.

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage	V <sup>±</sup>	±2		±16	V
Output Source Current	I <sub>O SOURCE</sub>			5	mA
Output Sink Current	I <sub>O SINK</sub>			3.5	mA
Capacitive Load (A <sub>v</sub> = +1, R <sub>f</sub> = 0 Ω)	C <sub>L</sub>			100	pF

**OFFSET VOLTAGE NULL CIRCUIT**



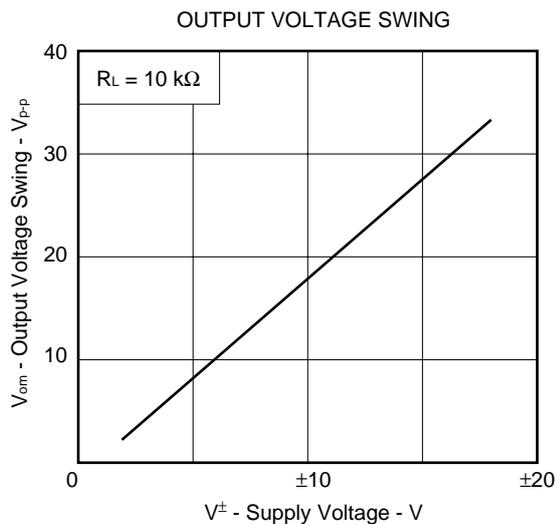
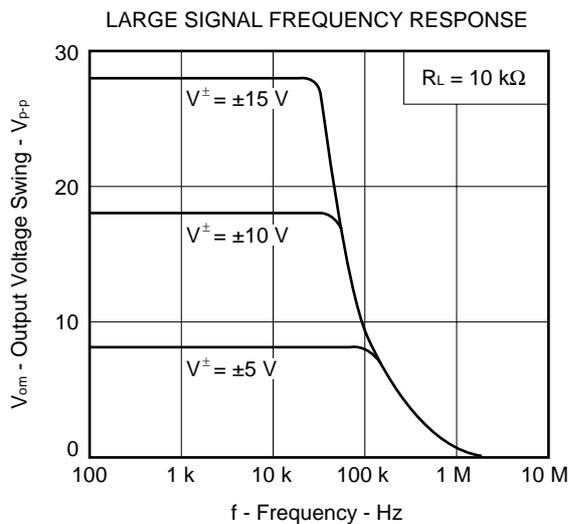
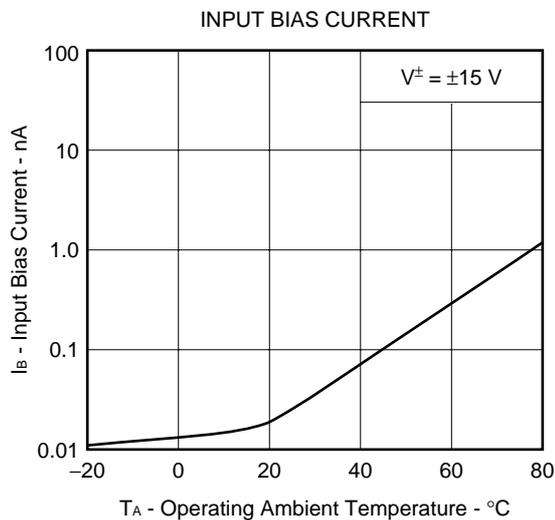
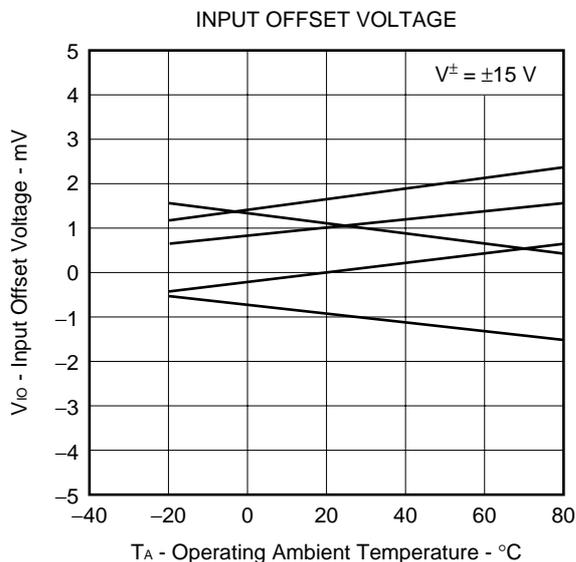
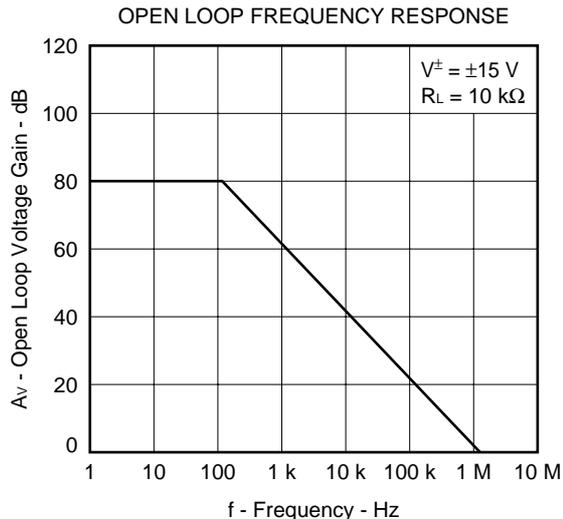
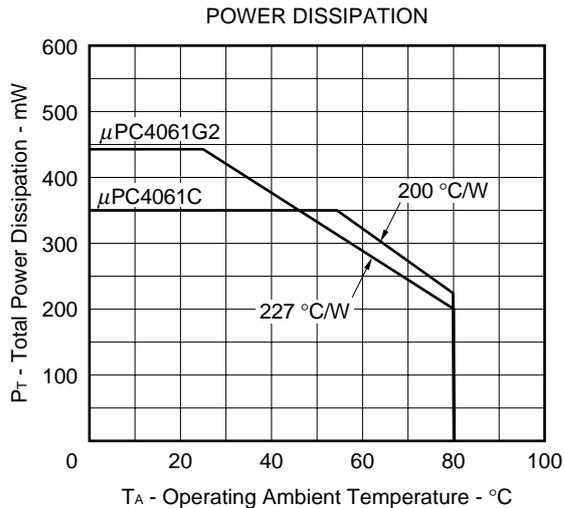
★ **Remark** The OFFSET NULL pins should be left open or connected to V<sup>-</sup> via a resistor as shown in the left figure. Don't connect to any lines other than V<sup>-</sup>, otherwise malfunction, degradation, or failure may occur.

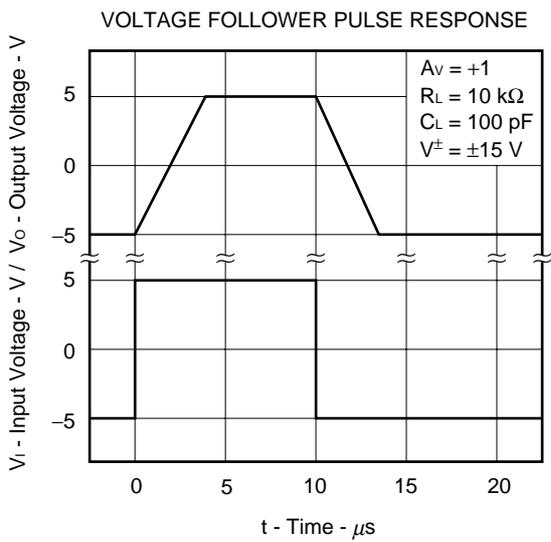
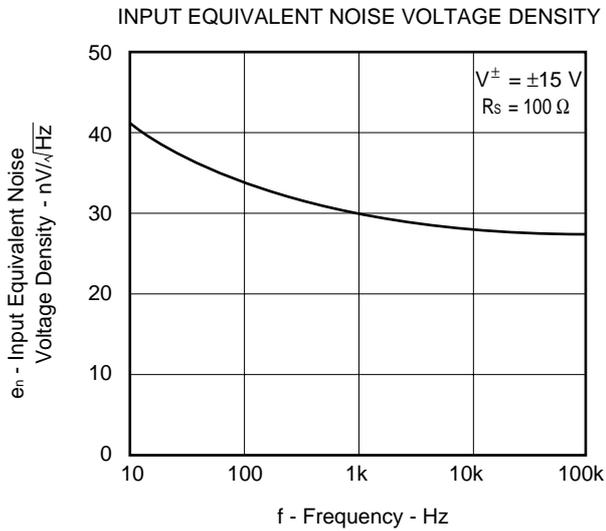
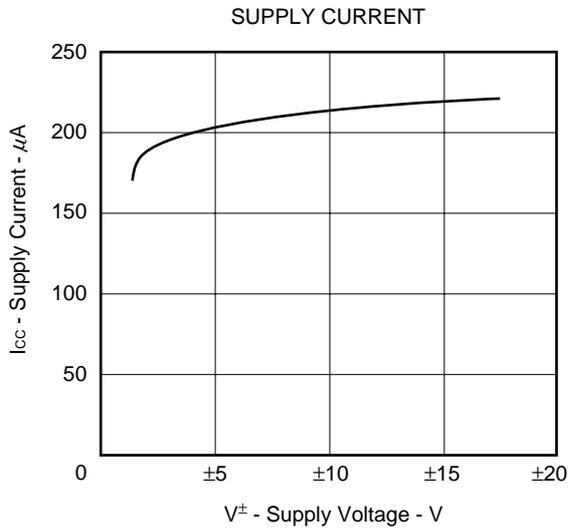
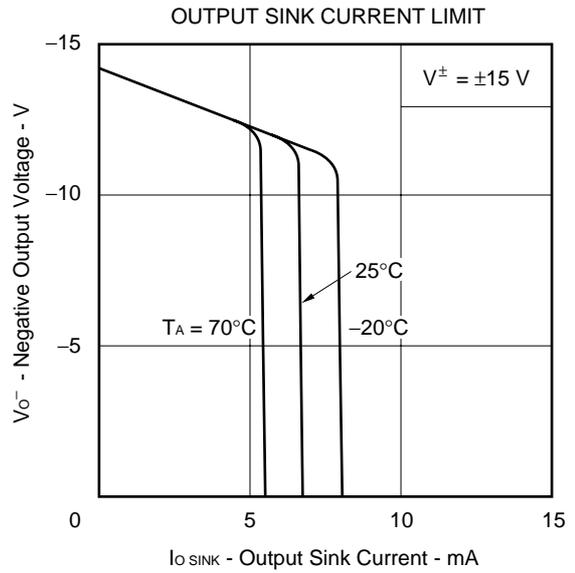
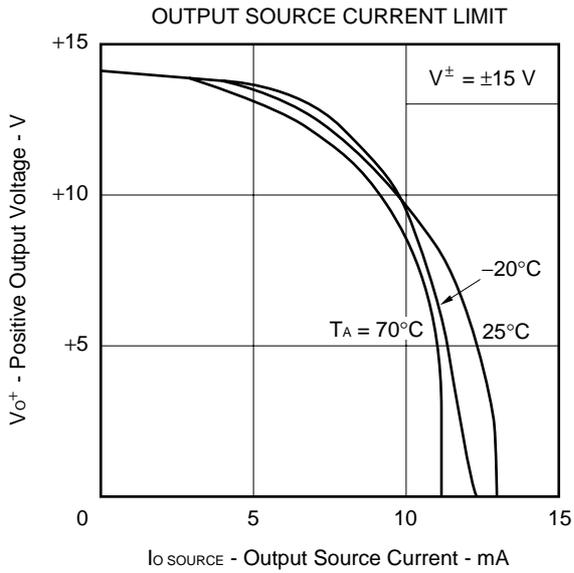
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, V<sup>±</sup> = ±15 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Offset Voltage	V <sub>IO</sub>	R <sub>S</sub> ≤ 50 Ω		±2	±10	mV
Input Offset Current <sup>Note 7</sup>	I <sub>IO</sub>			±5	±50	pA
Input Bias Current <sup>Note 7</sup>	I <sub>B</sub>			10	100	pA
Large Signal Voltage Gain	A <sub>V</sub>	R <sub>L</sub> ≥ 10 kΩ, V <sub>O</sub> = ±10 V	3000	9000		
Supply Current	I <sub>CC</sub>	I <sub>O</sub> = 0 A		220	250	μA
Common Mode Rejection Ratio	CMR		70	90		dB
Supply Voltage Rejection Ratio	SVR		70	90		dB
Output Voltage Swing	V <sub>OM</sub>	R <sub>L</sub> ≥ 10 kΩ	±12	+14.0 -13.6		V
Common Model Input Voltage Range	V <sub>ICM</sub>		±12	+15 -13		V
Slew Rate	SR	A <sub>V</sub> = 1		3		V/μs
Unity Gain Frequency	f <sub>unity</sub>			1		MHz
Input Equivalent Noise Voltage Density	e <sub>n</sub>	R <sub>S</sub> = 100 Ω, f = 1 kHz		30		nV/√Hz
Input Offset Voltage	V <sub>IO</sub>	R <sub>S</sub> ≤ 50 Ω, T <sub>A</sub> = -20 to +70 °C			±15	mV
Average V <sub>IO</sub> Temperature Drift	ΔV <sub>IO</sub> /ΔT	T <sub>A</sub> = -20 to +70 °C		±10		μV/°C
Input Offset Current <sup>Note 7</sup>	I <sub>IO</sub>	T <sub>A</sub> = -20 to +70 °C			±2	nA
Input Bias Current <sup>Note 7</sup>	I <sub>B</sub>	T <sub>A</sub> = -20 to +70 °C			3.5	nA

**Notes 7.** Input bias currents flow into IC. Because each currents are gate leak current of P-channel J-FET on input stage. And that are temperature sensitive. Short time measuring method is recommendable to maintain the junction temperature close to the operating ambient temperature.

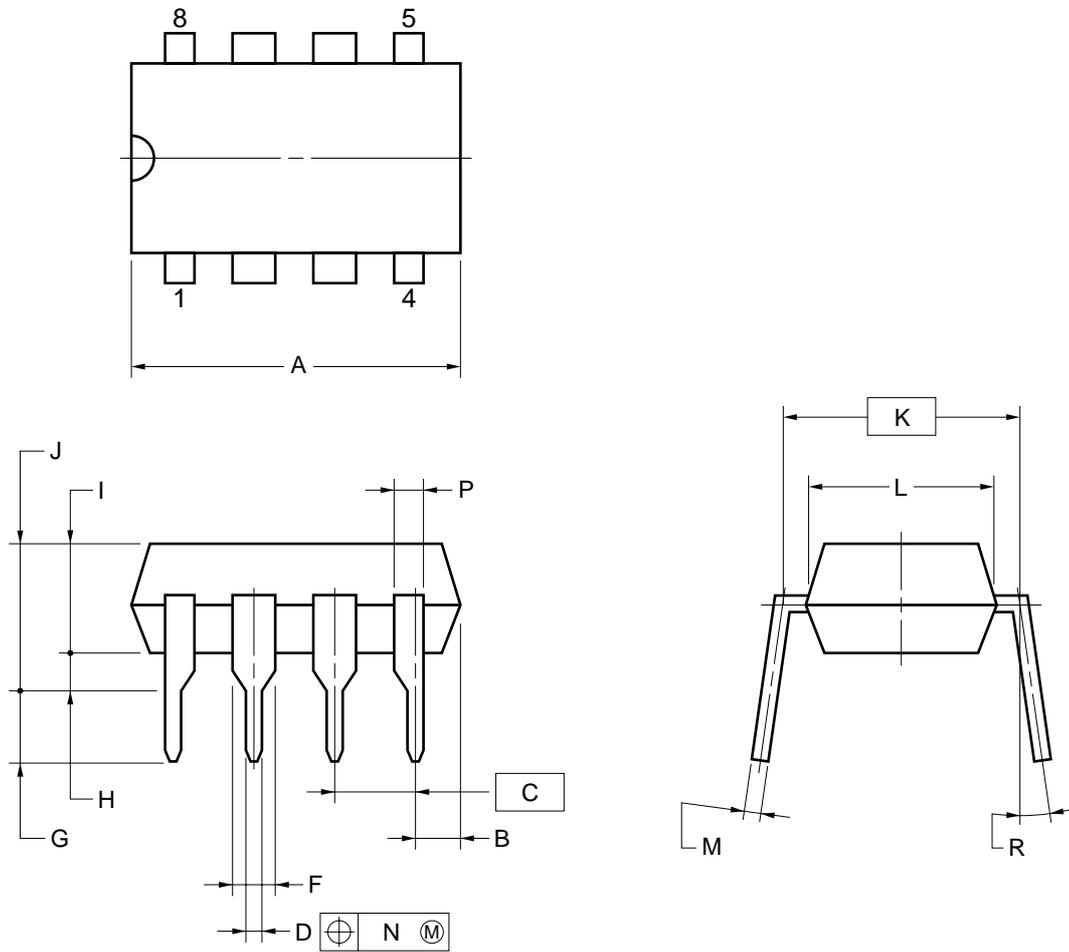
TYPICAL PERFORMANCE CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ , TYP.)





★ PACKAGE DRAWINGS (Unit : mm)

8-PIN PLASTIC DIP (7.62mm(300))



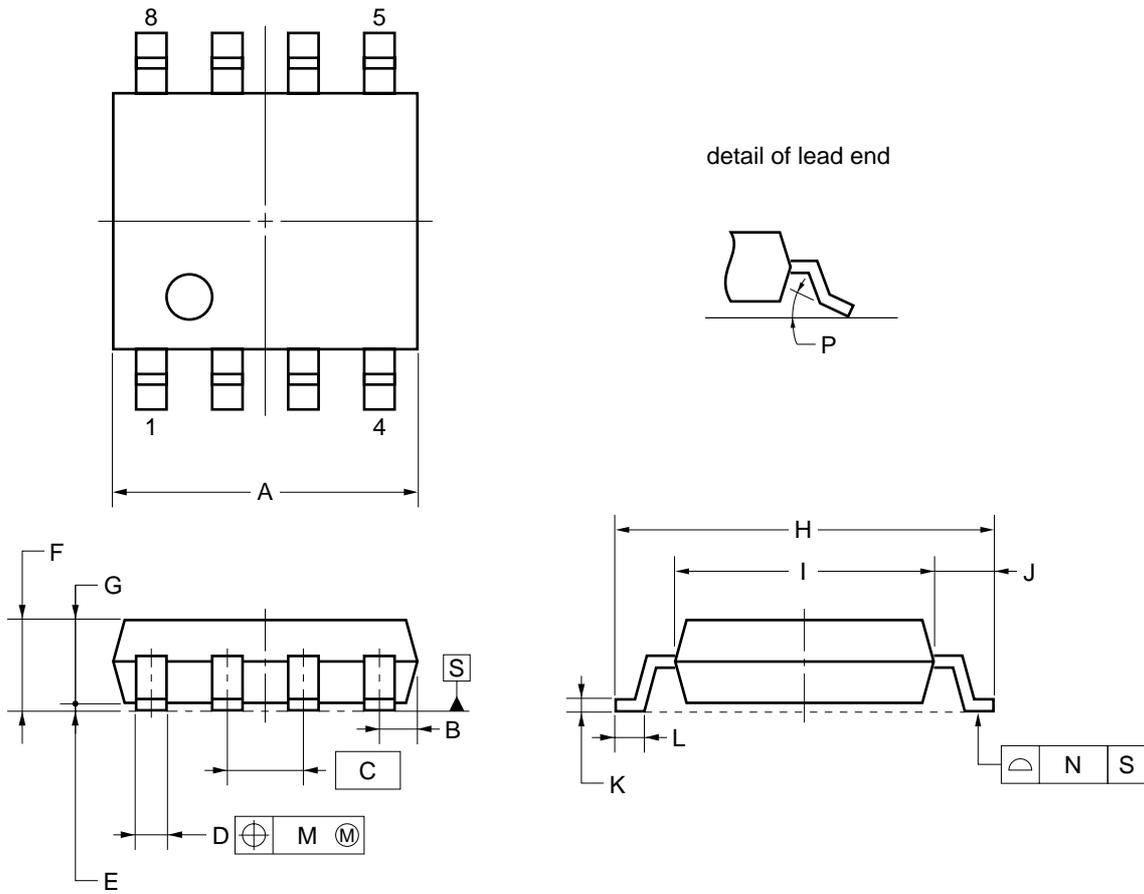
NOTES

1. Each lead centerline is located within 0.25 mm of its true position (T.P.) at maximum material condition.
2. Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS
A	10.16 MAX.
B	1.27 MAX.
C	2.54 (T.P.)
D	0.50±0.10
F	1.4 MIN.
G	3.2±0.3
H	0.51 MIN.
I	4.31 MAX.
J	5.08 MAX.
K	7.62 (T.P.)
L	6.4
M	0.25 <sup>+0.10</sup> <sub>-0.05</sub>
N	0.25
P	0.9 MIN.
R	0~15°

P8C-100-300B,C-2

8-PIN PLASTIC SOP (5.72 mm (225))



**NOTE**

Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	5.2 $\begin{smallmatrix} +0.17 \\ -0.20 \end{smallmatrix}$
B	0.78 MAX.
C	1.27 (T.P.)
D	0.42 $\begin{smallmatrix} +0.08 \\ -0.07 \end{smallmatrix}$
E	0.1±0.1
F	1.59±0.21
G	1.49
H	6.5±0.3
I	4.4±0.15
J	1.1±0.2
K	0.17 $\begin{smallmatrix} +0.08 \\ -0.07 \end{smallmatrix}$
L	0.6±0.2
M	0.12
N	0.10
P	3° $\begin{smallmatrix} +7° \\ -3° \end{smallmatrix}$

S8GM-50-225B-6

★ **RECOMMENDED SOLDERING CONDITIONS**

When soldering this product, it is highly recommended to observe the conditions as shown below. If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL"(C10535E).

**Type of Surface Mount Device**

**μPC4061G2: 8-pin plastic SOP (5.72 mm (225))**

Process	Conditions	Symbol
Infrared Ray Reflow	Peak temperature: 230 °C or below (Package surface temperature), Reflow time: 30 seconds or less (at 210 °C or higher), Maximum number of reflow processes: 1 time.	IR30-00-1
Vapor Phase Soldering	Peak temperature: 215 °C or below (Package surface temperature), Reflow time: 40 seconds or less (at 200 °C or higher), Maximum number of reflow processes: 1 time.	VP15-00-1
Wave Soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or less, Maximum number of flow processes: 1 time, Pre-heating temperature: 120 °C or below (Package surface temperature).	WS60-00-1
Partial Heating Method	Pin temperature: 300 °C or below, Heat time: 3 seconds or less (Per each side of the device).	—

**Caution** Apply only one kind of soldering condition to a device, except for "partial heating method", or the device will be damaged by heat stress.

**Type of Through-hole Device**

**μPC4061C: 8-pin plastic DIP (7.62 mm (300))**

Process	Conditions
Wave Soldering (only to leads)	Solder temperature: 260 °C or below, Flow time: 10 seconds or less.
Partial Heating Method	Pin temperature: 300 °C or below, Heat time: 3 seconds or less (per each lead).

**Caution** For through-hole device, the wave soldering process must be applied only to leads, and make sure that the package body does not get jet soldered.

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