



DATA SHEET

BIPOLAR ANALOG INTEGRATED CIRCUIT μ PC8163TB

SILICON MMIC 2.0 GHz FREQUENCY UP-CONVERTER FOR CELLULAR TELEPHONE

DESCRIPTION

The μ PC8163TB is a silicon monolithic integrated circuit designed as frequency up-converter for cellular telephone transmitter stage. The μ PC8163TB has improved intermodulation performance and smaller package.

The μ PC8163TB is manufactured using NEC's 20 GHz μ NESATTMIII silicon bipolar process. This process uses silicon nitride passivation film and gold electrodes. These materials can protect chip surface from external pollution and prevent corrosion/migration. Thus, this IC has excellent performance, uniformity and reliability.

FEATURES

- Recommended operating frequency : $f_{RFout} = 0.8$ to 2.0 GHz, $f_{IFin} = 50$ to 300 MHz
- Supply voltage : $V_{CC} = 2.7$ to 3.3 V
- High-density surface mounting : 6-pin super minimold package
- Higher IP₃ : OIP₃ = +9.5 dBm @ $f_{RFout} = 830$ MHz
- Minimized carrier leakage : Due to double balanced mixer

APPLICATION

- Digital cellular phones

ORDERING INFORMATION

Part Number	Package	Marking	Supplying Form
μ PC8163TB-E3	6-pin super minimold	C2Y	Embossed tape 8 mm wide. Pin 1, 2, 3 face the tape perforation side. Qty 3 kpcs/reel

Remark To order evaluation samples, please contact your local NEC sales office (Part number for sample order: μ PC8163TB).

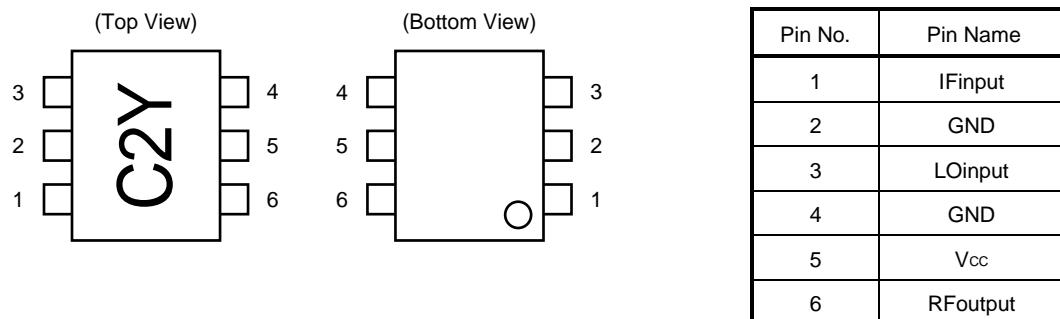
Caution Electro-static sensitive devices

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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1. PIN CONNECTIONS



★ 2. PRODUCT LINE-UP ($T_A = +25^\circ\text{C}$, $V_{cc} = V_{RFout} = 3.0 \text{ V}$, $Z_S = Z_L = 50 \Omega$)

Part Number	I _{cc} (mA)	f _{RFout} (GHz)	CG (dB)		
			@RF 0.9 GHz ^{Note}	@RF 1.9 GHz	@RF 2.4 GHz
μ PC8106TB	9	0.4 to 2.0	9	7	–
μ PC8109TB	5	0.4 to 2.0	6	4	–
μ PC8163TB	16.5	0.8 to 2.0	9	5.5	–
μ PC8172TB	9	0.8 to 2.5	9.5	8.5	8.0
μ PC8187TB	15	0.8 to 2.5	11	11	10

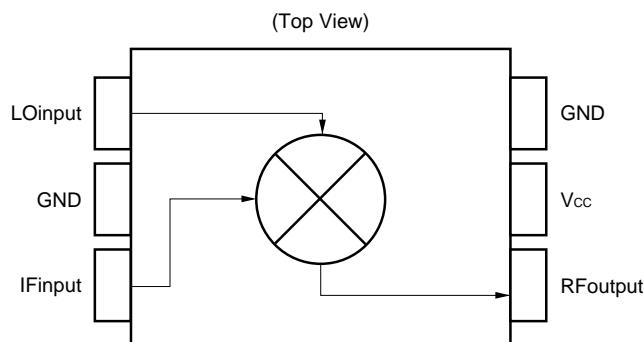
Part Number	P _{O(sat)} (dBm)			OIP ₃ (dBm)		
	@RF 0.9 GHz ^{Note}	@RF 1.9 GHz	@RF 2.4 GHz	@RF 0.9 GHz ^{Note}	@RF 1.9 GHz	@RF 2.4 GHz
μ PC8106TB	–2	–4	–	+5.5	+2.0	–
μ PC8109TB	–5.5	–7.5	–	+1.5	–1.0	–
μ PC8163TB	+0.5	–2	–	+9.5	+6.0	–
μ PC8172TB	+0.5	0	–0.5	+7.5	+6.0	+4.0
μ PC8187TB	+4	+2.5	+1	+10	+10	+8.5

Note f_{RFout} = 0.83 GHz @ μ PC8163TB and μ PC8187TB

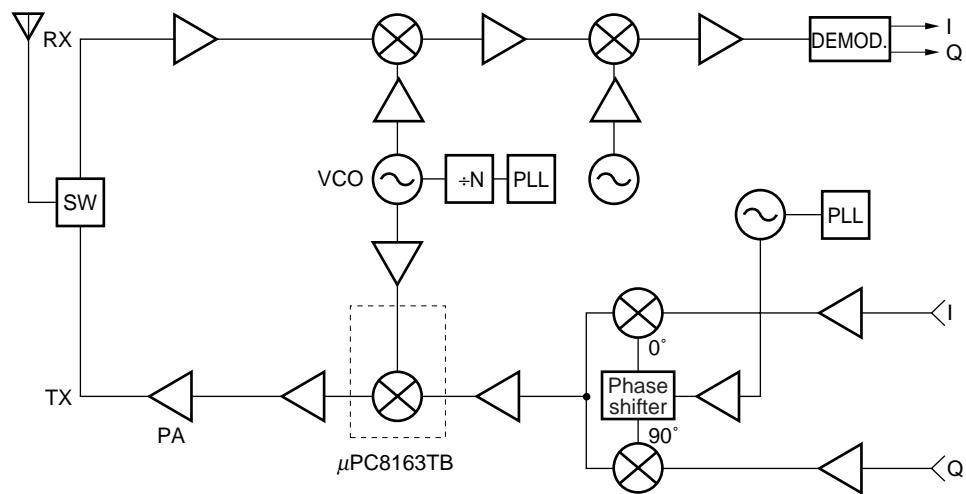
Remark Typical performance. Please refer to **ELECTRICAL CHARACTERISTICS** in detail.

To know the associated product, please refer to each latest data sheet.

3. INTERNAL BLOCK DIAGRAM (for the μ PC8163TB)



4. SYSTEM APPLICATION EXAMPLE (schematics of IC location in the system)



5. PIN EXPLANATION

Pin No.	Pin Name	Applied Voltage (V)	Pin Voltage Note (V)	Function and Explanation	Equivalent Circuit
1	IFinput	—	1.2	This pin is IF input to double balanced mixer (DBM). The input is designed as high impedance. The circuit contributes to suppress spurious signal. Also this symmetrical circuit can keep specified performance insensitive to process-condition distribution. For above reason, double balanced mixer is adopted.	
2 4	GND	GND	—	GND pin. Ground pattern on the board should be formed as wide as possible. Track Length should be kept as short as possible to minimize ground impedance.	
3	LOinput	—	2.1	Local input pin. Recommendable input level is -10 to 0 dBm.	
5	Vcc	2.7 to 3.3	—	Supply voltage pin.	
6	RFoutput	Same bias as Vcc through external inductor	—	This pin is RF output from DBM. This pin is designed as open collector. Due to the high impedance output, this pin should be externally equipped with LC matching circuit to next stage.	

Note Each pin voltage is measured at $V_{CC} = V_{RFout} = 3.0\text{ V}$.

6. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Rating	Unit
Supply Voltage	V _{CC}	T _A = +25°C, Pin 5 and 6	3.6	V
★ Package Power Dissipation	P _D	Mounted on double-sided copperclad 50 × 50 × 1.6 mm epoxy glass PWB T _A = +85°C	270	mW
Operating Ambient Temperature	T _A		-40 to +85	°C
Storage Temperature	T _{STG}		-55 to +150	°C
Maximum Input Power	P _{IN}		+10	dBm

7. RECOMMENDED OPERATING RANGE

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remarks
Supply Voltage	V _{CC}	2.7	3.0	3.3	V	The same voltage should be applied to pin 5 and 6
Operating Ambient Temperature	T _A	-40	+25	+85	°C	
Local Input Power	P _{LOin}	-10	-5	0	dBm	Z _S = 50 Ω (without matching)
RF Output Frequency	f _{RFout}	0.8	-	2.0	GHz	With external matching circuit
IF Input Frequency	f _{IFin}	50	-	300	MHz	

8. ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = V_{RFout} = 3.0 V, f_{IFin} = 150 MHz, P_{LOin} = -5 dBm)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Circuit Current	I _{CC}	No input signal	11.5	16.5	23	mA
Conversion Gain 1	CG1	f _{RFout} = 830 MHz, P _{IFin} = -20 dBm	6	9	12	dB
Conversion Gain 2	CG2	f _{RFout} = 1.9 GHz, P _{IFin} = -20 dBm	2.5	5.5	8.5	dB
Saturated Output Power 1	P _{O(sat) 1}	f _{RFout} = 830 MHz, P _{IFin} = 0 dBm	-1.5	+0.5	-	dBm
Saturated Output Power 2	P _{O(sat) 2}	f _{RFout} = 1.9 GHz, P _{IFin} = 0 dBm	-4.5	-2	-	dBm

9. OTHER CHARACTERISTICS, FOR REFERENCE PURPOSES ONLY

(T_A = +25°C, V_{CC} = V_{RFout} = 3.0 V, P_{LOin} = -5 dBm)

Parameter	Symbol	Conditions		Reference Value	Unit
3rd Order Distortion Input Intercept Point	IIP ₃ 1	f _{IFin1} = 150.0 MHz	f _{RFout} = 830 MHz	+0.5	dBm
	IIP ₃ 2	f _{IFin2} = 150.4 MHz	f _{RFout} = 1.9 GHz	+0.5	
3rd Order Distortion Output Intercept Point	OIP ₃ 1	f _{IFin1} = 150.0 MHz	f _{RFout} = 830 MHz	+9.5	dBm
	OIP ₃ 2	f _{IFin2} = 150.4 MHz	f _{RFout} = 1.9 GHz	+6.0	
SSB Noise Figure	SSB • NF	f _{RFout} = 830 MHz, f _{IFin} = 150 MHz		12.5	dB

10. TEST CIRCUIT

10.1 Test Circuit 1 ($f_{RFout} = 830$ MHz)

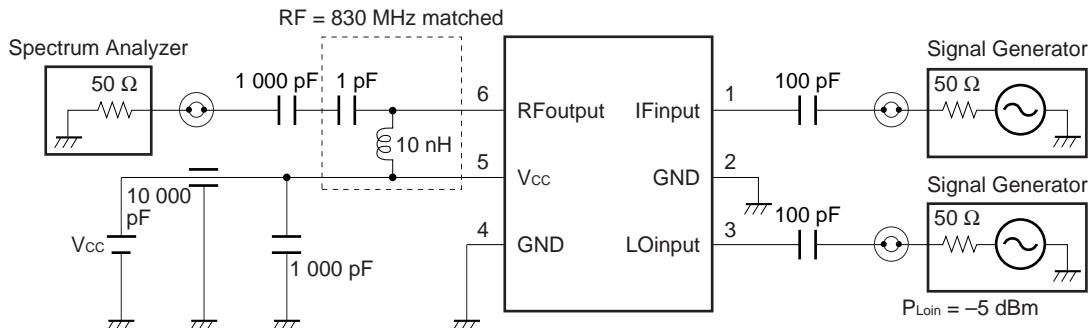
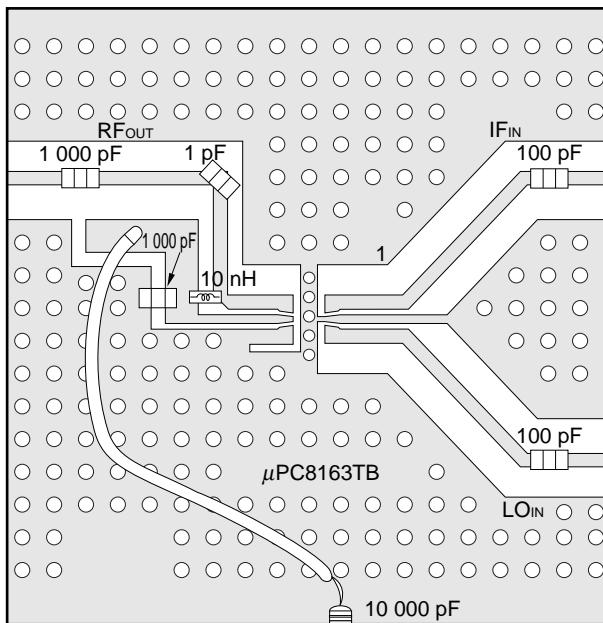


ILLUSTRATION OF TEST CIRCUIT 1 ASSEMBLED ON EVALUATION BOARD



EVALUATION BOARD CHARACTERS

- (1) Double-sided copper clad $35 \times 42 \times 0.4$ mm polyimide board
- (2) Back side: GND pattern
- (3) Solder plated patterns
- (4) ○○: Through holes

Caution Test circuit or print pattern in this sheet is for testing IC characteristics.

In the case of actual system application, external circuits including print pattern and matching circuit constant of output port should be designed in accordance with IC's S parameters and environmental components.

10.2 Test Circuit 2 ($f_{RFout} = 1.9$ GHz)

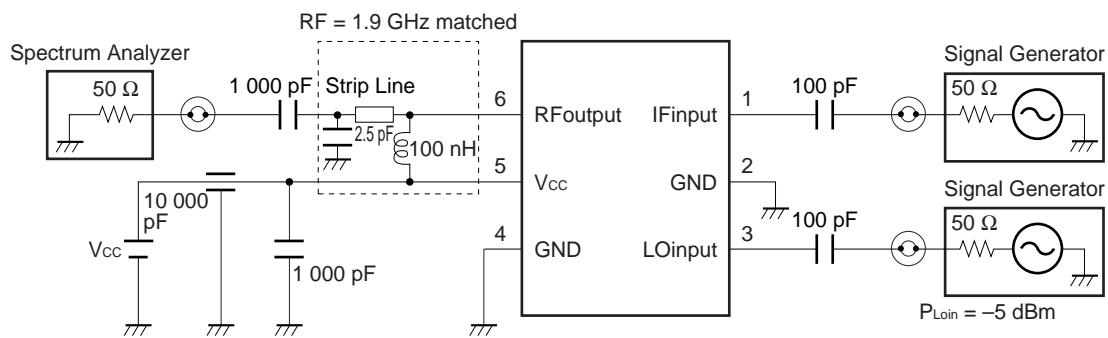
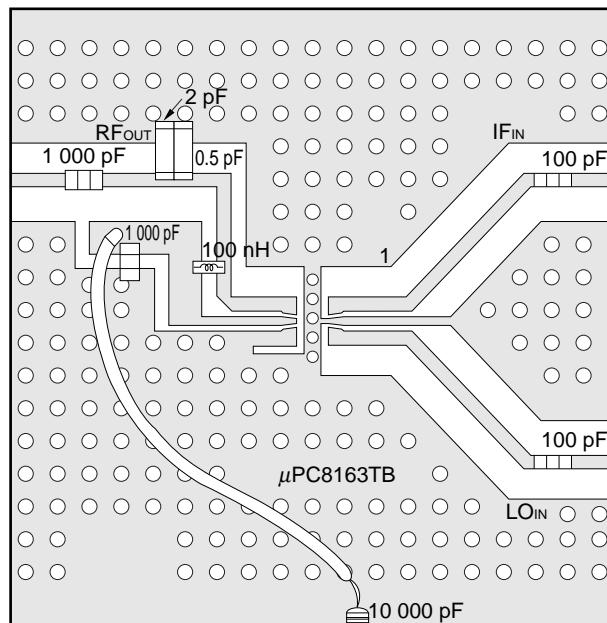


ILLUSTRATION OF TEST CIRCUIT 2 ASSEMBLED ON EVALUATION BOARD

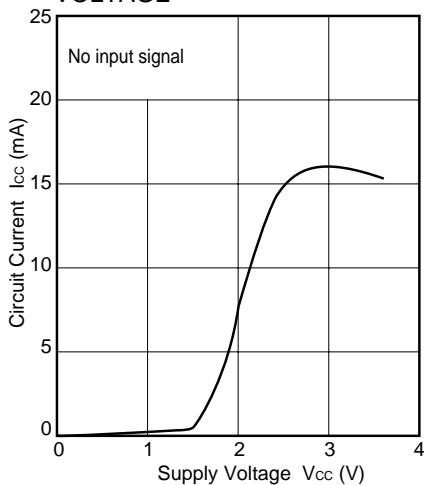


EVALUATION BOARD CHARACTERS

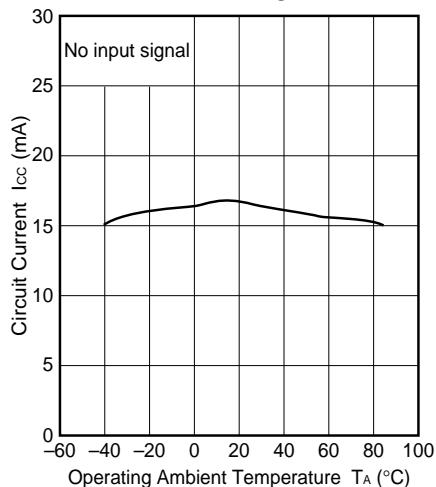
- (1) Double-sided copper clad $35 \times 42 \times 0.4$ mm polyimide board
- (2) Back side: GND pattern
- (3) Solder plated patterns
- (4) ○○: Through holes

11. TYPICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$, unless otherwise specified $V_{CC} = V_{RFout}$)

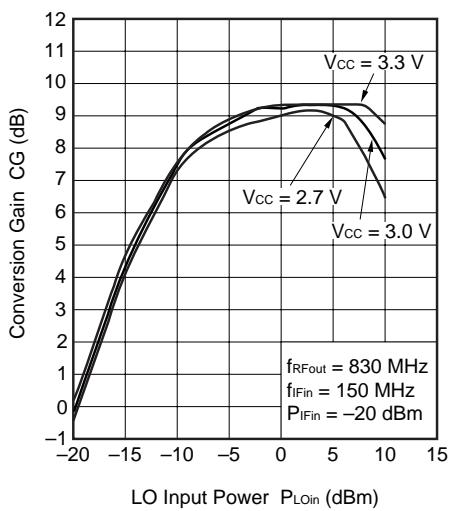
CIRCUIT CURRENT vs. SUPPLY VOLTAGE



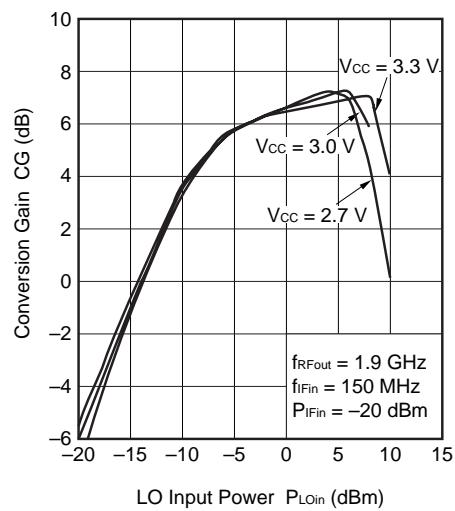
CIRCUIT CURRENT vs. OPERATING AMBIENT TEMPERATURE



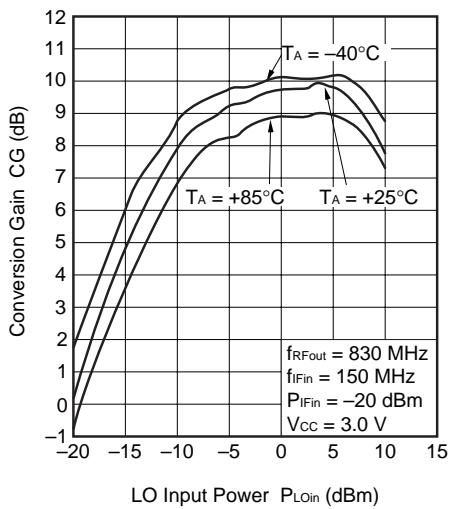
CONVERSION GAIN vs. LO INPUT POWER



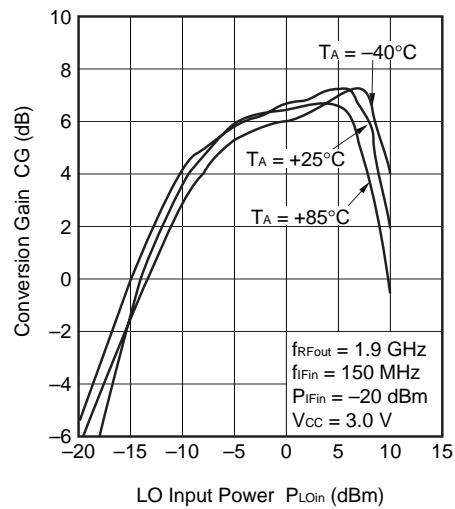
CONVERSION GAIN vs. LO INPUT POWER



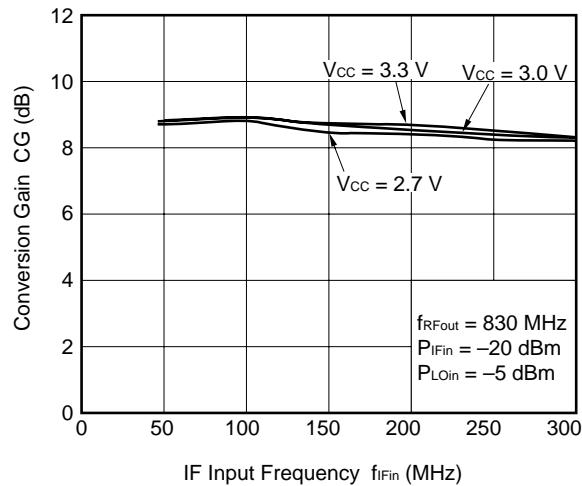
CONVERSION GAIN vs. LO INPUT POWER



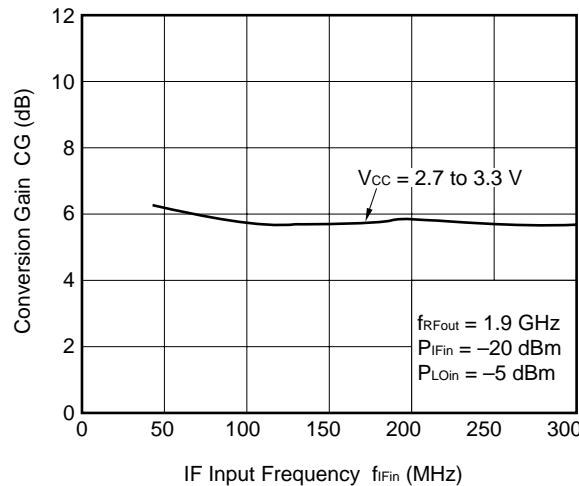
CONVERSION GAIN vs. LO INPUT POWER



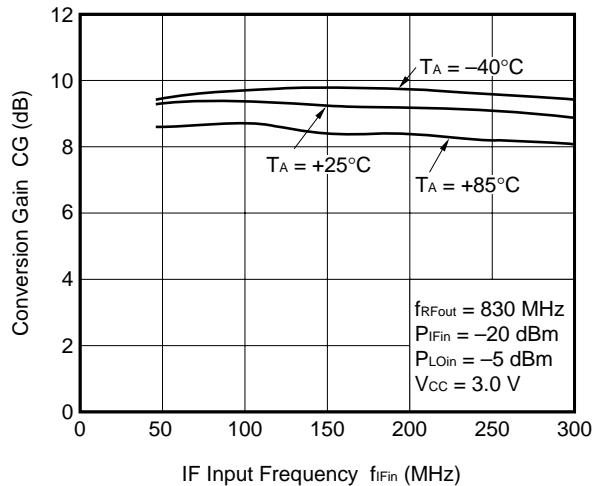
CONVERSION GAIN vs. IF INPUT FREQUENCY



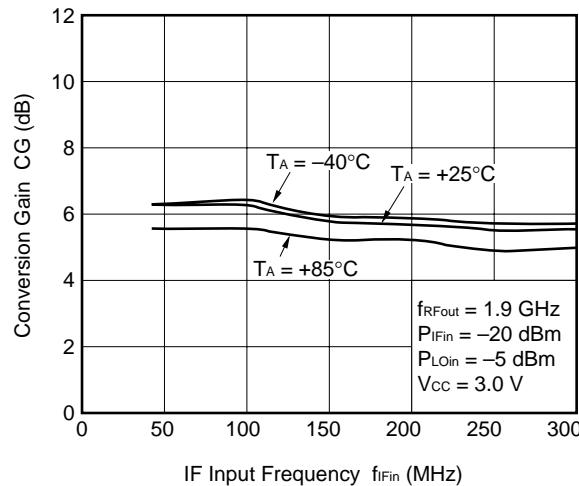
CONVERSION GAIN vs. IF INPUT FREQUENCY



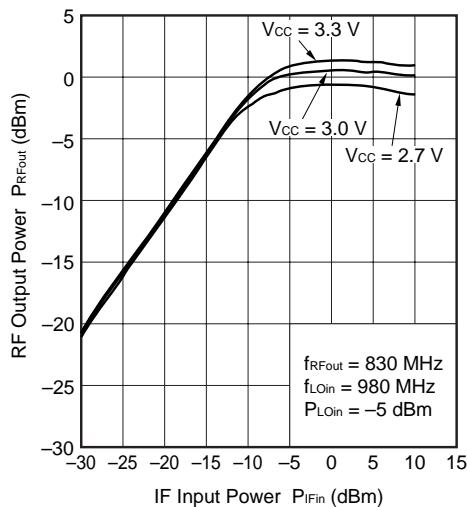
CONVERSION GAIN vs. IF INPUT FREQUENCY



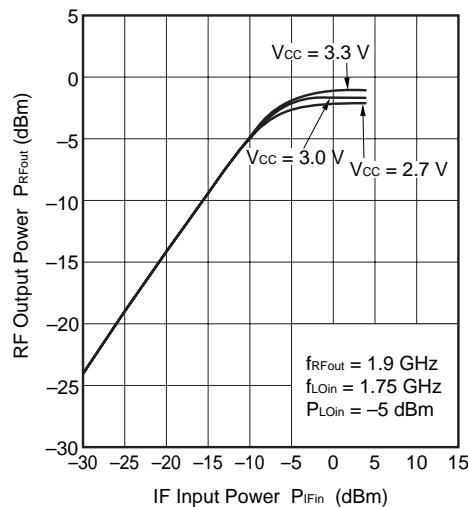
CONVERSION GAIN vs. IF INPUT FREQUENCY



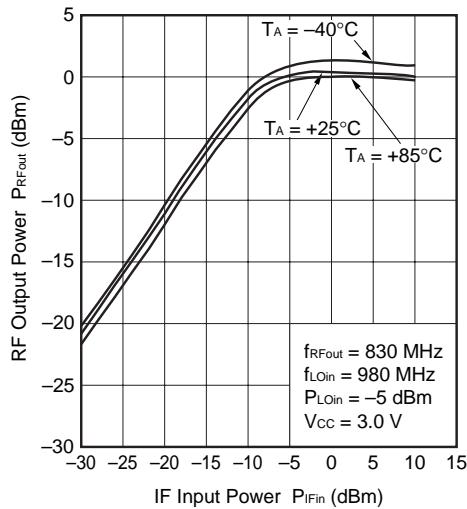
RF OUTPUT POWER vs. IF INPUT POWER



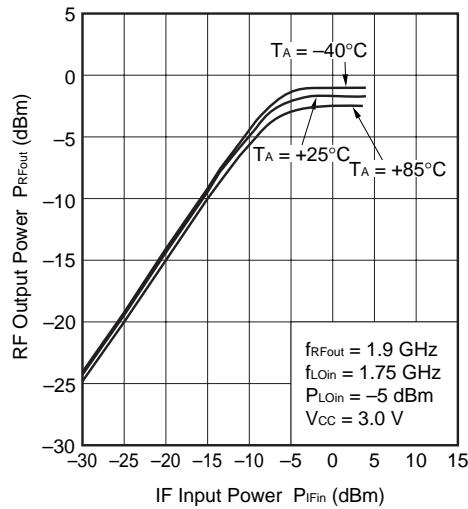
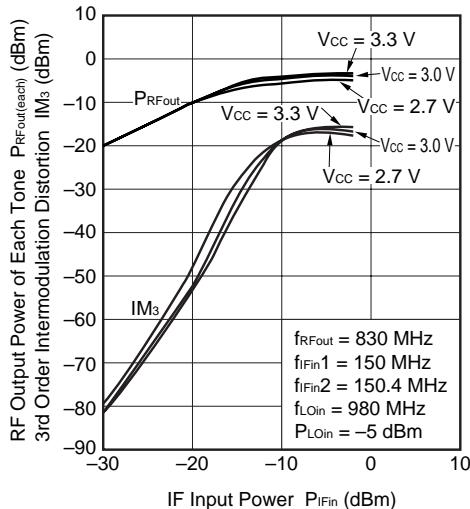
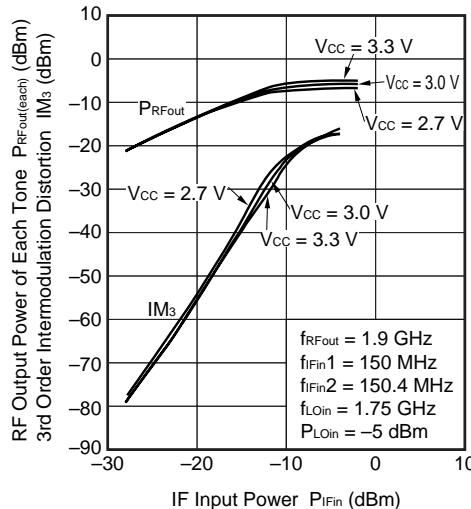
RF OUTPUT POWER vs. IF INPUT POWER



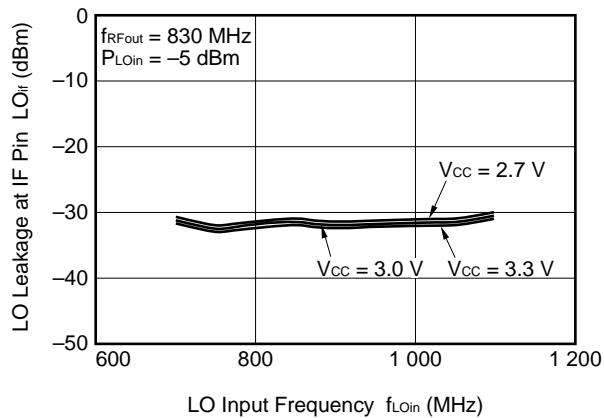
RF OUTPUT POWER vs. IF INPUT POWER



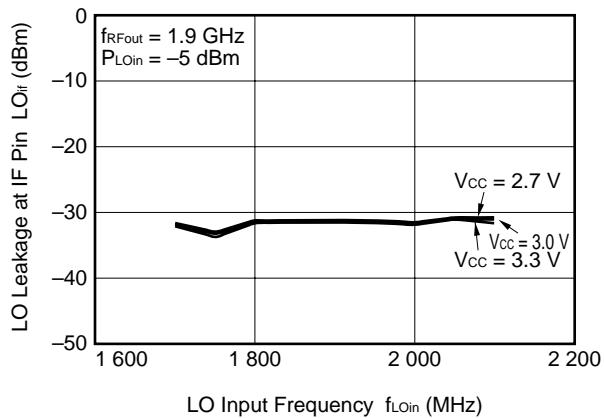
RF OUTPUT POWER vs. IF INPUT POWER

RF OUTPUT POWER OF EACH TONE, IM₃ vs. IF INPUT POWERRF OUTPUT POWER OF EACH TONE, IM₃ vs. IF INPUT POWER

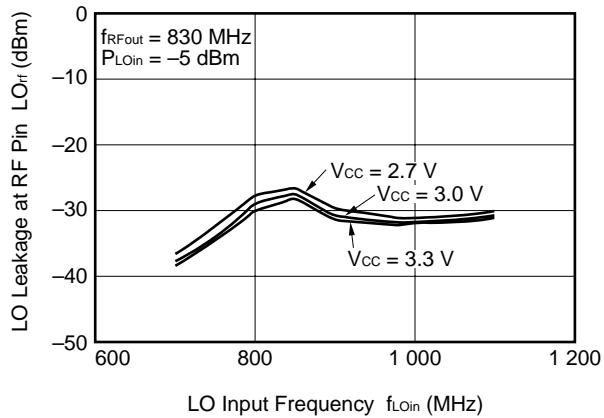
LO LEAKAGE AT IF PIN vs. LO INPUT FREQUENCY



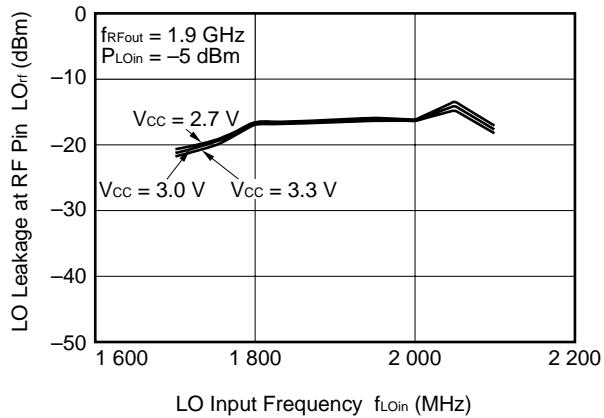
LO LEAKAGE AT IF PIN vs. LO INPUT FREQUENCY



LO LEAKAGE AT RF PIN vs. LO INPUT FREQUENCY



LO LEAKGE AT RF PIN vs. LO INPUT FREQUENCY



Remark The graphs indicate nominal characteristics.

12. S-PARAMETERS

12.1 S-parameters for Matched RF Output ($V_{cc} = V_{RFout} = 3.0$ V) – with test circuits 1 and 2 – (monitored at RF connector on board)

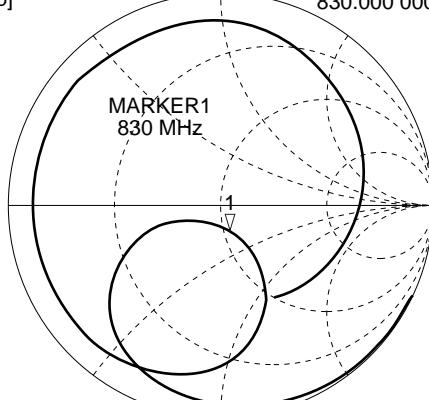
- RF output matched at 830 MHz

CH1 S₁₁ 1 U FS [hp] 1; 53.422 Ω -14.973 Ω 12.807 pF
830.000 000 MHz

PRm

Cor
Del

Hld



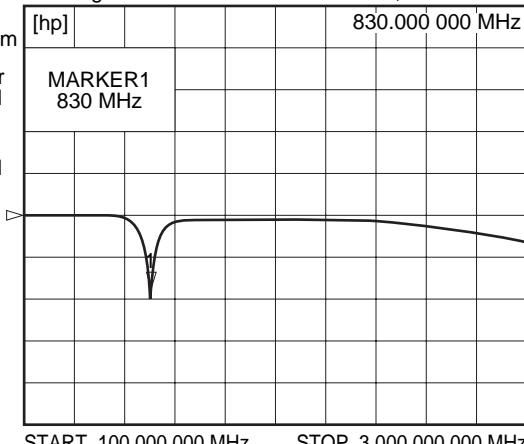
START 100.000 000 MHz STOP 3 000.000 000 MHz

CH1 S₁₁ log MAG 10 dB/ REF 0 dB 1;-17.331 dB

PRm

Cor
Del

Hld



START 100.000 000 MHz STOP 3 000.000 000 MHz

- RF output matched at 1.9 GHz

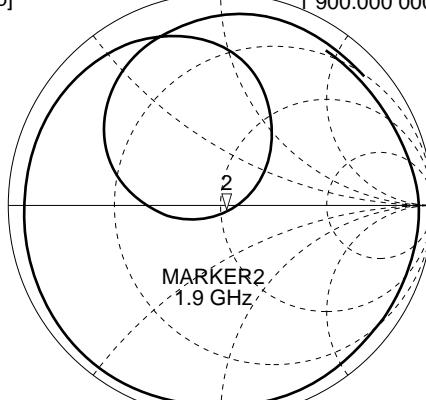
CH1 S₁₁ 1 U FS [hp] 2; 53.846 Ω -3.7441 Ω 22.373 pF
1 900.000 000 MHz

PRm

Cor
Del

Smo

Hld



START 100.000 000 MHz STOP 3 000.000 000 MHz

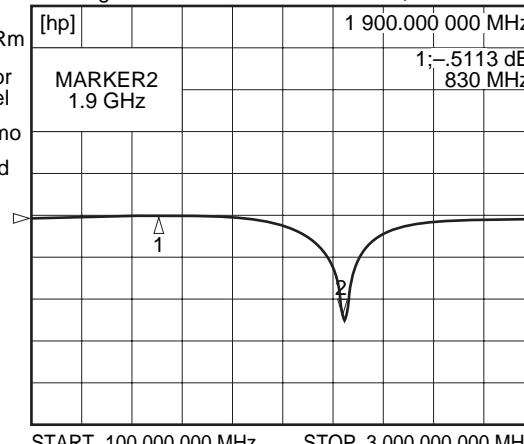
CH1 S₁₁ log MAG 10 dB/ REF 0 dB 2;-24.741 dB

PRm

Cor
Del

Smo

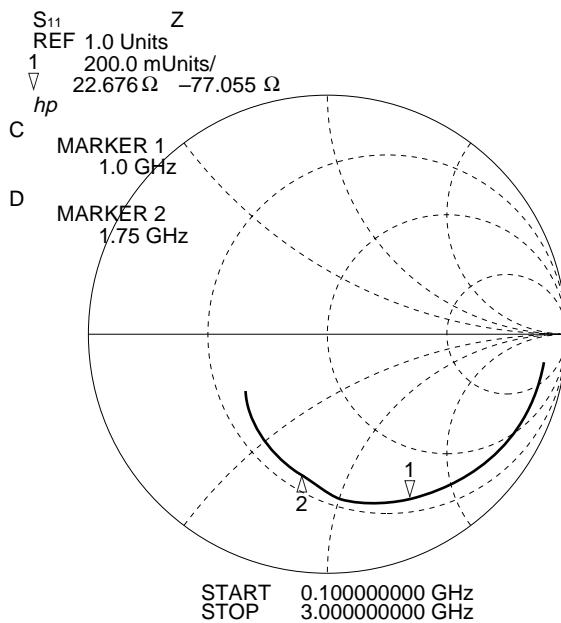
Hld



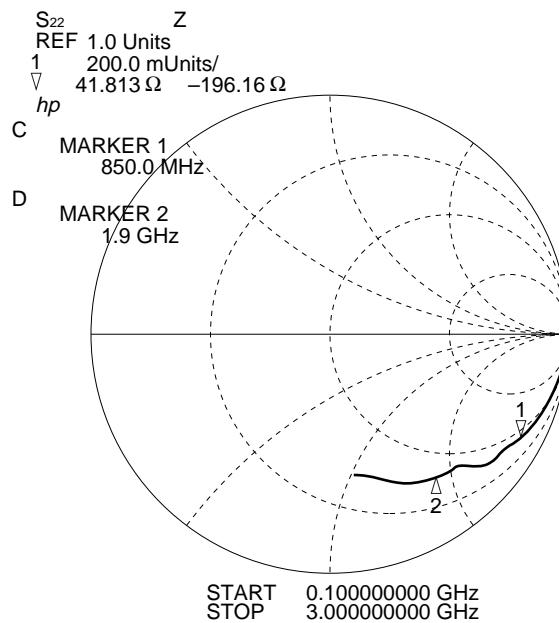
START 100.000 000 MHz STOP 3 000.000 000 MHz

12.2 S-parameters for Each Port ($V_{CC} = V_{RFout} = 3.0$ V)

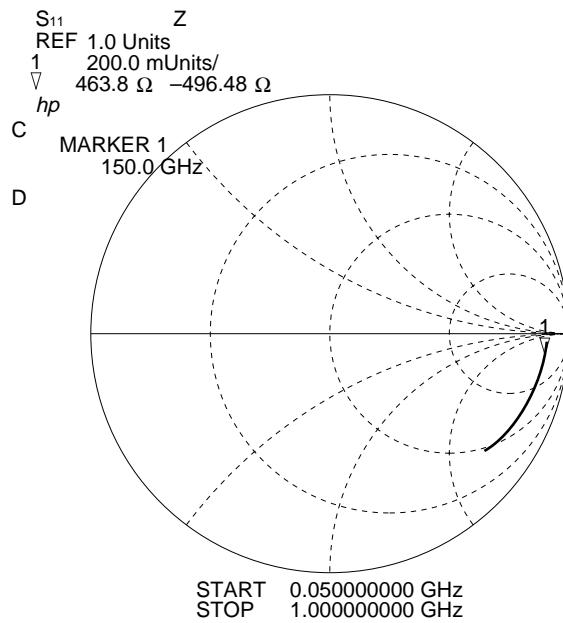
LO port



RF port (no matching)

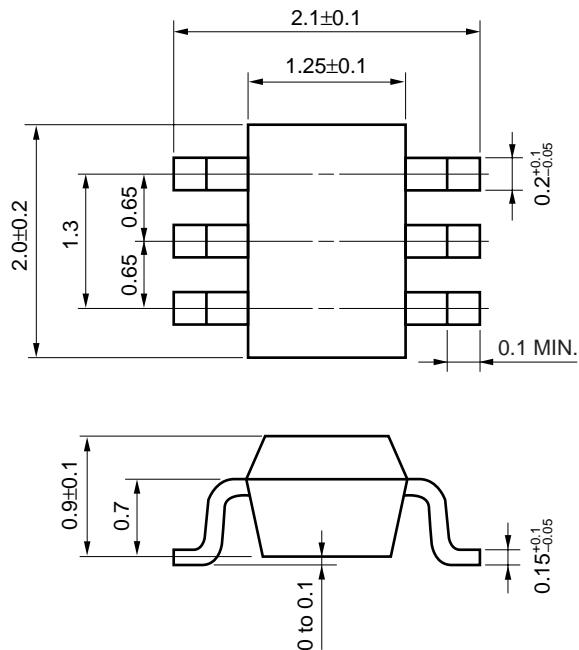


IF port



★ 13. PACKAGE DIMENSIONS

6-PIN SUPER MINIMOLD (UNIT: mm)



14. NOTE ON CORRECT USE

- (1) Observe precautions for handling because of electrostatic sensitive devices.
- (2) Form a ground pattern as widely as possible to minimize ground impedance (to prevent undesired oscillation).
- (3) Keep the track length of the ground pins as short as possible.
- (4) Connect a bypass capacitor (example: 1 000 pF) to the Vcc pin.

15. RECOMMENDED SOLDERING CONDITIONS

This product should be soldered under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared Reflow	Package peak temperature: 235°C or below Time: 30 seconds or less (at 210°C) Count: 3, Exposure limit: None ^{Note}	IR35-00-3
VPS	Package peak temperature: 215°C or below Time: 40 seconds or less (at 200°C) Count: 3, Exposure limit: None ^{Note}	VP15-00-3
Wave Soldering	Soldering bath temperature: 260°C or below Time: 10 seconds or less Count: 1, Exposure limit: None ^{Note}	WS60-00-1
Partial Heating	Pin temperature: 300°C Time: 3 seconds or less (per side of device) Exposure limit: None ^{Note}	—

Note After opening the dry pack, keep it in a place below 25°C and 65% RH for the allowable storage period.

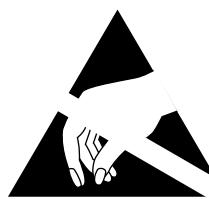
Caution Do not use different soldering methods together (except for partial heating).

For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E).

[MEMO]

[MEMO]

[MEMO]



ATTENTION

OBSERVE PRECAUTIONS
FOR HANDLING
ELECTROSTATIC
SENSITIVE
DEVICES

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