NEC

MOS INTEGRATED CIRCUITS

μPD63315

AC'97 SOUND CODEC

DESCRIPTION

The μPD63315 is an audio codec compliant with the AC'97 Rev 2.1 specification. It features 18-bit ADC's and DAC's (2 channels each) for mutual conversion between audio analog signals with a maximum signal band of 20 kHz and digital signals, and supports full-duplex communication.

The analog signal input block has four analog stereo signal input lines, LINE, CD, VIDEO, and AUX, and three analog monaural signal input lines, PHONE, PC_BEEP, and MIC (2 MIC pins selectable).

The analog signal output block has three outputs pins, LINE_OUT, LNLVL_OUT, and MONO_OUT, each with its own volume control.

The μPD63315 supports also sample rate conversion (SRC), EAPD, power management.

FEATURES

- AC'97 Rev 2.1 compliant
- Oversample ΔΣ-type ADC/DAC (2 channels each)
  - ADC SNR = 85 dB Typ.
  - DAC SNR = 90 dB Typ.
- Multiple codec support
- Sample rate conversion (SRC) support
- Power management support
- External Amplifier Power Down (EAPD) support
- Low-supply-voltage operation: DV_{DD} = 3.3 V, AV_{DD} = 3.3 V
- Operating ambient temperature: –40 to +85°C

APPLICATIONS

- PC sound systems
- PDA

ORDERING INFORMATION

Part Number	Package
μPD63315GA-9EU	48-pin plastic TQFP (fine pitch) (7 × 7)

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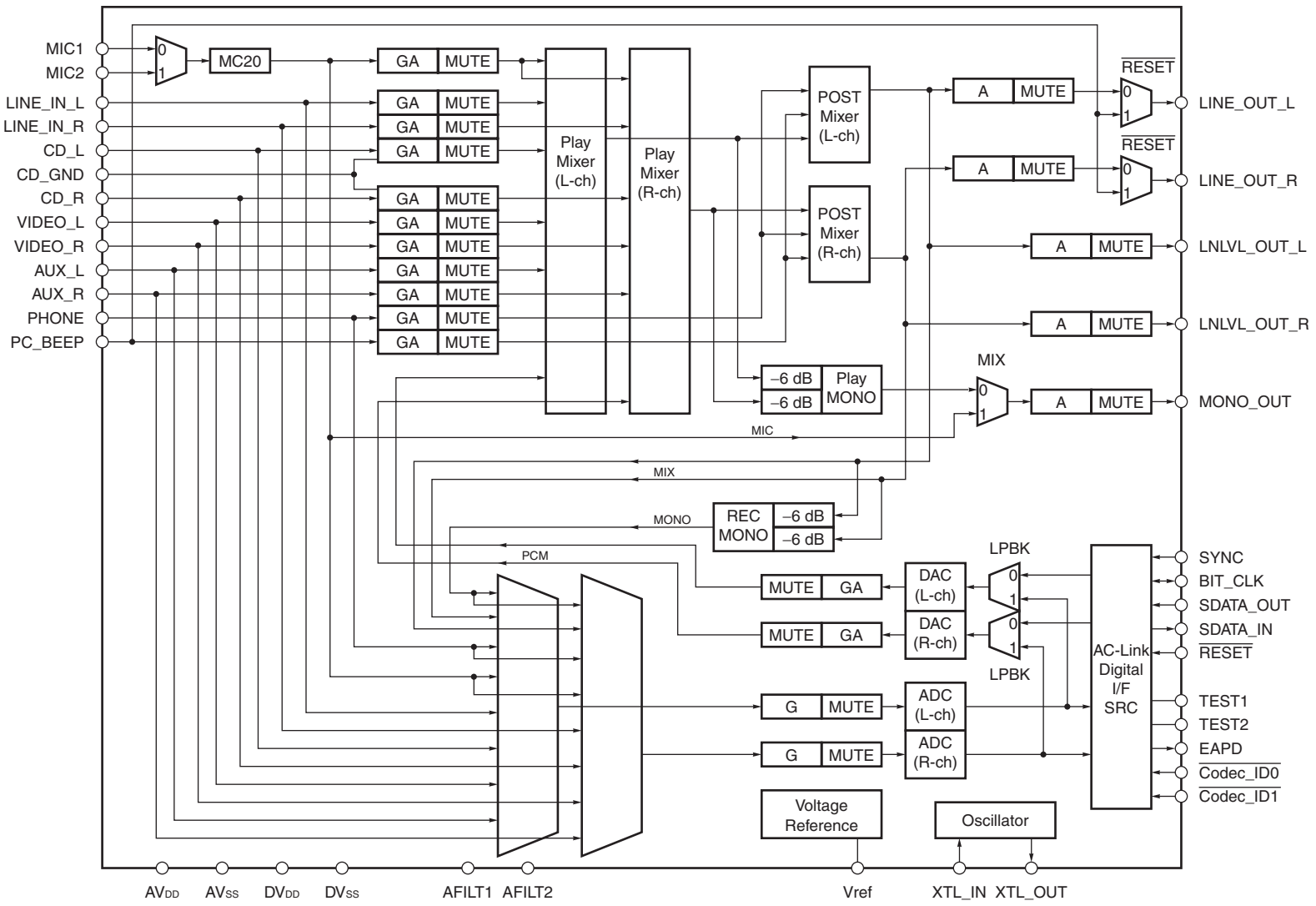
The mark ★ shows major revised points.

BLOCK DIAGRAM

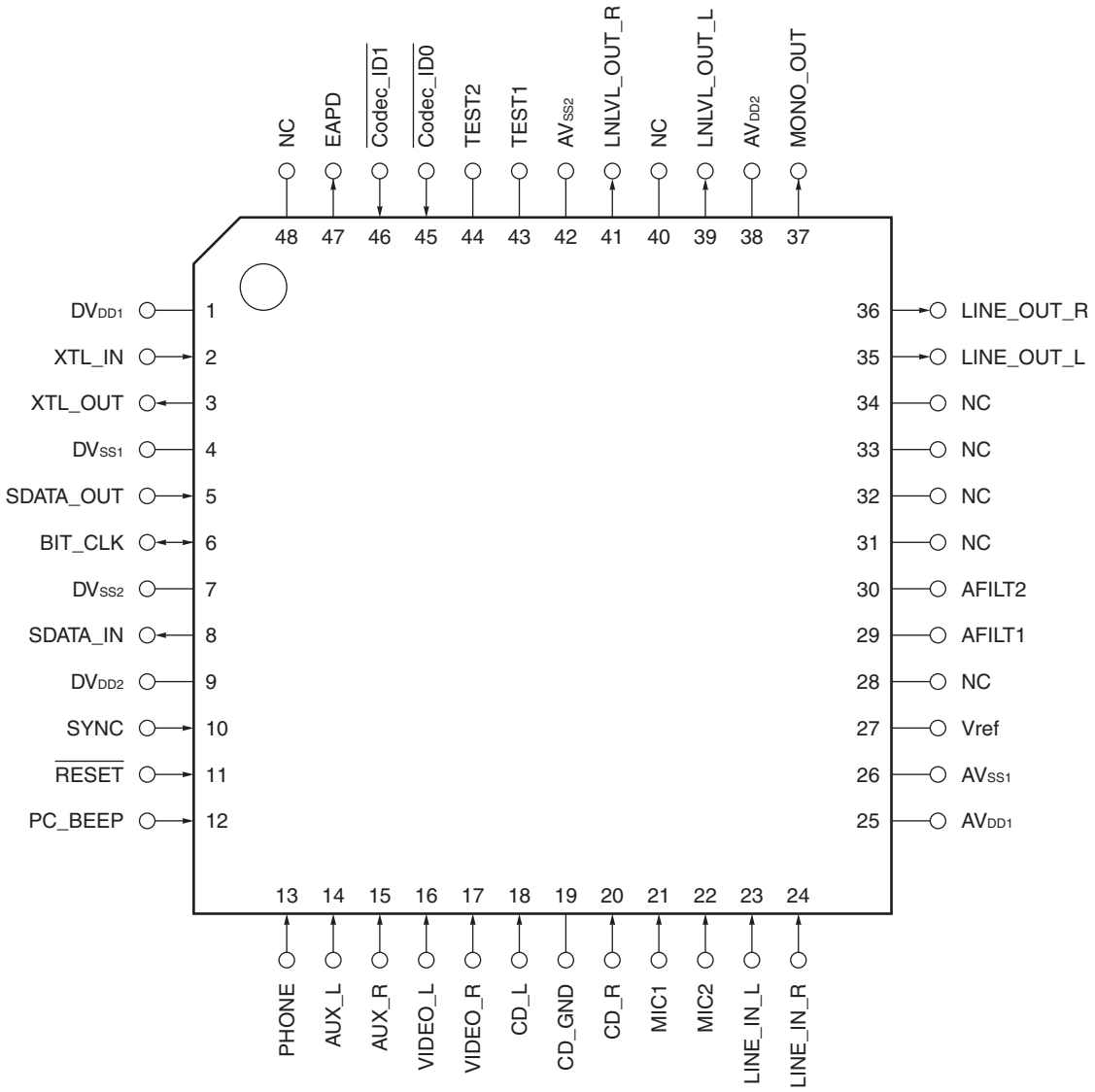


Remark A: Attenuate, G: Gain, GA: Gain or Attenuate

PIN CONFIGURATION (Top View)

48-pin plastic TQFP (fine pitch) (7 × 7)

- μPD633315GA-9EU



PIN FUNCTIONS

(1/2)

Pin No.	Symbol	Input/Output	Function
1	DV_{DD1}	–	Digital power supply
2	XTL_IN	Input	Crystal resonator connection pin/external clock input pin
3	XTL_OUT	Output	Crystal resonator connection pin. When external clock is used, leave this pin open.
4	DV_{SS1}	–	Digital ground
5	SDATA_OUT	Input	AC-link data input
6	BIT_CLK	Input/output	When primary codec: 12.288 MHz serial data clock output When secondary codec: Serial data clock input
7	DV_{SS2}	–	Digital ground
8	SDATA_IN	Output	AC-link data output
9	DV_{DD2}	–	Digital power supply
10	SYNC	Input	48 kHz sample clock input
11	$\overline{\text{RESET}}$	Input	Reset (active low)
12	PC_BEEP	Input	PC Beep monaural input
13	PHONE	Input	PHONE monaural input
14	AUX_L	Input	AUX stereo input, L channel
15	AUX_R	Input	AUX stereo input, R channel
16	VIDEO_L	Input	Video/audio/stereo input, L channel
17	VIDEO_R	Input	Video/audio/stereo input, R channel
18	CD_L	Input	CD stereo input, L channel
19	CD_GND	–	CD stereo input, ground pin
20	CD_R	Input	CD stereo input, R channel
21	MIC1	Input	Microphone input 1
22	MIC2	Input	Microphone input 2
23	LINE_IN_L	Input	Line input, L channel
24	LINE_IN_R	Input	Line input, R channel
25	AV_{DD1}	–	Analog power supply
26	AV_{SS1}	–	Analog ground
27	Vref	–	Reference voltage output for bypass capacitor connection
28	NC	–	Unused pin. Leave this pin open.
29	AFILT1	–	ADC, L channel, anti-alias filter pin
30	AFILT2	–	ADC, R channel, anti-alias filter pin
31	NC	–	Unused pin. Leave this pin open.
32	NC	–	Unused pin. Leave this pin open.
33	NC	–	Unused pin. Leave this pin open.
34	NC	–	Unused pin. Leave this pin open.
35	LINE_OUT_L	Output	Line output, L channel
36	LINE_OUT_R	Output	Line output, R channel
37	MONO_OUT	Output	Monaural output
38	AV_{DD2}	–	Analog power supply

(2/2)

Pin No.	Symbol	Input/Output	Function
39	LNLVL_OUT_L	Output	True line level output, L channel
40	NC	–	Unused pin. Leave this pin open.
41	LNLVL_OUT_R	Output	True line level output, R channel
42	AV_{SS2}	–	Analog ground
43	TEST1	–	IC selection test pin. Leave this pin open.
44	TEST2	–	IC selection test pin. Leave this pin open.
45	$\overline{\text{Codec\_ID0}}$	Input	Codec ID0 setting pin
46	$\overline{\text{Codec\_ID1}}$	Input	Codec ID1 setting pin
47	EAPD	Output	EAPD pin
48	NC	–	Unused pin. Leave this pin open.

CONTENTS

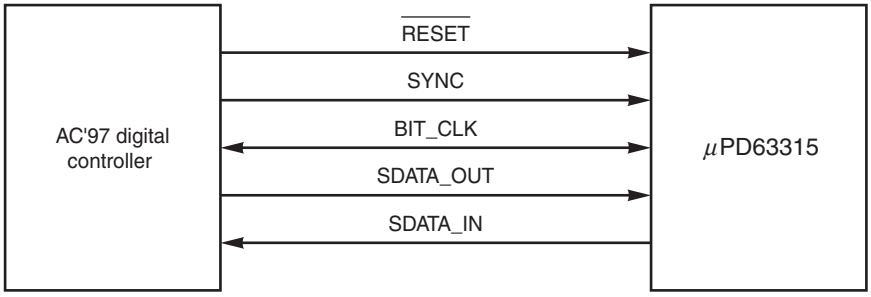
1. FUNCTIONS

1. 1 Connection with AC'97 Digital Controller

The μPD63315 is connected to an external AC'97 digital controller via AC-link (refer to **Figure 1-1**).

For details about the AC-link interface, refer to AC'97 Revision 2.1.

Figure 1-1. AC'97 Digital Controller Connection Example



1. 2 Analog Input Block

The μPD63315 supports four stereo signal inputs (LINE, CD, VIDEO, AUX), two monaural inputs (PHONE, PC_BEEP), and one microphone input (two input pins).

1. 3 Analog Output Block

The μPD63315 supports two stereo outputs (LINE_OUT, LNLVL_OUT), and one monaural output (MON_OUT).

1. 4 Clock

The μPD63315 has an internal clock generator incorporated. The μPD63315 can generate an internal master clock by connecting either a 24.576 MHz crystal resonator or a ceramic resonator to the XTL_IN and XTL_OUT pins.

An external clock can also be input to the oscillator. In this case, directly input the clock signal to the XTL_IN pin, and leave the XTL_OUT pin open.

1. 5 Reset

The μPD63315 supports three reset modes. Cold reset and warm reset are controlled from external pins, and register reset is controlled by writing to a register.

1. 5. 1 Cold reset

A cold reset resets all the internal blocks of the μPD63315, including registers. After a cold reset, registers will be set to their initial values. A cold reset is performed by driving the $\overline{\text{RESET}}$ pin low. Drive the SDATA_OUT and SYNC pins low while the $\overline{\text{RESET}}$ pin is low. Note that analog output pins other than the LINE_OUT_L and LINE_OUT_R pins are in a Hi-Z status during this period and the input from the PC_BEEP pin is directly output from the LINE_OUT_L and LINE_OUT_R pins.

The analog block inside the μPD63315 starts initialization after the $\overline{\text{RESET}}$ pin has risen. For a multiple codec configuration, simultaneously execute a cold reset for all the μPD63315 devices connected to the AC-Link.

1. 5. 2 Warm reset

A warm reset resets the AC-Link interface. It is performed by driving the SYNC signal high for a fixed period of time.

If a warm reset has been executed, bits PR4 and PR5 of the Power Down Control/Status register (26h) are set to 0. Other register values will be retained.

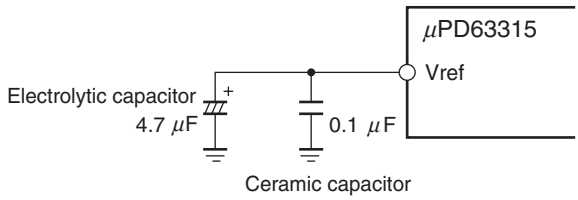
1. 5. 3 Register reset

Returns all the registers except the Power Down register to their default values.

1. 6 Noise Reduction Capacitor Connection Pin

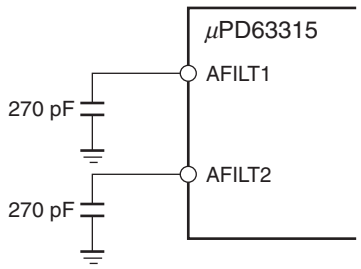
The Vref pin (pin 27) is a reference voltage connection pin for connecting a bypass capacitor. Connect the bypass capacitor for noise reduction as shown in the following figure.

Figure 1-2. Bypass Capacitor Connection Example



The AFILT1 pin (pin 29) and the AFILT2 pin (pin 30) are capacitor connection pins for the ADC anti-alias filter. Connect the capacitor for noise reduction as shown in the following figure.

Figure 1-3. Anti-Alias Filter Capacitor Connection Example



1. 7 Codec ID

The μPD63315 supports codec IDs for multiple codec use. The codec ID is set with the $\overline{\text{Codec\_ID0}}$ pin (pin 45) and the $\overline{\text{Codec\_ID1}}$ pin (pin 46). The $\overline{\text{Codec\_ID0}}$ and $\overline{\text{Codec\_ID1}}$ pins are pulled up internally. As shown in Table 1-1, the codec ID is set to the inverted value of the pin status. In other words, for the Primary codec setting, either leave both the $\overline{\text{Codec\_ID0}}$ pin and the $\overline{\text{Codec\_ID1}}$ pin open, or connect them to V_{DD}. The values of the $\overline{\text{Codec\_ID0}}$ pin and $\overline{\text{Codec\_ID1}}$ pin must be fixed at power application.

Table 1-1. μPD63315 Codec ID Settings

$\overline{\text{Codec\_ID1}}$ (46)	$\overline{\text{Codec\_ID0}}$ (45)	Codec ID	Setting
Leave open or V_{DD}	Leave open or V_{DD}	00	Primary
Leave open or V_{DD}	GND	01	Secondary
GND	Leave open or V_{DD}	10	Secondary
GND	GND	11	Secondary

The AC-link frame configurations for each codec ID setting are shown in Tables 1-2, 1-3, and 1-4. Slot 0 contains tag information that indicates which slots of the current frame are valid and invalid.

Table 1-2. Frame Configuration When Codec ID = 00 (Primary), Codec ID = 01 (Secondary)

Slot No.	Bit Length	SDATA_OUT	SDATA_IN
Slot 0	16	TAG	TAG
Slot 1	20	8-bit Command Address	8-bit Status Address
Slot 2	20	16-bit Command Data	16-bit Status Data
Slot 3	20	18-bit DAC Input Left	18-bit ADC Output Left
Slot 4	20	18-bit DAC Input Right	18-bit ADC Output Right
Slot 5	20	Invalid	Invalid
Slot 6	20	Invalid	Invalid
Slot 7	20	Invalid	Invalid
Slot 8	20	Invalid	Invalid
Slot 9	20	Invalid	Invalid
Slot 10	20	Invalid	Invalid
Slot 11	20	Invalid	Invalid
Slot 12	20	Invalid	Invalid

Table 1-3. Frame Configuration When Codec ID = 10 (Secondary)

Slot No.	Bit Length	SDATA_OUT	SDATA_IN
Slot 0	16	TAG	TAG
Slot 1	20	8-bit Command Address	8-bit Status Address
Slot 2	20	16-bit Command Data	16-bit Status Data
Slot 3	20	Invalid	18-bit ADC Output Left
Slot 4	20	Invalid	18-bit ADC Output Right
Slot 5	20	Invalid	Invalid
Slot 6	20	Invalid	Invalid
Slot 7	20	18-bit DAC Input Left	Invalid
Slot 8	20	18-bit DAC Input Right	Invalid
Slot 9	20	Invalid	Invalid
Slot 10	20	Invalid	Invalid
Slot 11	20	Invalid	Invalid
Slot 12	20	Invalid	Invalid

Table 1-4. Frame Configuration When Codec ID = 11 (Secondary)

Slot No.	Bit Length	SDATA_OUT	SDATA_IN
Slot 0	16	TAG	TAG
Slot 1	20	8-bit Command Address	8-bit Status Address
Slot 2	20	16-bit Command Data	16-bit Status Data
Slot 3	20	Invalid	18-bit ADC Output Left
Slot 4	20	Invalid	18-bit ADC Output Right
Slot 5	20	Invalid	Invalid
Slot 6	20	18-bit DAC Input Left	Invalid
Slot 7	20	Invalid	Invalid
Slot 8	20	Invalid	Invalid
Slot 9	20	18-bit DAC Input Right	Invalid
Slot 10	20	Invalid	Invalid
Slot 11	20	Invalid	Invalid
Slot 12	20	Invalid	Invalid

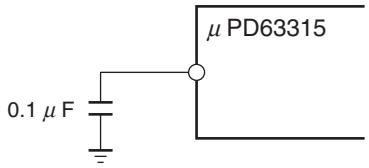
1. 8 Usage Precautions

1. 8. 1 Handling of unused analog input pin

Analog input pins may influence the internal circuit characteristics if register mute is cancelled while they are open.

Therefore, ground all unused analog input pins via a capacitor (refer to **Figure 1-4**) and set related registers to MUTE.

Figure 1-4. Example of Handling of Unused Analog Input Pin



1. 8. 2 Power on

Operation of the μPD63315 is started by driving the input of the $\overline{\text{RESET}}$ pin high after DV_{DD} and AV_{DD} have been applied. Make sure that the master clock is stable before driving the input signal to the $\overline{\text{RESET}}$ pin high.

2. REGISTERS

The register map of the μPD63315 is shown below.

Table 2-1. μPD63315 Register Map

Address	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0150h
02h	Play Master Volume	MVM	x	MVL5	MVL4	MVL3	MVL2	MVL1	MVL0	x	x	MVR5	MVR4	MVR3	MVR2	MVR1	MVR0	8000h
04h	LNLVL Volume	LVM	x	LVL5	LVL4	LVL3	LVL2	LVL1	LVL0	x	x	LVR5	LVR4	LVR3	LVR2	LVR1	LVR0	8000h
06h	Master Mono Volume	MMM	x	x	x	x	x	x	x	x	x	MVN5	MVN4	MVN3	MVN2	MVN1	MVN0	8000h
0Ah	PC_BEEP Volume	MPC	x	x	x	x	x	x	x	x	x	x	PCV3	PCV2	PCV1	PCV0	x	0000h
0Ch	Phone Volume	MPH	x	x	x	x	x	x	x	x	x	x	PHV4	PHV3	PHV2	PHV1	PHV0	8008h
0Eh	MIC Volume	MMC	x	x	x	x	x	x	x	x	MC20	x	MCV4	MCV3	MCV2	MCV1	MCV0	8008h
10h	Line Volume	MLV	x	x	LLV4	LLV3	LLV2	LLV1	LLV0	x	x	x	RLV4	RLV3	RLV2	RLV1	RLV0	8808h
12h	CD Volume	MCD	x	x	LCV4	LCV3	LCV2	LCV1	LCV0	x	x	x	RCV4	RCV3	RCV2	RCV1	RCV0	8808h
14h	Video Volume	MVV	x	x	LVV4	LVV3	LVV2	LVV1	LVV0	x	x	x	RVV4	RVV3	RVV2	RVV1	RVV0	8808h
16h	Aux Volume	MAV	x	x	LAV4	LAV3	LAV2	LAV1	LAV0	x	x	x	RAV4	RAV3	RAV2	RAV1	RAV0	8808h
18h	PCM Out Volume	MPO	x	x	LPO4	LPO3	LPO2	LPO1	LPO0	x	x	x	RPO4	RPO3	RPO2	RPO1	RPO0	8808h
1Ah	Record Select	x	x	x	x	x	SL2	SL1	SL0	x	x	x	x	x	SR2	SR1	SR0	0000h
1Ch	Record Gain	MRG	x	x	x	LRG3	LRG2	LRG1	LRG0	x	x	x	x	RRG3	RRG2	RRG1	RRG0	8000h
20h	General Purpose	0	x	x	x	x	x	MIX	MS	LPBK	x	x	x	x	x	x	x	0000h
26h	Power Down Control/Status	EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0	x	x	x	x	REF	ANL	DAC	ADC	000xh
28h	Extended Audio ID	ID1	ID0	x	x	x	x	AMAP	x	x	x	x	x	x	x	x	1	x201h
2Ah	Extended Audio Control/Status	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	VRA	0000h
2Ch	PCM DAC Rate	PDR15	PDR14	PDR13	PDR12	PDR11	PDR10	PDR9	PDR8	PDR7	PDR6	PDR5	PDR4	PDR3	PDR2	PDR1	PDR0	BB80h
32h	PCM ADC Rate	PAR15	PAR14	PAR13	PAR12	PAR11	PAR10	PAR9	PAR8	PAR7	PAR6	PAR5	PAR4	PAR3	PAR2	PAR1	PAR0	BB80h
7Ch	Vendor ID 1	0	1	0	0	1	1	1	0	0	1	0	0	0	1	0	1	4E45h
7Eh	Vendor ID 2	0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	1	4301h

Caution Read and write access to registers that are not indicated in the above table, in other words registers that do not exist, is prohibited.

2. 1 Description of Registers

2. 1. 1 Reset register (00h)

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0150h

When this register is written to, all the registers except the Power Down Control/Status register (26h) are returned to their default value. This register returns the default value when it is read.

2. 1. 2 Play Master Volume register (02h)

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
02h	MVM	x	MVL5	MVL4	MVL3	MVL2	MVL1	MVL0	x	x	MVR5	MVR4	MVR3	MVR2	MVR1	MVR0	8000h

This register is used to set the master volume for LINE_OUT_L and LINE_OUT_R. The relationships between the bits and gain are shown in Table 2-2 below. The master volume can be set in 1.5 dB steps, in the range of 0 dB to −46.5 dB. Mute is set simultaneously for the left and right channels.

The default value is 8000h (gain: 0 dB, mute: ON).

- MVM: Play Master Volume L channel/Play Master Volume R channel mute control bit
- MVL[5:0]: Play Master Volume L channel gain control bit
- MVR[5:0]: Play Master Volume R channel gain control bit

When “1xxxxx” is written to MVL[5:0]/MVR[5:0], this gets written as “011111” to the internal register, and the gain setting becomes −46.5 dB. Thereafter, “011111” is returned when the value of this register is read.

Table 2-2. Relationship Between Bit and Gain for Play Master Volume Register (02h)

MVM	MVL [5:0]/MVR [5:0]	Gain
0	00 0000	0 dB
0	00 0001	−1.5 dB
⋮	⋮	⋮
0	00 1110	−45.0 dB
0	00 1111	−46.5 dB
0	1x xxxx	−46.5 dB
1	xx xxxx	Mute
1	00 0000	Default setting

2. 1. 3 LNLVL Volume register (04h)

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
04h	LVM	x	LVL5	LVL4	LVL3	LVL2	LVL1	LVL0	x	x	LVR5	LVR4	LVR3	LVR2	LVR1	LVR0	8000h

This register is used to set the LNLVL (True Line Level Out) output volume. The relationships between the bits and gain are shown in Table 2-3 below. The volume can be set in 1.5 dB steps, in the range of 0 dB to –46.5 dB. Mute is set simultaneously for the left and right channels.

The default value is 8000h (gain: 0 dB, mute: ON).

- LVM: LNLVL Volume L channel/LNLVL Volume R channel mute control bit
- LVL[5:0]: LNLVL Volume L channel gain control bit
- LVR[5:0]: LNLVL Volume R channel gain control bit

When “1xxxxx” is written to LVL[5:0]/LVR[5:0], this gets written as “011111” to the internal register, and the gain setting becomes –46.5 dB. Thereafter, “011111” is returned when the value of this register is read.

Table 2-3. Relationship Between Bit and Gain Setting for LNLVL Volume Register (04h)

LVM	LVL [5:0]/LVR [5:0]	Gain
0	00 0000	0 dB
0	00 0001	–1.5 dB
⋮	⋮	⋮
0	00 1110	–45.0 dB
0	00 1111	–46.5 dB
0	1x xxxx	–46.5 dB
1	xx xxxx	Mute
1	00 0000	Default setting

2. 1. 4 Master Mono Volume register (06h)

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
06h	MMM	x	x	x	x	x	x	x	x	x	MVN5	MVN4	MVN3	MVN2	MVN1	MVN0	8000h

This register is used to set the MONO_OUT output master volume. The relationships between the bits and gain are shown in Table 2-4 below. The master volume can be set in 1.5 dB steps, in the range of 0 dB to –46.5 dB. Mute is set simultaneously for the left and right channels.

The default value is 8000h (gain: 0 dB, mute: ON).

- MMM: Monaural (Mono) Master Volume mute control bit
- MVN[5:0]: Monaural (Mono) Master Volume gain control bit

When “1xxxxx” is written to MVN[5:0], this gets written as “011111” to the internal register, and the gain setting becomes –46.5 dB. Thereafter, “011111” is returned when the value of this register is read.

Table 2-4. Relationship Between Bit and Gain Setting for Master Mono Volume Register (06h)

MMM	MVN [5:0]	Gain
0	00 0000	0 dB
0	00 0001	–1.5 dB
⋮	⋮	⋮
0	00 1110	–45.0 dB
0	00 1111	–46.5 dB
0	1x xxxx	–46.5 dB
1	xx xxxx	Mute
1	00 0000	Default setting

2. 1. 5 PC Beep Volume register (0Ah)

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0Ah	MPC	x	x	x	x	x	x	x	x	x	x	PCV3	PCV2	PCV1	PCV0	x	0000h

This register is used to set the PC_BEEP mixer input volume. The relationships between the bits and gain are shown in Table 2-5 below. The volume can be set in 3.0 dB steps, in the range of 0 dB to –45 dB.

The default value is 0000h (gain: 0 dB, mute: OFF).

- MPC: PC_BEEP mute control bit
- PCV[3:0]: PC_BEEP gain control bit

The PC_BEEP input is directly connected to the LINE_OUT_L and LINE_OUT_R outputs while the reset signal is low level. This function serves to acknowledge warning beeps such as that emitted during the POST (power on self test) immediately after the PC is powered up even when this LSI does not operate.

Table 2-5. Relationship Between Bit and Gain Setting for PC Beep Volume Register (0Ah)

MPC	PCV [3:0]	Gain
0	0000	0 dB
0	0001	–3.0 dB
⋮	⋮	⋮
0	1110	–42.0 dB
0	1111	–45.0 dB
1	xxxx	Mute
0	0000	Default setting

2. 1. 6 Phone Volume register (0Ch)

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0Ch	MPH	x	x	x	x	x	x	x	x	x	x	PHV4	PHV3	PHV2	PHV1	PHV0	8008h

This register is used to set the PHONE mixer input volume. The relationships between the bits and gain are shown in Table 2-6 below. The volume can be set in 1.5 dB steps, in the range of +12.0 dB to −34.5 dB.

The default value is 8008h (gain: 0 dB, mute: OFF).

- MPH: PHONE mute control bit
- PHV[4:0]: PHONE gain control bit

Table 2-6. Relationship Between Bit and Gain for Phone Volume Register (0Ch)

MPH	PHV [4:0]	Gain
0	0 0000	+12.0 dB
0	0 0001	+10.5 dB
⋮	⋮	⋮
0	0 1000	0 dB
⋮	⋮	⋮
0	1 1110	−33.0 dB
0	1 1111	−34.5 dB
1	x xxxx	Mute
1	0 1000	Default setting

2. 1. 7 MIC Volume register (0Eh)

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0Eh	MMC	x	x	x	x	x	x	x	x	MC20	x	MCV4	MCV3	MCV2	MCV1	MCV0	8008h

This register is used to set the timer mixer input volume and 20 dB gain. The relationships between the bits and gain are shown in Table 2-8 below. The volume can be set in 1.5 dB steps, in the range of +12.0 dB to –34.5 dB.

The default value is 8008h (gain: 0 dB, mute: ON).

- MMC: MIC mute control bit
- MC20: MIC 20 dB gain ON/OFF setting
- MCV[4:0]: MIC gain control bit

Table 2-7. Gain Settings for MC20 Bit

MC20	Gain Setting
0	20 dB gain OFF (0 dB)
1	20 dB gain ON (20 dB)

Table 2-8. Relationship Between Bit and Gain for MIC Volume Register (0Eh)

MMC	MCV [4:0]	Gain
0	0 0000	+12.0 dB
0	0 0001	+10.5 dB
⋮	⋮	⋮
0	0 1000	0 dB
⋮	⋮	⋮
0	1 1110	–33.0 dB
0	1 1111	–34.5 dB
1	x xxxx	Mute
1	0 1000	Default setting

2. 1. 8 LINE Volume register (10h)

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
10h	MLV	x	x	LLV4	LLV3	LLV2	LLV1	LLV0	x	x	x	RLV4	RLV3	RLV2	RLV1	RLV0	8808h

This register is used to set the LINE_L and LINE_R mixer input volume. The relationships between the bits and gain are shown in Table 2-9 below. The volume can be set in 1.5 dB steps, in the range of +12.0 dB to −34.5 dB.

The default value is 8808h (gain: 0 dB, mute: ON).

- MLV: Line Volume mute control bit
- LLV[4:0]: Line Volume L channel gain control bit
- RLV[4:0]: Line Volume R channel gain control bit

Table 2-9. Relationship Between Bit and Gain for LINE Volume Register (10h)

MLV	LLV [4:0]/RLV [4:0]	Gain
0	0 0000	+12.0 dB
0	0 0001	+10.5 dB
⋮	⋮	⋮
0	0 1000	0 dB
⋮	⋮	⋮
0	1 1110	−33.0 dB
0	1 1111	−34.5 dB
1	x xxxx	Mute
1	0 1000	Default setting

2. 1. 9 CD Volume register (12h)

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
12h	MCD	x	x	LCV4	LCV3	LCV2	LCV1	LCV0	x	x	x	RCV4	RCV3	RCV2	RCV1	RCV0	8808h

This register is used to set the CD_L and CD_R mixer input volume. The relationships between the bits and gain are shown in Figure 2-10 below. The volume can be set in 1.5 dB steps, in the range of +12.0 dB to −34.5 dB.

The default value is 8808h (gain: 0 dB, mute: ON).

- MCD: CD Volume mute control bit
- LCV[4:0]: CD Volume L channel gain control bit
- RCV[4:0]: CD Volume R channel gain control bit

Table 2-10. Relationship Between Bit and Gain for CD Volume Register (12h)

MCD	LCV [4:0]/RCV [4:0]	Gain
0	0 0000	+12.0 dB
0	0 0001	+10.5 dB
⋮	⋮	⋮
0	0 1000	0 dB
⋮	⋮	⋮
0	1 1110	−33.0 dB
0	1 1111	−34.5 dB
1	x xxxx	Mute
1	0 1000	Default setting

2. 1. 10 Video Volume register (14h)

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
14h	MVV	x	x	LVV4	LVV3	LVV2	LVV1	LVV0	x	x	x	RVV4	RVV3	RVV2	RVV1	RVV0	8808h

This register is used to set the VIDEO_L and VIDEO/R mixer input volume. The relationships between the bits and gain are shown in Table 2-11 below. The volume can be set in 1.5 dB steps, in the range of +12.0 dB to –34.5 dB.

The default value is 8808h (gain: 0 dB, mute: ON).

- MVV: Video Volume mute control bit
- LVV[4:0]: Video Volume L channel gain control bit
- RVV[4:0]: Video Volume R channel gain control bit

Table 2-11. Relationship Between Bit and Gain for Video Volume Register (14h)

MVV	LVV [4:0]/RVV [4:0]	Gain
0	0 0000	+12.0 dB
0	0 0001	+10.5 dB
⋮	⋮	⋮
0	0 1000	0 dB
⋮	⋮	⋮
0	1 1110	–33.0 dB
0	1 1111	–34.5 dB
1	x xxxx	Mute
1	0 1000	Default setting

2. 1. 11 Aux Volume register (16h)

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
16h	MAV	x	x	LAV4	LAV3	LAV2	LAV1	LAV0	x	x	x	RAV4	RAV3	RAV2	RAV1	RAV0	8808h

This register is used to set the AUX_L and AUX_R mixer input volume. The relationships between the bits and gain are shown in Table 2-12 below. The volume can be set in 1.5 dB steps, in the range of +12.0 dB to –34.5 dB. Mute is set simultaneously for the left and right channels.

The default value is 8808h (gain: 0 dB, mute: ON).

- MAV: Aux Volume mute control bit
- LAV[4:0]: Aux Volume L channel gain control bit
- RAV[4:0]: Aux Volume R channel gain control bit

Table 2-12. Relationship Between Bit and Gain for Aux Volume Register (16h)

MAV	LAV [4:0]/RAV [4:0]	Gain
0	0 0000	+12.0 dB
0	0 0001	+10.5 dB
⋮	⋮	⋮
0	0 1000	0 dB
⋮	⋮	⋮
0	1 1110	–33.0 dB
0	1 1111	–34.5 dB
1	x xxxx	Mute
1	0 1000	Default setting

2. 1. 12 PCM Out Volume register (18h)

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
18h	MPO	x	x	LPO4	LPO3	LPO2	LPO1	LPO0	x	x	x	RPO4	RPO3	RPO2	RPO1	RPO0	8808h

This register is used to set the PCM Out output volume. The relationships between the bits and gain are shown in Table 2-13 below. The volume can be set in 1.5 dB steps, in the range of +12.0 dB to −34.5 dB.

The default value is 8808h (gain: 0 dB, mute: ON).

- MPO: PCM Out Volume mute control bit
- LPO[4:0]: PCM Out Volume L channel gain control bit
- RPO[4:0]: PCM Out Volume R channel gain control bit

Table 2-13. Relationship Between Bit and Gain for PCM Out Volume Register (18h)

MPO	LPO [4:0]/RPO [4:0]	Gain
0	0 0000	+12.0 dB
0	0 0001	+10.5 dB
⋮	⋮	⋮
0	0 1000	0 dB
⋮	⋮	⋮
0	1 1110	−33.0 dB
0	1 1111	−34.5 dB
1	x xxxx	Mute
1	0 1000	Default setting

2. 1. 13 Record Select register (1Ah)

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
1Ah	x	x	x	x	x	SL2	SL1	SL0	x	x	x	x	x	SR2	SR1	SR0	0000h

This register is used to select the signal input to ADC. The relationships between the bits and ADC input are shown in Table 2-14 below.

The default value is 0000h (MIC input to both L channel and R channel).

- SL[2:0]: L channel input selection
- SR[2:0]: R channel input selection

Table 2-14. Relationship Between Bit and ADC Input for Record Select Register (1Ah)

SL [2:0]	Left Channel Record Source	SR [2:0]	Right Channel Record Source
000	MIC (default value)	000	MIC (default value)
001	CD_L	001	CD_R
010	VIDEO_L	010	VIDEO_R
011	AUX_L	011	AUX_R
100	LINE_IN_L	100	LINE_IN_R
101	Stereo Mix (L-ch)	101	Stereo Mix (R-ch)
110	Mono Mix	110	Mono Mix
111	PHONE	111	PHONE

In the case of Stereo Mix, mixer output is input to ADC.

In the case of Mono Mix, the mixer output gain is attenuated by −6 dB, and the resulting signal is input to the left and right channels.

2. 1. 14 Record Gain register (1Ch)

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
1Ch	MRG	x	x	x	LRG3	LRG2	LRG1	LRG0	x	x	x	x	RRG3	RRG2	RRG1	RRG0	8000h

This register is used to set the record gain. The relationships between the bits and gain are shown in Table 2-15 below. The volume can be set in 1.5 dB steps, in the range of +22.5 dB to 0.0 dB.

The default value is 8000h (gain: 0 dB, mute: ON).

- MRG: Record Gain mute control bit
- LRG[3:0]: Record Gain L channel control bit
- RRG[3:0]: Record Gain R channel control bit

Table 2-15. Relationship Between Bit and Gain for Record Gain Register (1Ch)

MRG	LRG [3:0]/RRG [3:0]	Gain
0	0000	0 dB
0	0001	+1.5 dB
⋮	⋮	⋮
0	1110	+21.0 dB
0	1111	+22.5 dB
1	xxxx	Mute
1	0000	Default setting

2. 1. 15 General Purpose register (20h)

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
20h	0	x	x	x	x	x	MIX	MS	LPBK	x	x	x	x	x	x	x	0000h

This register is used to set the internal signal path. The relationships between the bits and path are shown in Table 2-16 below. For the connection of each path, refer to the block diagram.

The default value is 0000h (Mono Out: Mixer, MIC Select: MIC1, Loopback: OFF).

Table 2-16. Relationship Between Bit and Path for General Purpose Register (20h)

Bit	Function	Path	
MIX	Mono Output Select	0	Mixer
		1	MIC
MS	MIC Select	0	MIC1
		1	MIC2
LPBK	ADC/DAC Digital Loopback	0	OFF
		1	ON

2. 1. 16 Power Down Control/Status register (26h)

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
26h	EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0	x	x	x	x	REF	ANL	DAC	ADC	000xh

This register indicates the control/operation status of the power down mode of the μPD63315. The higher 8 bits (D[15:8]) are a write-only register used to control the power down mode. The lower 8 bits (D[7:0]) are a read-only register that indicates the operating status of the analog blocks.

Table 2-17. Relationship Between Power Down Status Bits (Lower 8 Bits of Register 26h) and Operation Status

Bit	Internal Block	Operation Status	
REF	Reference voltage circuit	0	Not ready
		1	Ready
ANL	Analog Mixer	0	Not ready
		1	Ready
DAC	DAC	0	Not ready
		1	Ready
ADC	ADC	0	Not ready
		1	Ready

Table 2-18. Description of Power Down Control Bits (Higher 8 Bits of Register 26h)

Bit	Function
EAPD	External amplifier power down
PR6	True line level output power amp
PR5	Internal clock stop
PR4	Digital interface (AC-Link) power down
PR3	Analog mixer power down (Vref: OFF)
PR2	Analog mixer power down (Vref: ON)
PR1	DAC power down
PR0	ADC, input multiplexer power down

Table 2-19. Relationship Between Power Down Control Bit (Higher 8 Bits of Register 26h) and Internal Block Status

Bit	ADC, Record Gain	DAC, DAC Volume	Play Mixer, Mono Mixer	Mixer Volume	Master Volume	Mono Master Volume	LNLVL Master Volume	Vref	AC-Link	Clock	External Amp.
PR0 = "1"	PD	x	x	x	x	x	x	x	x	x	x
PR1 = "1"	x	PD	x	x	x	x	x	x	x	x	x
PR2 = "1"	x	x	PD	PD	PD	x	x	x	x	x	x
PR3 = "1"	PD	PD	PD	PD	PD	PD	PD	PD	x	x	x
PR4 = "1"	PD	PD	x	x	x	x	x	x	PD	x	x
PR5 = "1"	PD	PD	x	x	x	x	x	x	PD	PD	x
PR6 = "1"	x	x	x	x	x	x	PD	x	x	x	x
EAPD = "1"	x	x	x	x	x	x	x	x	x	x	PD (EAPD = "H")

Caution When using a multiple codec configuration, the PR4 and PR5 bits of the μPD63315 operating as the primary codec also influence the PR4 and PR5 bits of the secondary codec.
In other words, when the PR4 and PR5 bits of the primary codec are written, the write values also get written simultaneously to the PR4 and PR5 bits of the secondary codec. However, when the PR4 and PR5 bits of the secondary codec are written, the write values do not get written to the PR4 and PR5 bits of the primary codec.

Remark x: No change, PD: Power down

2. 1. 17 Extended Audio ID register (28h)

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
28h	ID1	ID0	x	x	x	x	AMAP	x	x	x	x	x	x	x	x	1	x201h

This register indicates the codec IDs used when the μPD63315 is used in a multiple codec configuration, and also whether or not the sample rate conversion function is supported.

ID1 and ID0 hold values set by the $\overline{\text{Codec\_ID1}}$ pin (pin 46) and the $\overline{\text{Codec\_ID0}}$ pin (pin 45).

Since the μPD63315 supports the sample rate conversion function, bit D0 always returns 1.

Table 2-20. μPD63315 Codec ID Settings

$\overline{\text{Codec\_ID1}}$ (46)		$\overline{\text{Codec\_ID0}}$ (45)		Setting
Pin Connection	ID1	Pin Connection	ID0	
Leave open or V_{DD}	0	Leave open or V_{DD}	0	Primary
Leave open or V_{DD}	0	GND	1	Secondary
GND	1	Leave open or V_{DD}	0	Secondary
GND	1	GND	1	Secondary

2. 1. 18 Extended Audio Control/Status register (2Ah)

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
2Ah	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	VRA	0000h

This register is used to control the sample rate of the μPD63315. The PCM DAC Rate register (2Ch) and the PCM ADC Rate register (32h) are enabled by writing 1 to the VRA bit. When VRA bit is set to 0, PCM DAC Rate register and PCM ADC Rate register values are set to default (BB80h).

The default value is 0000h (VRA disabled = sample rate of 48 kHz for both ADC and DAC).

Table 2-21. VRA Bit Settings

VRA	PCM DAC Rate Register (2Ch)	PCM ADC Rate Register (32h)	Sample Rate
1	Enabled		44.1 kHz or 48 kHz
0	Disabled		48 kHz

2. 1. 19 PCM DAC Rate register (2Ch)

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
2Ch	PDR15	PDR14	PDR13	PDR12	PDR11	PDR10	PDR9	PDR8	PDR7	PDR6	PDR5	PDR4	PDR3	PDR2	PDR1	PDR0	BB80h

This register is used to set the sample rate of the DAC. The DAC sample rate is changed by the value set to this register only when the VRA bit of the Extended Audio Control/Status register (2Ah) is set to 1.

The μPD63315 supports two sample rates, 44.1 kHz and 48 kHz. If a value other than these two rates is written, the DAC sample rate is set to either 44.1 kHz or 48 kHz depending on that value (refer to **Table 2-22**).

The default value is BB80h (48 kHz).

Table 2-22. Relationship Between PCM DAC Rate Register (2Ch) Setting and DAC Sample Rate

Write Data	PDR [15:0] Setting	DAC Sample Rate
0000h to AFFFh	AC44h	44.1 kHz
B000h to FFFFh	BB80h	48 kHz

2. 1. 20 PCM ADC Rate register (32h)

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
32h	PAR15	PAR14	PAR13	PAR12	PAR11	PAR10	PAR9	PAR8	PAR7	PAR6	PAR5	PAR4	PAR3	PAR2	PAR1	PAR0	BB80h

This register is used to set the sample rate of the ADC. The ADC sample rate is changed by the value set to this register only when the VRA bit of the Extended Audio Control/Status register (2Ah) is set to 1.

The μPD63315 supports two sample rates, 44.1 kHz and 48 kHz. If a value other than these two rates is written, the ADC sample rate is set to either 44.1 kHz or 48 kHz depending on that value (refer to **Table 2-23**).

Table 2-23. Relationship Between PCM ADC Rate Register (32h) Setting and ADC Sample Rate

Write Data	PAR [15:0] Setting	ADC Sample Rate
0000h to AFFFh	AC44h	44.1 kHz
B000h to FFFFh	BB80h	48 kHz

2. 1. 21 Vendor ID register (7Ch, 7Eh)

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
7Ch	0	1	0	0	1	1	1	0	0	1	0	0	0	1	0	1	4E45h
7Eh	0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	1	4301h

This read-only register indicates the vendor information and product information of the μPD63315.

Table 2-24. Vendor ID Register (7Ch, 7Eh) Settings

Address	D [15:8]	D [7:0]
7Ch	4Eh = “N”	45h = “E”
7Eh	43h = “C”	01h = “Rev. 1.0”

3. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Digital block power supply voltage	DV_{DD}		−0.3 to +4.6	V
Analog block power supply voltage	AV_{DD}		−0.3 to +4.6	V
Input current	I_I	Pins except power supply and ground	−10 to +10	mA
Digital input voltage	DV_I	All digital input pins	−0.3 to DV_{DD} +0.3	V
Analog input voltage	AV_I	All analog input pins	−0.3 to AV_{DD} +0.3	V
Operating ambient temperature	T_A	Device ambient temperature	−40 to +85	°C
Storage temperature	T_{stg}		−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operation Range (DV_{SS} = AV_{SS} = 0 V, load capacitance = 20 pF)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Digital block power supply voltage	DV_{DD}		3.0	3.3	3.6	V
Analog block power supply voltage	AV_{DD}		3.0	3.3	3.6	V
Operating ambient temperature	T_A	Device ambient temperature	−40	+25	+85	°C
Master clock frequency	f_{MCLK}		−	24.576	−	MHz
Master clock duty factor Note	f_{DTY}		45	50	55	%
★ Digital input voltage (high level)	V_{IH}		1.95	−	−	V
★ Digital input voltage (low level)	V_{IL}		−	−	1.26	V
Analog input signal voltage	V_I		−	0.7	−	$V_{r.m.s.}$
Analog output pin load resistance	R_L	Analog output pin	10	−	−	kΩ

Note Using a master clock duty factor that is outside the recommended operation range may result in degradation of analog characteristics.

DC Characteristics (DV_{DD} = AV_{DD} = 3.3 V, DV_{SS} = AV_{SS} = 0 V, T_A = –40 to +85°C)

(1) Digital Block

	Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
★	Digital block current consumption	I_{DV1}	During normal operation	–	10.0	15.0	mA
★	Digital standby current	I_{DV2}	During power down mode	–	0.0	0.1	mA
	Input leakage current	I_{LI}		–10.0	–	+10.0	μA
	Output leakage current	I_{LO}	During high impedance mode	–10.0	–	+10.0	μA
★	Input voltage, high	V_{IH}		1.95	–	–	V
★	Input voltage, low	V_{IL}		–	–	1.26	V
★	Output voltage, high	V_{OH}	Output current = –5.0 mA	2.70	–	–	V
★	Output voltage, low	V_{OL}	Output current = 5.0 mA	–	–	0.36	V
	Pull-up resistance	R_{UP}		20	50	100	kΩ

(2) Analog Block

	Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
★	Analog block current consumption	I_{AV1}	During normal operation	–	40.0	50.0	mA
★	Analog standby current	I_{AV2}	During power down mode	–	0.0	0.1	mA
	Reference voltage	V_{REF}		1.35	1.4	1.45	V
	Analog input voltage	V_{AI}	Except for MIC input	–	0.7	–	$V_{r.m.s.}$
		V_{MI0}	+20 dB = ON	–	0.07	–	$V_{r.m.s.}$
		V_{MI20}	+20 dB = OFF	–	0.7	–	$V_{r.m.s.}$
	Analog output voltage	V_{AO}		–	0.7	–	$V_{r.m.s.}$
	Input impedance	R_{IN}	Analog output pin	10	–	–	kΩ

Transmission Characteristics

(unless otherwise specified, DV_{DD} = AV_{DD} = 3.3 V, DV_{SS} = AV_{SS} = 0 V, T_A = –40 to +85°C, sampling frequency = 48 kHz, bandwidth = 20 Hz to 19.2 kHz, input signal = 1 kHz)

(1) AD Block

	Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
★	AD dynamic range	DR_X	–60 dB input	75	85	–	dB
★	AD total harmonic distortion	THD_X	–3 dB input	–	0.01	0.02	%
	AD absolute gain	G_X	0 dB input	–1.0	±0.5	+1.0	dB
★	AD frequency gain characteristic	GR_X	20 Hz to 19.2 kHz	–0.25	±0.1	+0.25	dB
★	AD offset voltage	V_{OFFX}		–50	±10	+50	mV
★	AD crosstalk	XTK_X	vs. input channel	–	–85	–70	dB
	AD full-scale analog input amplitude Note	$VIFS_X$		–	0.7	–	$V_{r.m.s.}$

Note The AD full-scale analog input amplitude ($VIFS_X$) indicates the input amplitude of the internal AD converter. Before inputting to the AD converter, calculate the amplitude that does not exceed this value from the setting values of MIC amp and each volume.

(2) DA Block

	Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
★	DA dynamic range	DR_R	–60 dB input	80	90	–	dB
★	DA total harmonic distortion	THD_R	–3 dB input	–	0.01	0.02	%
	DA absolute gain	G_R	0 dB input	–1.0	±0.5	+1.0	dB
★	DA frequency gain characteristic	GR_R	20 Hz to 19.2 kHz	–0.25	±0.1	+0.25	dB
★	DA offset voltage	V_{OFFR}		–50	±10	+50	mV
★	DA crosstalk	XTK_R	vs. input channel	–	–85	–70	dB
	DA full-scale analog output amplitude	$VOFS_R$		–	0.7	–	$V_{r.m.s.}$

(3) MIC Block

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
MIC absolute gain	G_{MC20}	–20 dB input, +20 dB = ON	18	20	22	dB

★ **(4) Mixer Block**

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Dynamic range	DR_A	–60 dB input	85	90	–	dB
Total harmonic distortion	THD_A	–3 dB input	–	0.01	0.02	%
Absolute gain	G_A	0 dB input	–1.0	±0.5	+1.0	dB
Frequency gain characteristic	GR_A	20 Hz to 19.2 kHz	–0.25	±0.1	+0.25	dB
Offset voltage	V_{OFFA}		–50	±10	+50	mV
Crosstalk	XTK_A	vs. input channel	–	–80	–70	dB
Full-scale analog input amplitude	$VIFS_A$		–	0.7	–	$V_{r.m.s.}$
Full-scale analog output amplitude	$VOFS_A$		–	0.7	–	$V_{r.m.s.}$

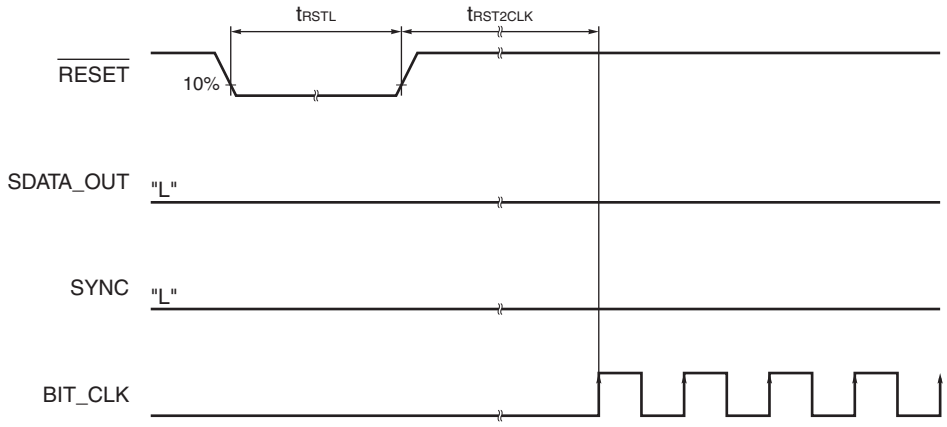
AC Characteristics (unless otherwise specified, DV_{DD} = AV_{DD} = 3.3 V, DV_{SS} = AV_{SS} = 0 V, T_A = –40 to +85°C)

(1) Cold Reset Timing

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
$\overline{\text{RESET}}$ low-level width [Notes 1, 2]	t_{RSTL}		1.0	–	–	μs
Setup time from $\overline{\text{RESET}}$ to BIT_CLK	$t_{RST2CLK}$		162.8	–	–	ns

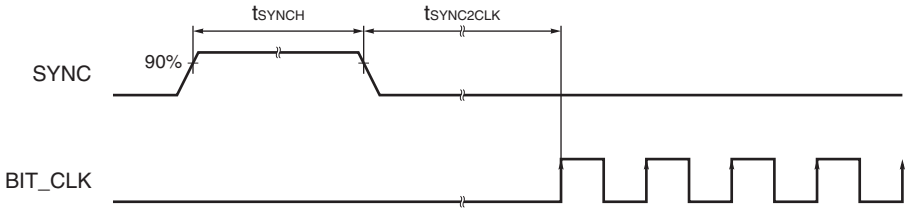
Notes 1. t_{RSTL} is the time required for initialization of this LSI. When performing a reset, set $\overline{\text{RESET}}$ to active (low level) for t_{RSTL} period.

2. The internal reset circuit operates as a trigger for the master clock. The master clock should be input even while executing a reset.



(2) Warm Reset Timing

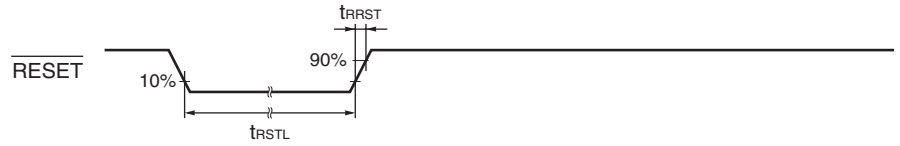
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
SYNC high-level width	t_{SYNCH}		–	1.3	–	μs
Setup time from SYNC to BIT_CLK	$t_{SYNC2CLK}$		162.8	–	–	ns



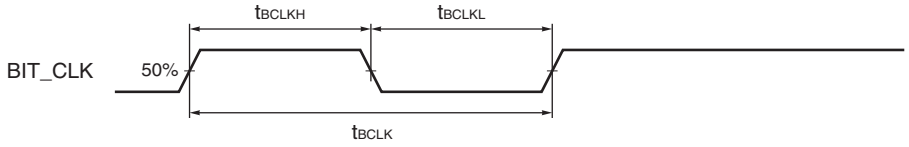
(3) Clock Timing

Parameter	Symbo	Conditions	Min.	Typ.	Max.	Unit
$\overline{\text{RESET}}$ rise time	t_{RRST}	Time for V_{DD} to change from 10% to 90%	–	–	1.0	μs
BIT_CLK frequency	f_{BCLK}		–	12.288	–	MHz
BIT_CLK cycle	t_{BCLK}		–	81.4	–	ns
BIT_CLK low-level width	t_{BCLKL}		36.0	40.7	45.0	ns
BIT_CLK high-level width	t_{BCLKH}		36.0	40.7	45.0	ns
SYNC frequency	f_{SYNC}		–	48	–	kHz
SYNC cycle	t_{SYNC}		–	20.8	–	μs
SYNC low-level width	t_{SYNCL}		–	19.5	–	μs
SYNC high-level width	t_{SYNCH}		–	1.3	–	μs

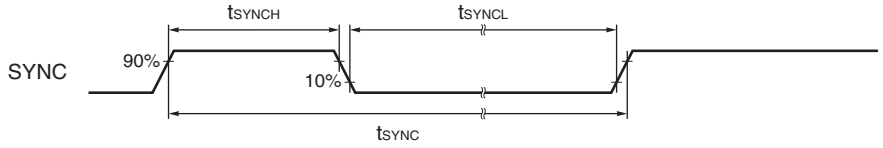
(a) $\overline{\text{RESET}}$ Timing



(b) BIT_CLK Timing

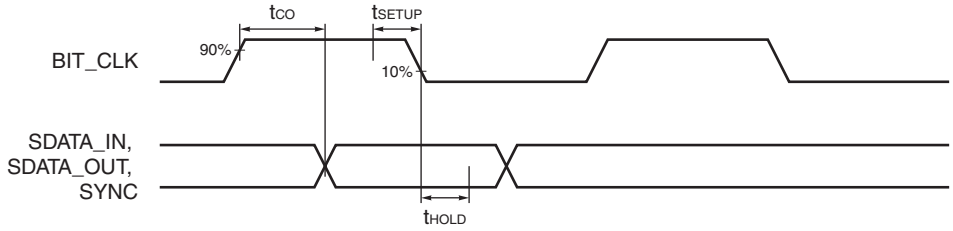


(c) SYNC Timing



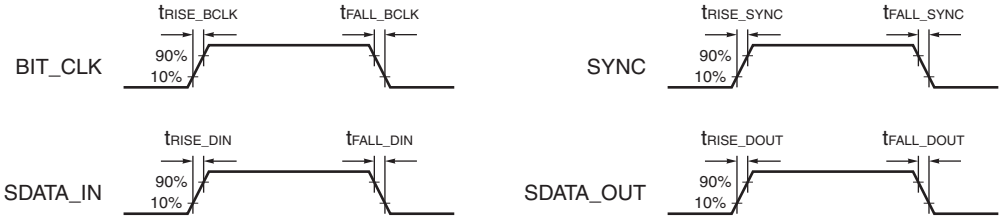
(4) AC-Link Timing

Parameter	Symbo	Conditions	Min.	Typ.	Max.	Unit
Delay time from BIT_CLK to data output	t_{CO}		–	–	15	ns
Data setup time	t_{SETUP}		10	–	–	ns
Data hold time	t_{HOLD}		10	–	–	ns



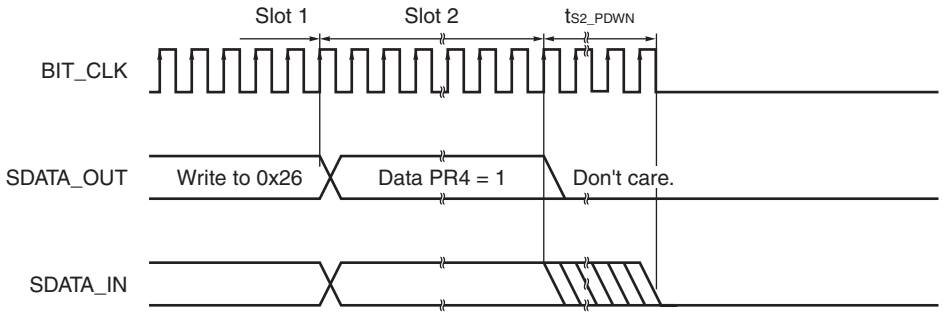
(5) Rise/Fall Timing

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
BIT_CLK rise time	t_{RISE_BCLK}	Time for V_{DD} to change from 10% to 90%	–	–	6	ns
BIT_CLK fall time	t_{FALL_BCLK}	Time for V_{DD} to change from 10% to 90%	–	–	6	ns
SYNC rise time	t_{RISE_SYNC}	Time for V_{DD} to change from 10% to 90%	–	–	6	ns
SYNC fall time	t_{FALL_SYNC}	Time for V_{DD} to change from 10% to 90%	–	–	6	ns
SDATA_IN rise time	t_{RISE_DIN}	Time for V_{DD} to change from 10% to 90%	–	–	6	ns
SDATA_IN fall time	t_{FALL_DIN}	Time for V_{DD} to change from 10% to 90%	–	–	6	ns
SDATA_OUT rise time	t_{RISE_DOUT}	Time for V_{DD} to change from 10% to 90%	–	–	6	ns
SDATA_OUT fall time	t_{FALL_DOUT}	Time for V_{DD} to change from 10% to 90%	–	–	6	ns

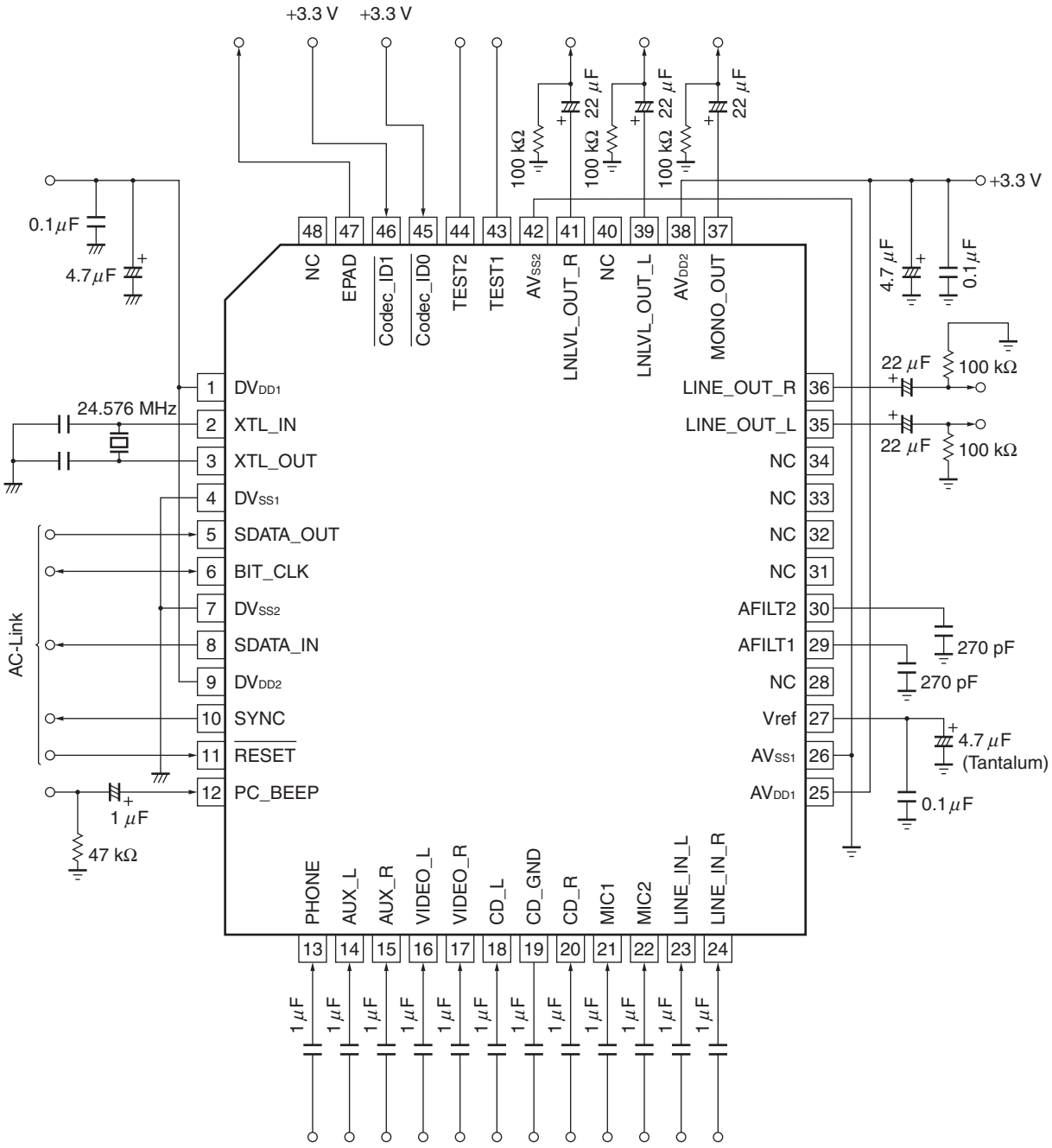


(6) Timing of AC-Link Low Power Mode

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Low-power mode transition time	t_{S2_PDWN}	Slot 2 data transfer to BIT_CLK, SDATA_IN = Low	–	–	1.0	μs



4. APPLICATION EXAMPLE

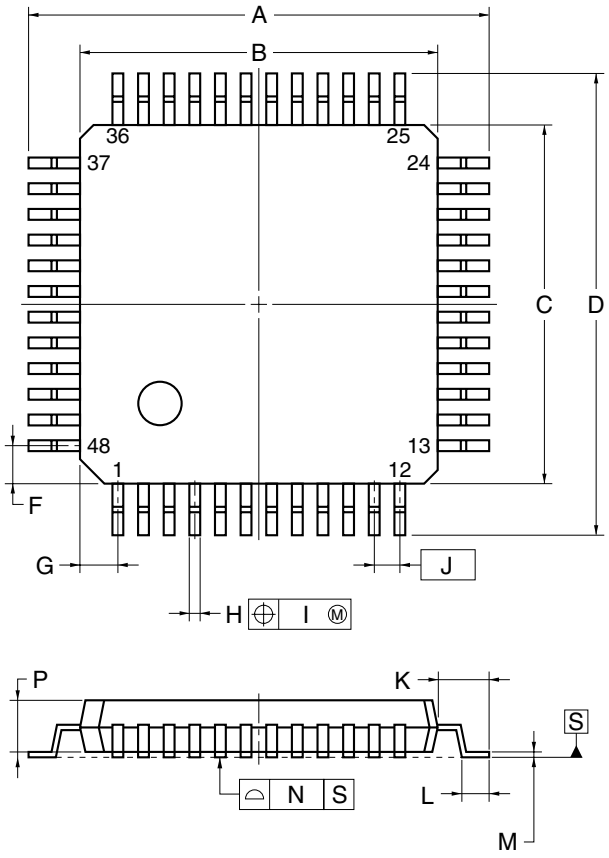


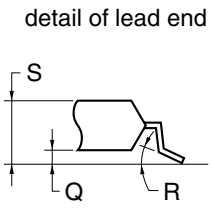
Remark ⏚ : Analog ground

⏚ : Digital ground

5. PACKAGE DRAWING

48-PIN PLASTIC TQFP (FINE PITCH) (7x7)





NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	9.0±0.2
B	7.0±0.2
C	7.0±0.2
D	9.0±0.2
F	0.75
G	0.75
H	$0.22^{+0.05}_{-0.04}$
I	0.10
J	0.5 (T.P.)
K	1.0±0.2
L	0.5±0.2
M	$0.145^{+0.055}_{-0.045}$
N	0.10
P	1.0±0.1
Q	0.1±0.05
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.27 MAX.

S48GA-50-9EU-2

6. RECOMMENDED SOLDERING CONDITIONS

The μPD63315 should be soldered and mounted under the following recommended conditions.

For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Table 6-1. Surface Mounting Type Soldering Conditions

- **μPD63315GA-9EU: 48-pin plastic TQFP (fine pitch) (7 × 7)**

	Soldering Method	Soldering Conditions	Recommended Condition Symbol
★	Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds Max. (at 210°C or higher), Count: three times or less, Exposure limit [Note]: 3 days (after that, prebaking is necessary at 125°C for 10 hours)	IR35-103-3
★	VPS	Package peak temperature: 215°C, Time: 40 seconds Max. (at 200°C or higher), Count: three times or less, Exposure limit [Note]: 3 days (after that, prebaking is necessary at 125°C for 10 hours)	VP15-103-3
	Partial heating	Pin temperature: 300°C Max., Time: 3 seconds Max. (per pin row)	–

Note The number of days for storage after the dry pack has been opened. Storage conditions are 25°C and 65% RH max.

Caution Do not use different soldering methods together (except for partial heating).

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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  "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

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