

4-BIT SINGLE-CHIP MICROCONTROLLER

The μ PD754304 is one of the "75XL Series" 4-bit single-chip microcontrollers with data processing capability comparable to that of 8-bit microcontrollers. The μ PD754303(A) has a higher reliability than the μ PD754304.

The microcontrollers in the 75XL Series have expanded CPU functions than those of the 75X Series and can operate at a voltage of as low as 1.8 V; therefore, they are ideal for battery-driven application systems.

As the one-time PROM version of the μ PD754304, the μ PD75P4308 is ideal for evaluation of a system under development or for small-scale production of application systems.

Detailed information about functions can be found in the following document. Be sure to read the following document before designing.

μ PD754304 User's Manual: U10123E

FEATURES

- Low-voltage operation: $V_{DD} = 1.8$ to 5.5 V
- Internal memory
 - Program memory (ROM):
 - 2048 \times 8 bits (μ PD754302, 754302(A))
 - 4096 \times 8 bits (μ PD754304, 754304(A))
 - Data memory (RAM): 256 \times 4 bits
- Variable instruction execution time effective for high-speed operation and power saving
 - 0.95, 1.91, 3.81, or 15.3 μ s (at 4.19 MHz)
 - 0.67, 1.33, 2.67, or 10.7 μ s (at 6.0 MHz)
- Internal serial interface (1 channel)
- Powerful timer function (3 channels)
- Inherits instruction set of existing 75X Series for easy replacement

APPLICATIONS

- μ PD754302, 754302(A)
Cordless telephones, TVs, VCRs, audio systems, household appliances, office machines, etc.
- ★ • μ PD754304, 754304(A)
Automotive appliance, etc.
- ★ The μ PD754302 and 754304 differ from the μ PD754302(A) and 754304(A) only in terms of their quality grade. Unless otherwise specified, the μ PD754304 is treated as a representative model in this Data Sheet. For the models other than the μ PD754304, μ PD754304 can be read as the other model name. If different descriptions are made for the μ PD754302 and 754304, the (A) models correspond as follows:
 μ PD754302 \rightarrow μ PD754302(A), μ PD754304 \rightarrow μ PD754304(A)

The information in this document is subject to change without notice.

ORDERING INFORMATION

| | Parts Number | Package | Quality Grade |
|---|--------------------|---|---------------|
| | μPD754302GS-xxx | 36-pin plastic shrink SOP (300 mil, 0.8 mm pitch) | Standard |
| | μPD754304GS-xxx | 36-pin plastic shrink SOP (300 mil, 0.8 mm pitch) | Standard |
| ★ | μPD754302GS(A)-xxx | 36-pin plastic shrink SOP (300 mil, 0.8 mm pitch) | Special |
| ★ | μPD754304GS(A)-xxx | 36-pin plastic shrink SOP (300 mil, 0.8 mm pitch) | Special |

Remark × indicates a ROM code number.

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

★ **Difference between μPD75430× and μPD75430×(A)**

| Parts Number | μPD754302 | μPD754302(A) |
|---------------|-----------|--------------|
| Item | μPD754304 | μPD754304(A) |
| Quality grade | Standard | Special |

Functional Outline

| Parameter | | Function | |
|-------------------------------|--------------------------------------|---|--|
| Instruction execution time | | <ul style="list-style-type: none"> • 0.95, 1.91, 3.81, 15.3 μs (@ 4.19 MHz with system clock) • 0.67, 1.33, 2.67, 10.7 μs (@ 6.0 MHz with system clock) | |
| On-chip memory | ROM | 2048 × 8 bits (μPD754302) | |
| | | 4096 × 8 bits (μPD754304) | |
| | RAM | 256 × 4 bits | |
| General-purpose register | | <ul style="list-style-type: none"> • 4-bit operation: 8 × 4 banks • 8-bit operation: 4 × 4 banks | |
| Input/ output port | CMOS input | 8 | On-chip pull-up resistors can be specified by software: 7 |
| | CMOS input/output | 18 | On-chip pull-up resistors can be specified by software: 18 |
| | N-ch open-drain input/output pins | 4 | 13 V withstand voltage. On-chip pull-up resistors can be specified by mask option. |
| | Total | 30 | |
| Timer | | 3 channels <ul style="list-style-type: none"> • 8-bit timer/event counter: 2 channels (16-bit timer/event counter) • Basic interval timer/watchdog timer: 1 channel | |
| Serial interface | | <ul style="list-style-type: none"> • 3-wire serial I/O mode ... MSB or LSB can be selected for transferring top bit • 2-wire serial I/O mode | |
| Bit sequential buffer | | 16 bits | |
| Clock output (PCL) | | <ul style="list-style-type: none"> • Φ, 524, 262, 65.5 kHz (@ 4.19 MHz with system clock) • Φ, 750, 375, 93.8 kHz (@ 6.0 MHz with system clock) | |
| Vectored interrupts | | External: 3, Internal: 4 | |
| Test input | | External: 1 | |
| System clock oscillator | | Ceramic or crystal oscillator | |
| Standby function | | STOP/HALT mode | |
| Operating ambient temperature | | T _A = -40 to +85 °C | |
| Power supply voltage | | V _{DD} = 1.8 to 5.5 V | |
| Package | | 36-pin plastic shrink SOP (300 mil, 0.8-mm pitch) | |

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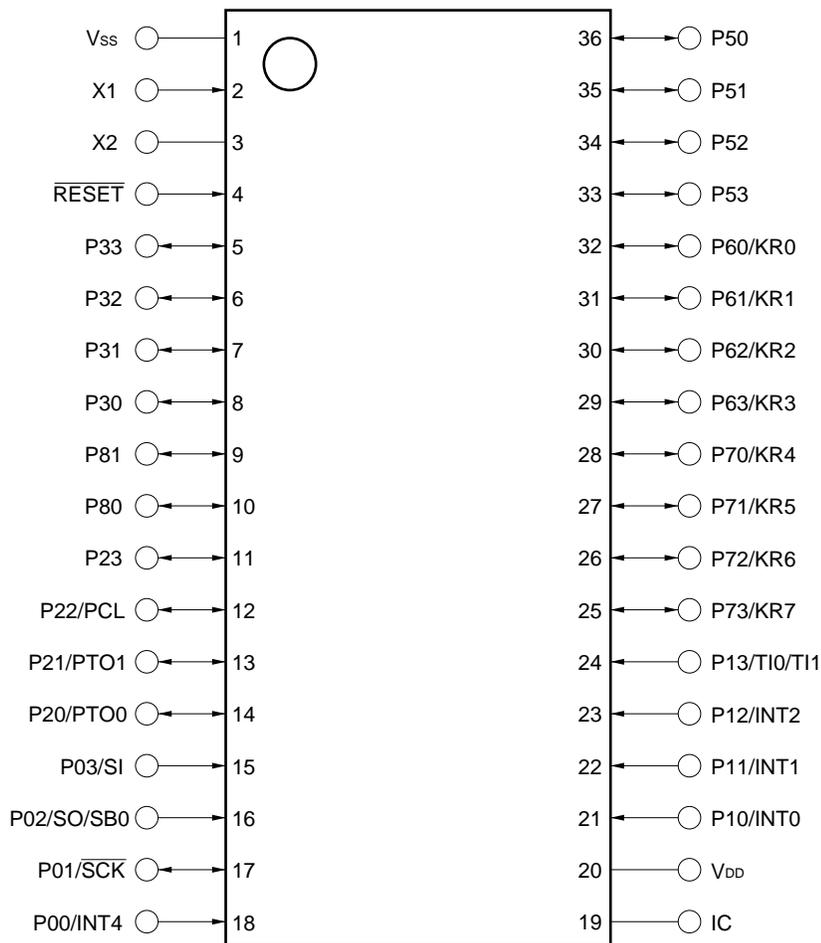
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1. PIN CONFIGURATION (Top View)

36-pin plastic shrink SOP (300 mil, 0.8-mm pitch)

μPD754302GS-xxx, μPD754302GS(A)-xxx

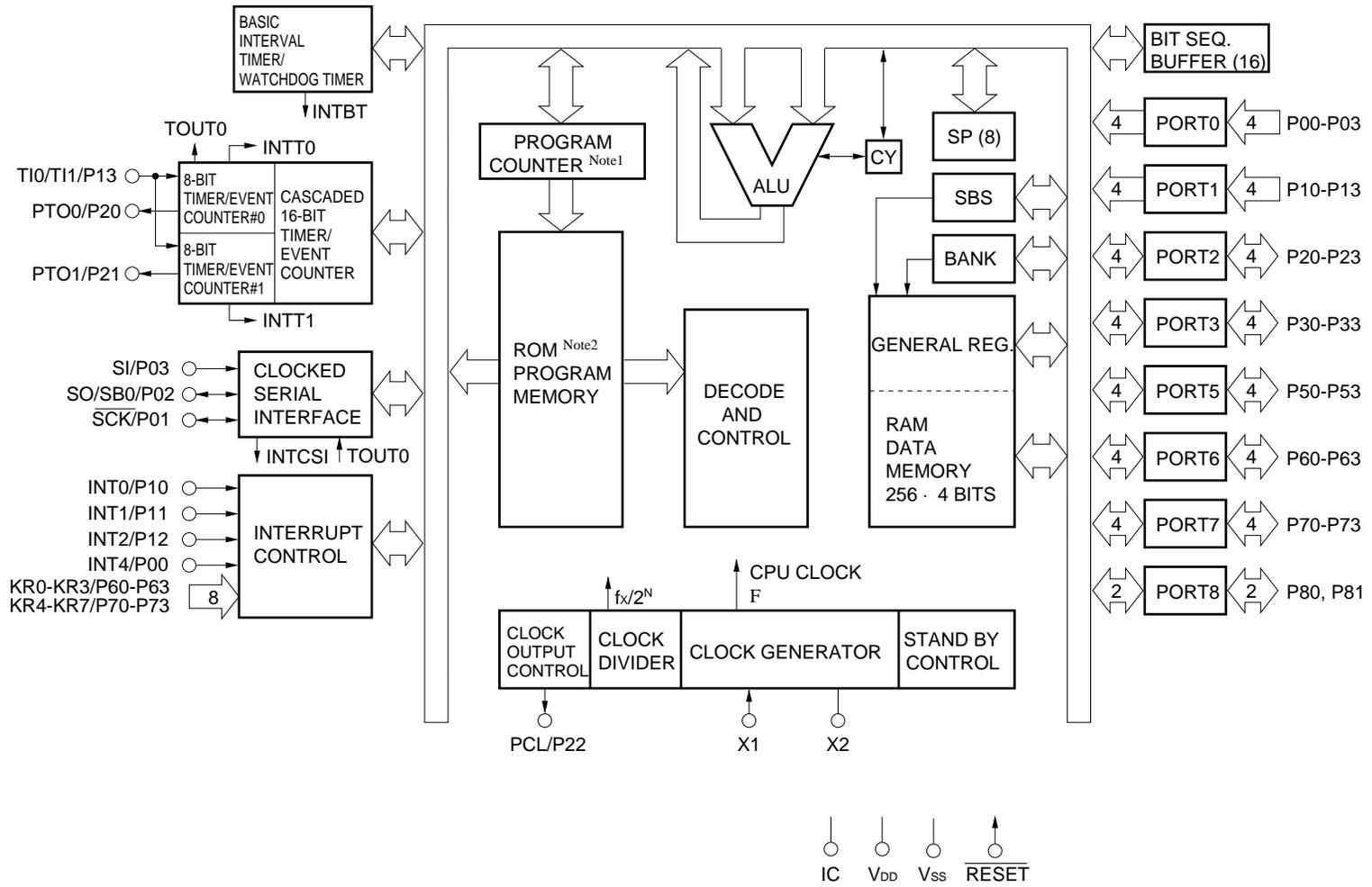
μPD754304GS-xxx, μPD754304GS(A)-xxx



IC: Internally Connected (Connect directly this pin to V_{DD}.)

PIN IDENTIFICATION

| | |
|--|--|
| P00-P03 : PORT0 | $\overline{\text{RESET}}$: Reset Input |
| P10-P13 : PORT1 | TI0, TI1 : Timer Input 0, 1 |
| P20-P23 : PORT2 | PTO0, PTO1: Programmable Timer Output 0, 1 |
| P30-P33 : PORT3 | PCL : Programmable Clock |
| P50-P53 : PORT5 | INT0, 1, 4 : External Vectored Interrupt 0, 1, 4 |
| P60-P63 : PORT6 | INT2 : External Test Input 2 |
| P70-P73 : PORT7 | V _{SS} : GND |
| P80, P81: PORT8 | X1, X2 : System Clock Oscillation 1, 2 |
| KR0-KR7: Key Return 0-7 | IC : Internally Connected |
| $\overline{\text{SCK}}$: Serial Clock | V _{DD} : Positive Power Supply |
| SI : Serial Input | |
| SO : Serial Output | |
| SB0 : Serial data Bus 0 | |



- Notes**
1. The μPD754302 and μPD754304 program counters are 11 and 12 bits, respectively.
 2. The ROM capacity of the μPD754302 is 2048 × 8 bits, and that of the μPD754304 is 4096 × 8 bits.

3. PIN FUNCTION

3.1 Port Pins

| Pin Name | Input/Output | Alternate Function | Function | 8-bit I/O | After Reset | I/O Circuit TYPE <small>Note 1</small> |
|-------------------------------|--------------|--------------------|--|-----------|--|--|
| P00 | Input | INT4 | 4-bit input port (PORT0). | × | Input | ⓑ |
| P01 | Input/Output | SCK | For P01 to P03, on-chip pull-up resistors can be specified by software in 3-bit units. | | | ⓕ-A |
| P02 | Input/Output | SO/SB0 | | | | ⓕ-B |
| P03 | Input | SI | | | | ⓑ-C |
| P10 | Input | INT0 | 4-bit input port (PORT1). | × | Input | ⓑ-C |
| P11 | | INT1 | On-chip pull-up resistors can be specified by software in 4-bit units. | | | |
| P12 | | INT2 | Noise elimination circuit can be selected | | | |
| P13 | | TI0/TI1 | (Only P10/INT0) | | | |
| P20 | Input/Output | PTO0 | 4-bit input/output port (PORT2). | × | Input | E-B |
| P21 | | PTO1 | On-chip pull-up resistors can be specified by software in 4-bit units. | | | |
| P22 | | PCL | | | | |
| P23 | | – | | | | |
| P30 | Input/Output | – | Programmable 4-bit input/output port (PORT3). | × | Input | E-B |
| P31 | | – | This port can be specified for input/output bit-wise. On-chip pull-up resistor can be specified by software in 4-bit units. | | | |
| P32 | | – | | | | |
| P33 | | – | | | | |
| P50-P53 <small>Note 2</small> | Input/Output | – | N-ch open-drain 4-bit input/output port (PORT5). A pull-up resistor can be contained bit-wise (mask option). Withstand voltage is 13 V in open-drain mode. | × | High level (when pull-up resistors are provided) or high-impedance | M-D |
| P60 | Input/Output | KR0 | Programmable 4-bit input/output port (PORT6). | √ | Input | ⓕ-A |
| P61 | | KR1 | This port can be specified for input/output bit-wise. On-chip pull-up resistors can be specified by software in 4-bit units. | | | |
| P62 | | KR2 | | | | |
| P63 | | KR3 | | | | |
| P70 | Input/Output | KR4 | 4-bit input/output port (PORT7). | | Input | ⓕ-A |
| P71 | | KR5 | On-chip pull-up resistors can be specified by software in 4-bit units. | | | |
| P72 | | KR6 | | | | |
| P73 | | KR7 | | | | |
| P80 | Input/Output | – | 2-bit input/output port (PORT8). | × | Input | E-B |
| P81 | | – | On-chip pull-up resistors can be specified by software in 2-bit units. | | | |

- Notes**
1. Circled characters indicate the Schmitt-trigger input.
 2. If on-chip pull-up resistors are not specified by mask option (when used as N-ch open-drain input port), low level input leakage current increases when input or bit manipulation instruction is executed.

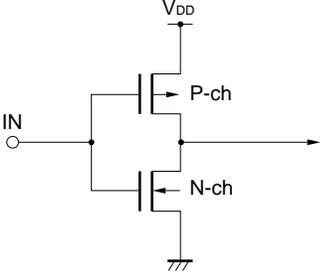
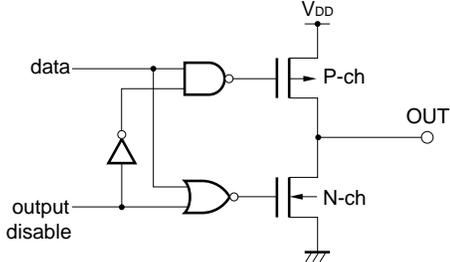
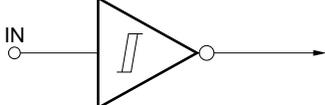
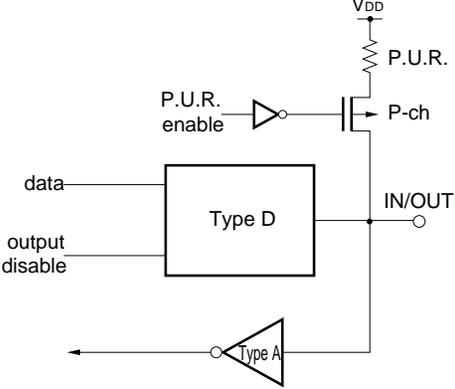
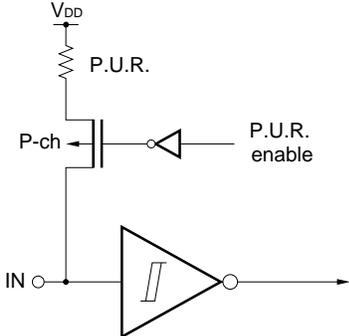
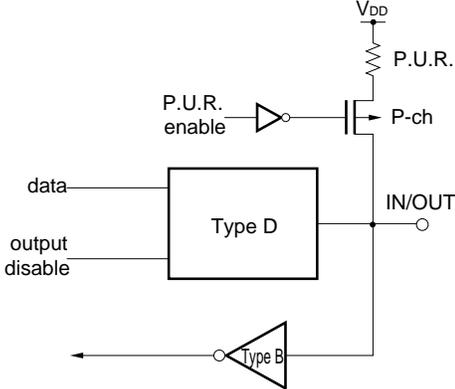
3.2 Non-port Pins

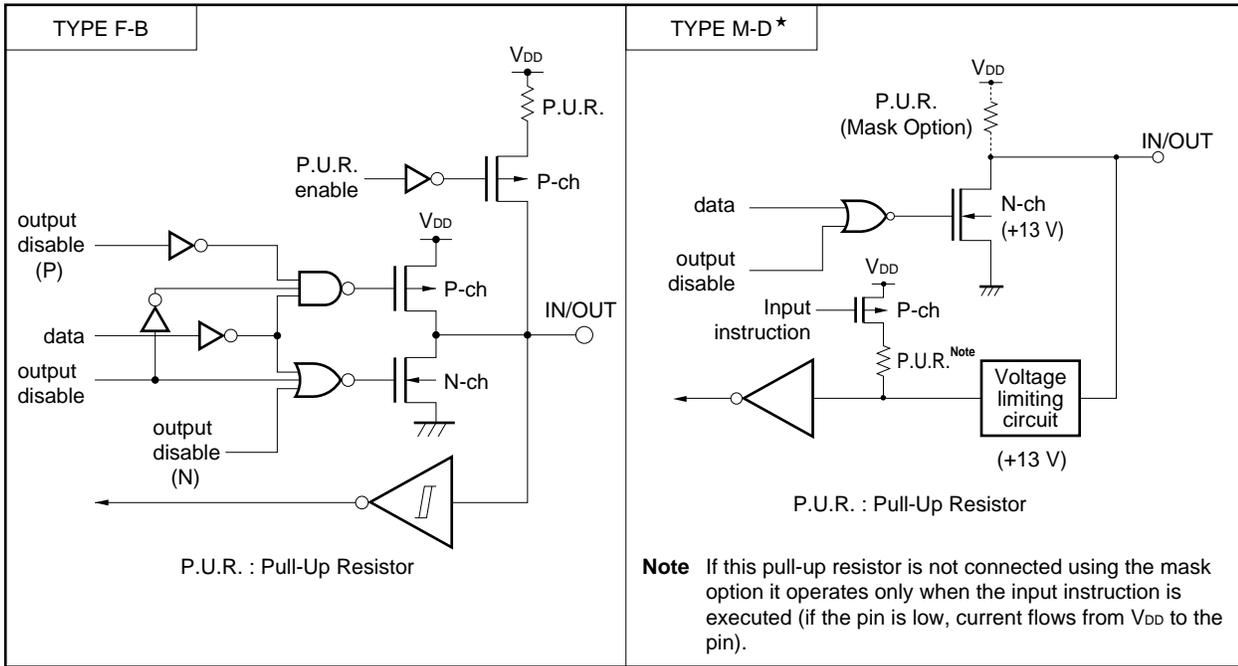
| Pin Name | Input/Output | Alternate Function | Function | After Reset | I/O Circuit TYPE <small>Note</small> | |
|-----------------|--------------|--------------------|--|---|--------------------------------------|-----|
| TI0/TI1 | Input | P13 | Inputs external event pulses to the timer/event counter. | Input | ⓑ-C | |
| PTO0 | Output | P20 | Timer/event counter output | Input | E-B | |
| PTO1 | | P21 | | | | |
| PCL | | P22 | Clock output | | | |
| SCK | Input/Output | P01 | Serial clock input/output | Input | ⓕ-A | |
| SO/SB0 | | P02 | Serial data output Serial data bus input/output | | ⓕ-B | |
| SI | | | P03 | | Serial data input | ⓑ-C |
| INT4 | Input | P00 | Edge detection vectored interrupt input (both rising edge and falling edge detection) | Input | ⓑ | |
| INT0 | Input | P10 | Edge detection vectored interrupt input (detection edge can be selected). INT0/P10 can select a noise elimination circuit. | Asynchronous with noise elimination circuit can be selected | Input | ⓑ-C |
| INT1 | | P11 | Asynchronous | | | |
| INT2 | Input | P12 | Edge detection testable input (rising edge detection) | Asynchronous | Input | ⓑ-C |
| KR0-KR3 | Input | P60-P63 | Testable input (falling edge detection) | Input | ⓕ-A | |
| KR4-KR7 | | P70-P73 | | | | |
| X1 | Input | - | Crystal/ceramic connection pin for the system clock oscillator. When inputting the external clock, input the external clock to pin X1, and the inverted phase of the external clock to pin X2. | - | - | |
| X2 | - | | | | | |
| RESET | Input | - | System reset input (low-level active) | - | ⓑ | |
| IC | - | - | Internally connected. Connect directly to V _{DD} . | - | - | |
| V _{DD} | - | - | Positive power supply | - | - | |
| V _{SS} | - | - | Ground potential | - | - | |

Note Circled characters indicate the Schmitt-trigger input.

3.3 Pin Input/Output Circuits

The μ PD754304 pin input/output circuits are shown schematically.

| | |
|---|---|
| <p>TYPE A</p>  <p>CMOS specification input buffer.</p> | <p>TYPE D</p>  <p>Push-pull output that can be placed in output high-impedance (both P-ch, N-ch off).</p> |
| <p>TYPE B</p>  <p>Schmitt trigger input having hysteresis characteristic.</p> | <p>TYPE E-B</p>  <p>P.U.R. : Pull-Up Resistor</p> |
| <p>TYPE B-C</p>  <p>P.U.R. : Pull-Up Resistor</p> | <p>TYPE F-A</p>  <p>P.U.R. : Pull-Up Resistor</p> |



3.4 Recommended Connections for Unused Pins

Table 3-1. List of Recommended Connections for Unused Pins

| Pin | Recommended Connection |
|------------------------------|---|
| ★ P00/INT4 | Connect to V _{SS} or V _{DD} |
| P01/ $\overline{\text{SCK}}$ | Connect to V _{SS} or V _{DD} through the resistor individually |
| P02/SO/SB0 | |
| P03/SI | Connect to V _{SS} |
| ★ P10/INT0-P12/INT2 | Connect to V _{SS} or V _{DD} |
| ★ P13/TI0/TI1 | |
| P20/PTO0 | Input state : Connect to V _{SS} or V _{DD} through the resistor individually |
| P21/PTO1 | |
| P22/PCL | Output state : Leave open |
| P23 | |
| P30-P33 | |
| ★ P50-P53 | Input state : Connect to V _{SS} Output state : Connect to V _{SS} (Pull-up resistor by mask option should not be connected) |
| P60/KR0-P63/KR3 | Input state : Connect to V _{SS} or V _{DD} through the resistor individually |
| P70/KR4-P73/KR7 | |
| P80, P81 | Output state : Leave open |
| IC | Connect to V _{DD} directly |

4. SWITCHING FUNCTION BETWEEN Mk I MODE AND Mk II MODE

4.1 Difference between Mk I and Mk II Modes

The CPU of μPD754304 has the following two modes: Mk I and Mk II, either of which can be selected. The mode can be switched by the bit 3 of the stack bank select register (SBS).

- Mk I mode: Can be used in the 75XL CPU with a ROM capacity of up to 16K bytes.
- Mk II mode: Can be used in all the 75XL CPU's including those products whose ROM capacity is more than 16K bytes.

Table 4-1. Differences between Mk I Mode and Mk II Mode

| | Mk I mode | Mk II mode |
|--|------------------|------------------|
| Number of stack bytes for subroutine instructions | 2 bytes | 3 bytes |
| BRA !addr1 instruction CALLA !addr1 instruction | Not available | Available |
| CALL !addr instruction | 3 machine cycles | 4 machine cycles |
| CALLF !faddr instruction | 2 machine cycles | 3 machine cycles |

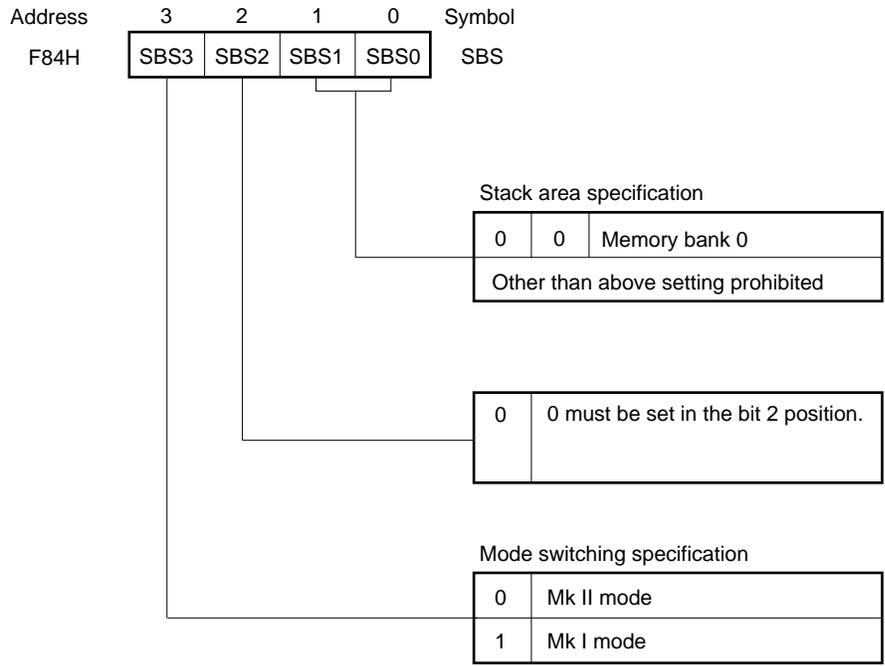
- ★ **Caution** The Mk II mode supports a program area exceeding 16K bytes in the 75X and 75XL series. This mode can improve software compatibility with products with a program area of more than 16K bytes.
- When Mk II mode is selected, the number of stack bytes when a subroutine call instruction is executed is greater by 1 byte per stack compared with the Mk I mode. When the CALL !addr or CALLF !faddr instruction is used, one more machine cycle is required. To emphasize the efficiency of the RAM and processing speed rather than software compatibility, therefore, use the Mk I mode.

4.2 Setting Method of Stack Bank Select Register (SBS)

Switching between the Mk I mode and Mk II mode can be done by the SBS. Figure 4-1 shows the format. The SBS is set by a 4-bit memory manipulation instruction.

When using the Mk I mode, the SBS must be initialized to 1000B at the beginning of a program. When using the Mk II mode, it must be initialized to 0000B.

Figure 4-1. Stack Bank Select Register Format



Caution Since SBS. 3 is set to “1” after a RESET signal is generated, the CPU operates in the Mk I mode. When executing an instruction in the Mk II mode, set SBS. 3 to “0” to select the Mk II mode.

5. MEMORY CONFIGURATION

- **Program Memory (ROM)** 2048 × 8 bits (μ PD754302)
.... 4096 × 8 bits (μ PD754304)

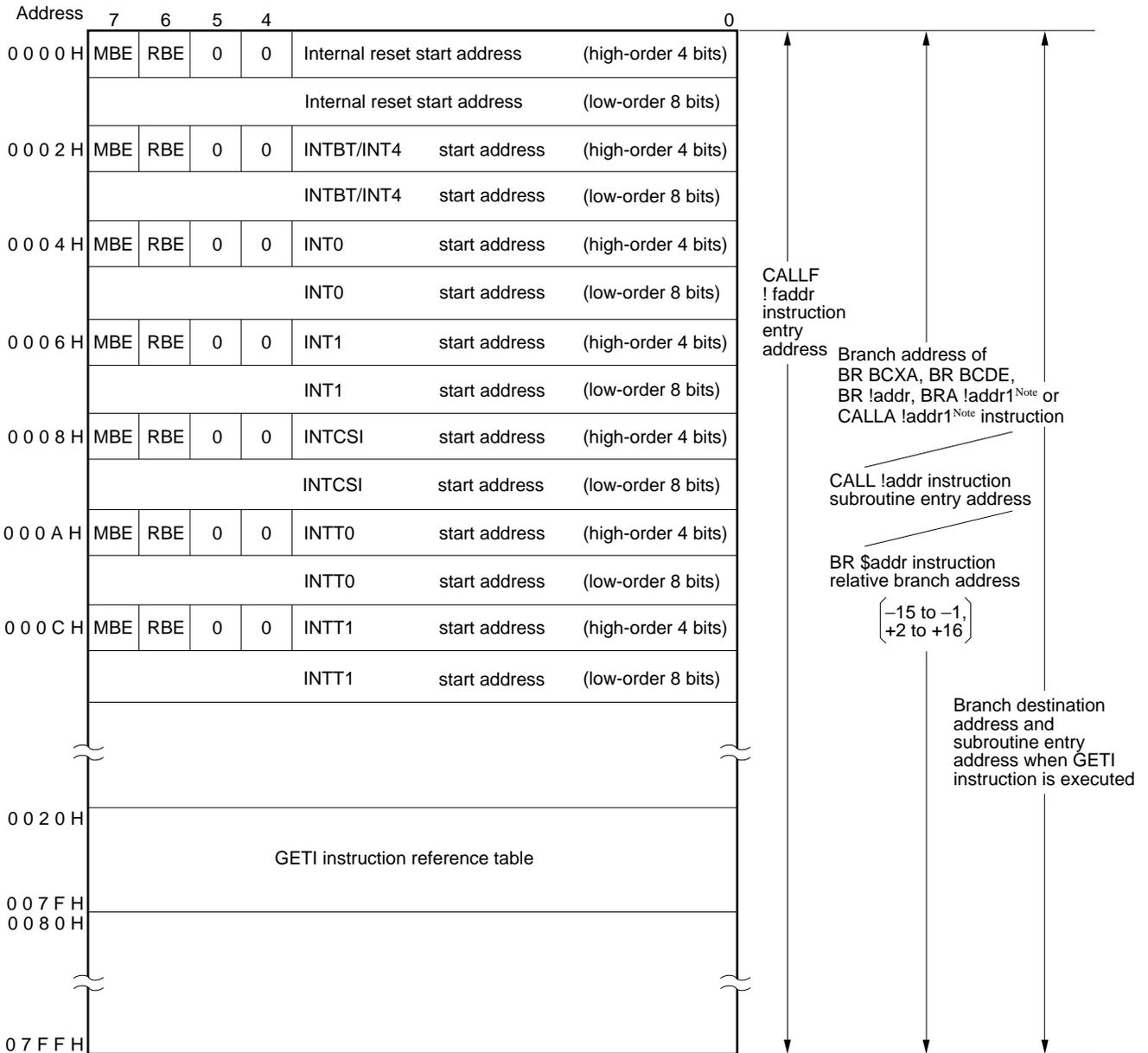
- Addresses 0000H and 0001H
Vector table wherein the program start address and the values set for the RBE and MBE at the time a $\overline{\text{RESET}}$ signal is generated are written. Reset and start are possible at an arbitrary address.
- Addresses 0002H-000DH
Vector table wherein the program start address and values set for the RBE and MBE by the vectored interrupts are written. Interrupt execution can be started at an arbitrary address.
- Addresses 0020H-007FH
Table area referenced by the GETI instruction ^{Note}.

Note The GETI instruction realizes a 1-byte instruction on behalf of an arbitrary 2-byte instruction, 3-byte instruction, or two 1-byte instructions. It is used to decrease the program steps.

- **Data Memory (RAM)**
 - Data area 256 words × 4 bits (000H-0FFH)
 - Peripheral hardware area 128 words × 4 bits (F80H-FFFH)

Figure 5-1. Program Memory Map (1/2)

(a) μPD754302

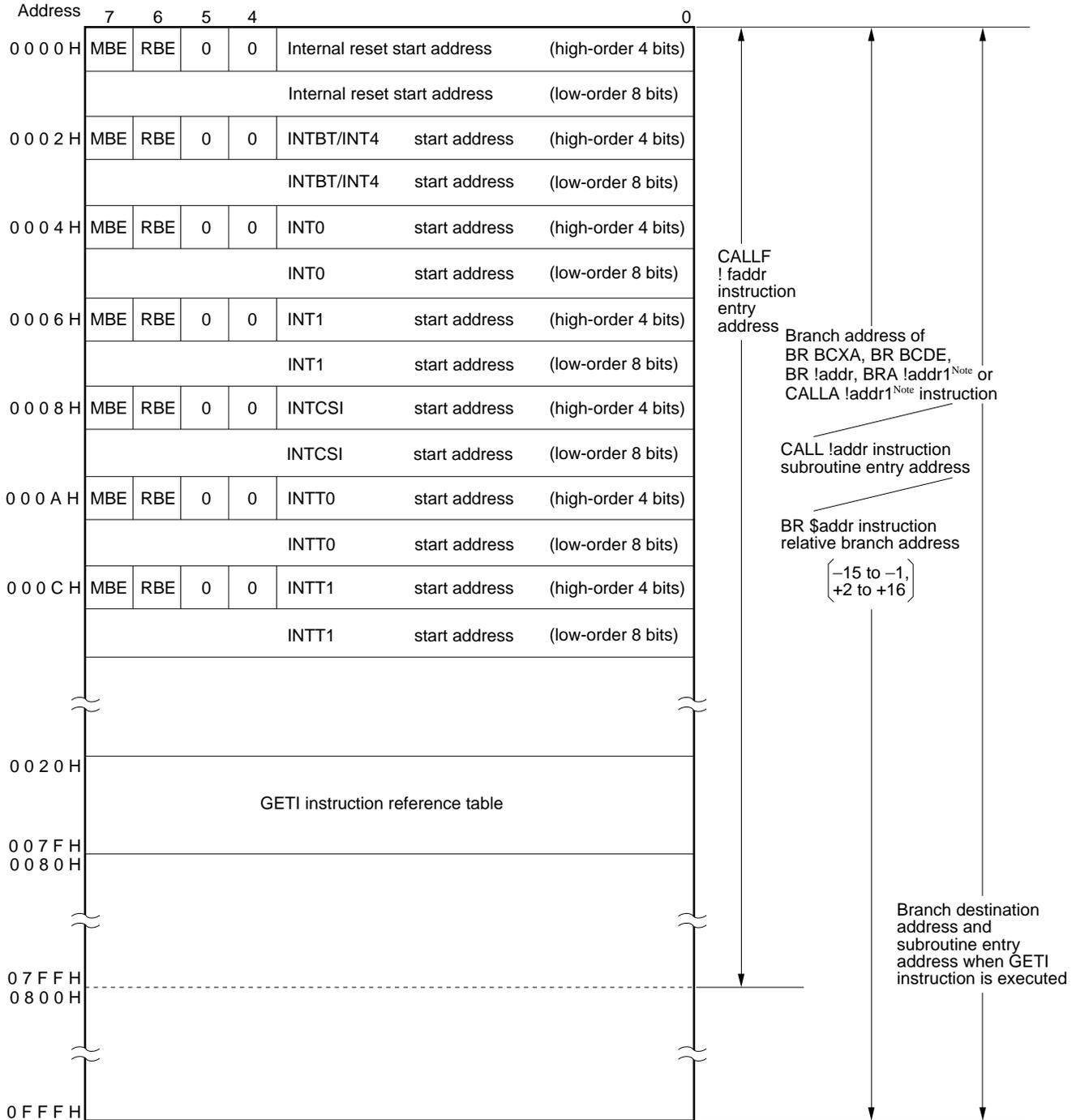


★ **Note** Can be used in the Mk II mode only.

Remark In addition to the above, a branch can be taken to the address indicated by changing only the low-order eight bits of PC by executing the BR PCDE or BR PCXA instruction.

Figure 5-1. Program Memory Map (2/2)

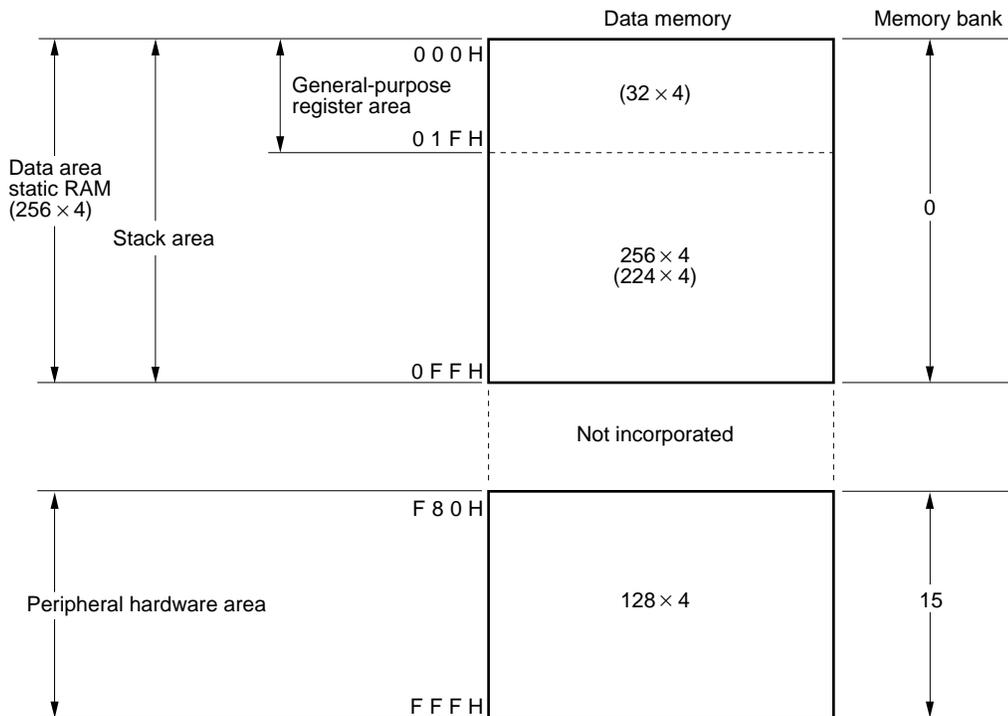
(b) μPD754304



★ **Note** Can be used in the Mk II mode only.

Remark In addition to the above, a branch can be taken to the address indicated by changing only the low-order eight bits of PC by executing the BR PCDE or BR PCXA instruction.

Figure 5-2. Data Memory Map



6. PERIPHERAL HARDWARE FUNCTIONS

6.1 Digital Input Ports

The following three types of I/O ports are provided.

- CMOS input (Ports 0, 1) : 8
 - CMOS I/O (Ports 2, 3, 6 to 8) : 18
 - N-ch open-drain I/O (Port 5) : 4
-
- Total 30

Table 6-1. Types and Features of Digital Ports

| Port Name | Function | Operation, Features | | Remark |
|-----------|-------------|--|---|--|
| PORT0 | 4-bit input | When serial interface function is used, multiplexed pin has output function depending on operation mode. | | Multiplexed with INT4, $\overline{\text{SCK}}$, SO/SB0, and SI pins |
| PORT1 | | Input port. | | Multiplexed with INT0 through INT2 and TI0/TI1 pins. |
| PORT2 | 4-bit I/O | Can be set in input or output mode in 4-bit units. | | Multiplexed with PTO0, PTO1, and PCL pins. |
| PORT3 | | Can be set in input or output mode in 1-bit units. | | |
| PORT5 | | 4-bit I/O (N-ch open-drain, 13 V) | Can be set in input or output mode in 4-bit units. Pull-up resistor can be connected in 1-bit units by mask option. | |
| PORT6 | 4-bit I/O | Can be set in input or output mode in 1-bit units. | Ports 6 and 7 are used in pairs and can input or output data in 8-bit units. | Multiplexed with KR0 through KR3 pins. |
| PORT7 | | Can be set in input or output mode in 4-bit units. | | Multiplexed with KR4 through KR7 pins. |
| PORT8 | 2-bit I/O | Can be set in input or output mode in 2-bit units. | | — |

6.2 Clock Generator

• Clock generator configuration

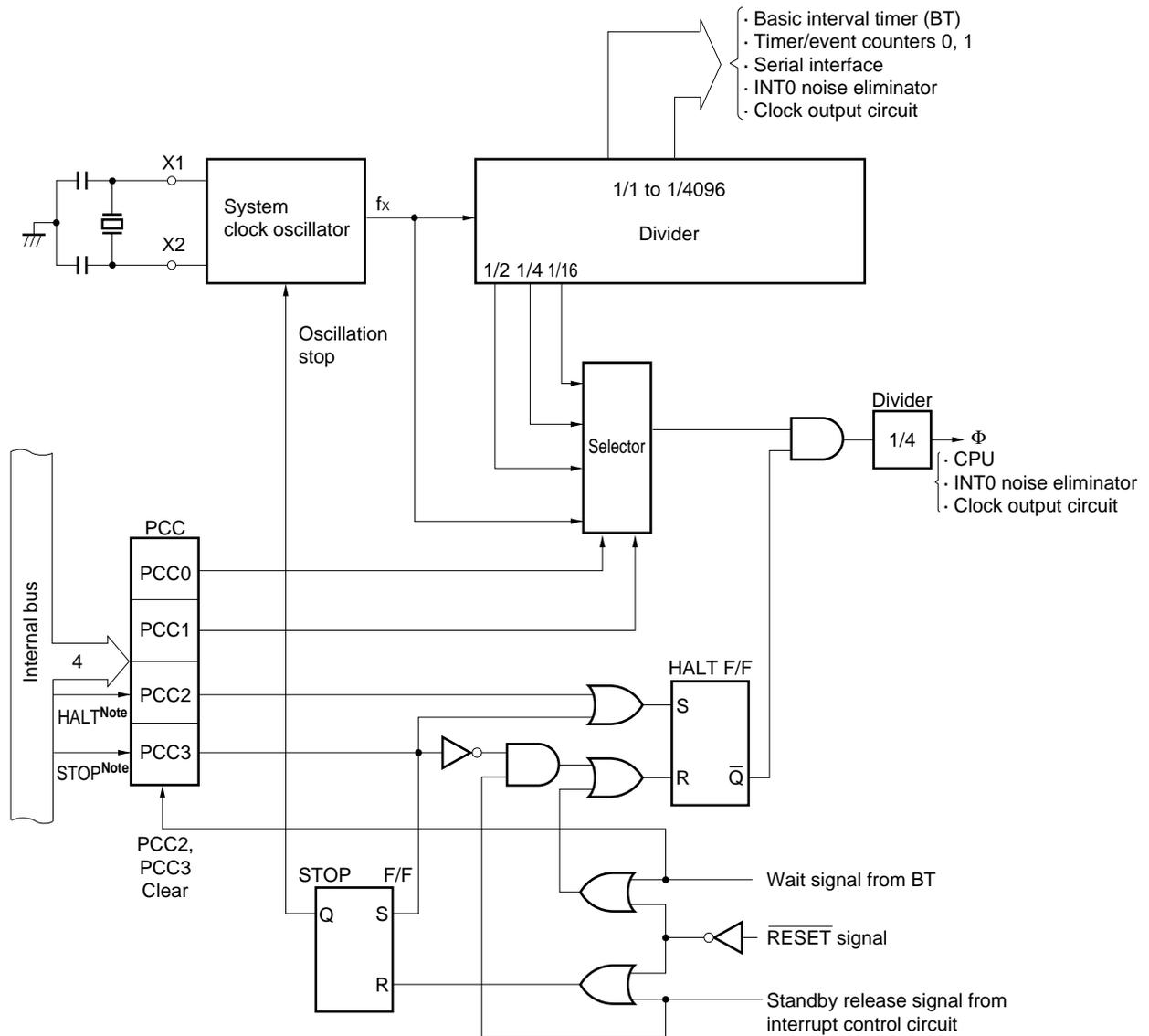
The clock generator provides the clock signals to the CPU and peripheral hardware and its configuration is shown in Figure 6-1.

The operation of the clock generator is set with the processor clock control register (PCC).

The instruction execution time can be changed.

- 0.95, 1.91, 3.81, 15.3 μ s (system clock operating at 4.19 MHz)
- 0.67, 1.33, 2.67, 10.7 μ s (system clock operating at 6.0 MHz)

Figure 6-1. Clock Generator Block Diagram



Note Instruction execution

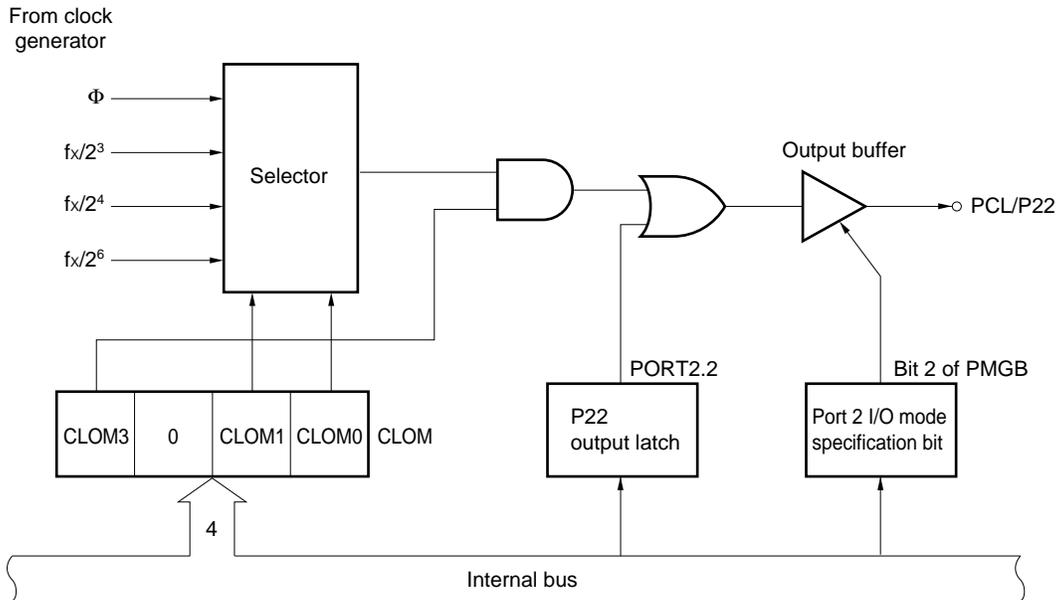
- Remarks**
1. f_x = System clock frequency
 2. Φ = CPU clock
 3. PCC: Processor Clock Control Register
 4. One clock cycle (t_{CY}) of the CPU clock is equal to one machine cycle of the instruction.

6.3 Clock Output Circuit

The clock output circuit outputs clock pulses from the P22/PCL pin, and is used to apply for remote controller waveform output or to supply clock pulse peripheral LSIs.

- Clock output (PCL) : Φ , 524, 262, 65.5 kHz (during 4.19-MHz operation)
 Φ , 750, 375, 93.8 kHz (during 6.0-MHz operation)

Figure 6-2. Clock Output Circuit Block Diagram



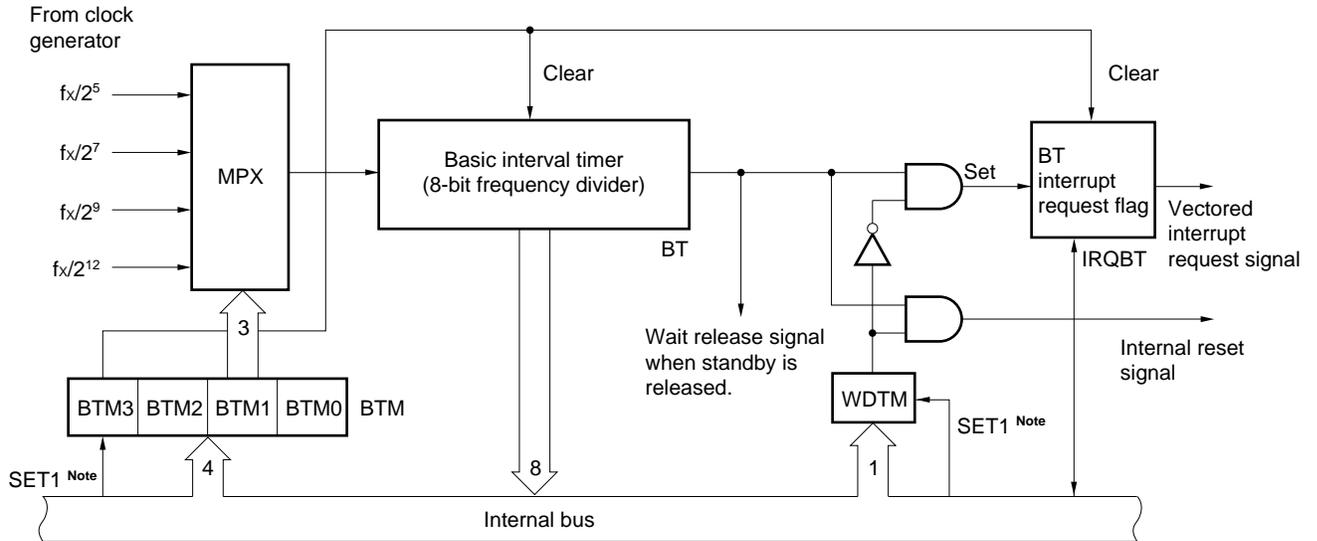
Remark Special care has been taken in designing the chip so that small-width pulses may not be output when switching clock output enable/disable.

6.4 Basic Interval Timer/Watchdog Timer

The basic interval timer/watchdog timer has the following functions.

- Interval timer operation to generate a reference time interrupt
- Watchdog timer operation to detect a runaway of program and reset the CPU
- Selects and counts the wait time when the standby mode is released
- Reads the contents of counting

Figure 6-3. Basic Interval Timer/Watchdog Timer Block Diagram



Note Instruction execution

6.5 Timer/Event Counter

The μPD754304 has two channels of timer/event counters. Its configuration is shown in Figures 6-4 and 6-5.

The timer/event counter has the following functions.

- Programmable interval timer operation
- Square wave output of any frequency to the PTO_n pin (n = 0, 1)
- Event counter operation
- Divides the frequency of signal input via the TIn pin to 1-Nth of the original signal and outputs the divided frequency to the PTO_n pin (frequency divider operation).
- Supplies the shift clock to the serial interface circuit.
- Reads the count value.

The timer/event counter operates in the following two modes as set by the mode register.

Table 6-2. Operation Modes of Timer/Event Counter

| Mode | Channel | |
|---------------------------------|-----------|-----------|
| | Channel 0 | Channel 1 |
| 8-bit timer/event counter mode | √ | √ |
| 16-bit timer/event counter mode | √ | |

Figure 6-4. Timer/Event Counter (Channel 0) Block Diagram

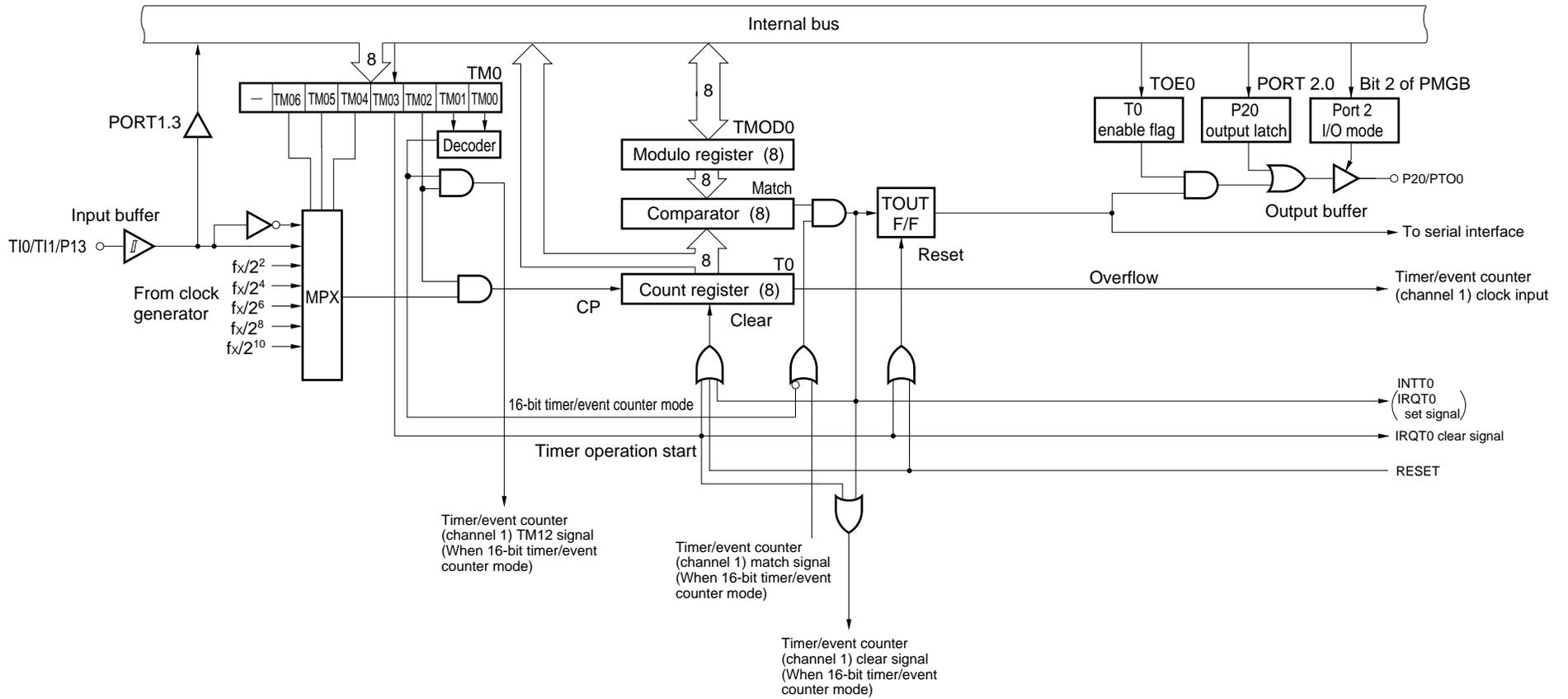
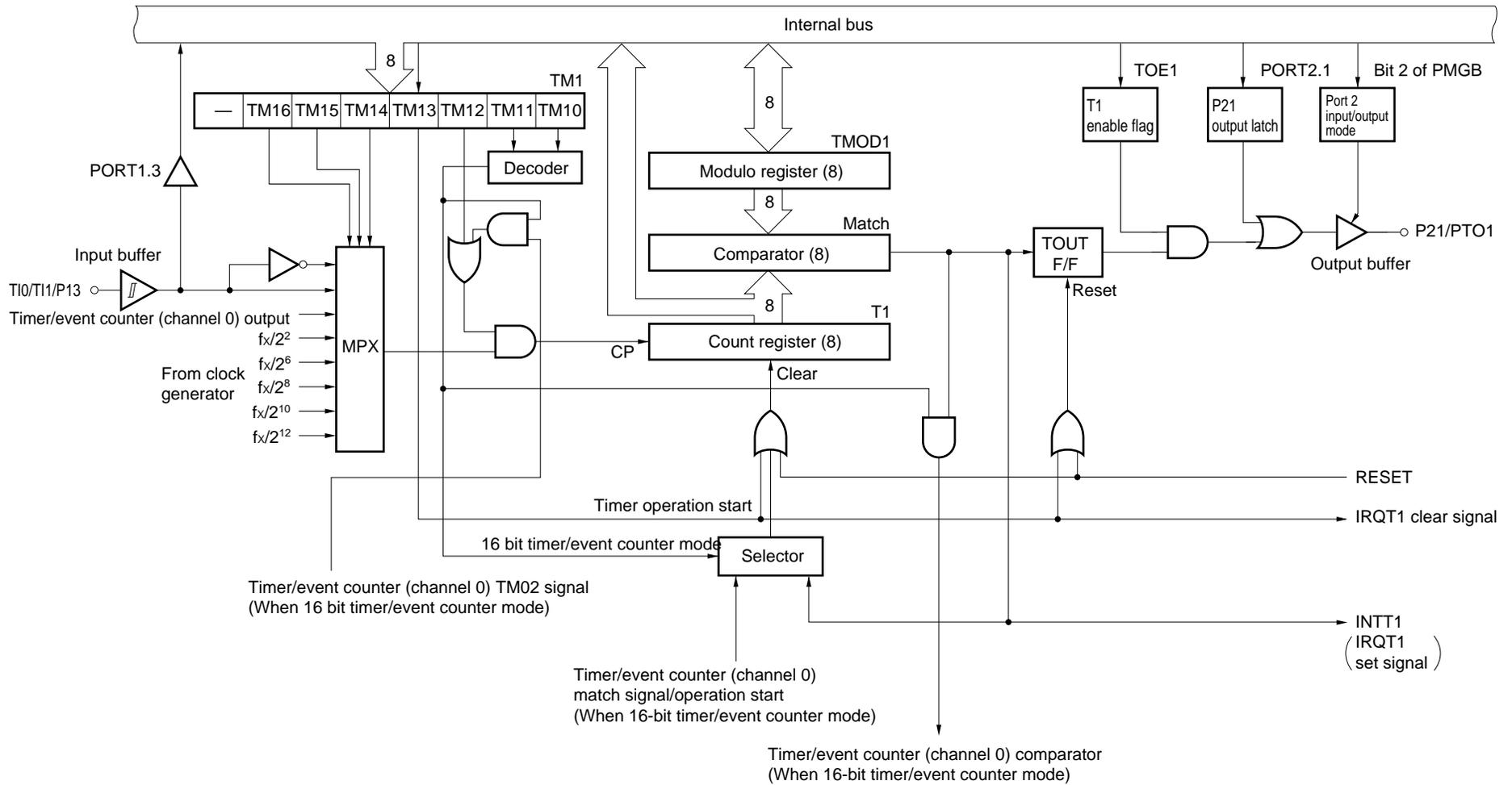


Figure 6-5. Timer/Event Counter (Channel 1) Block Diagram

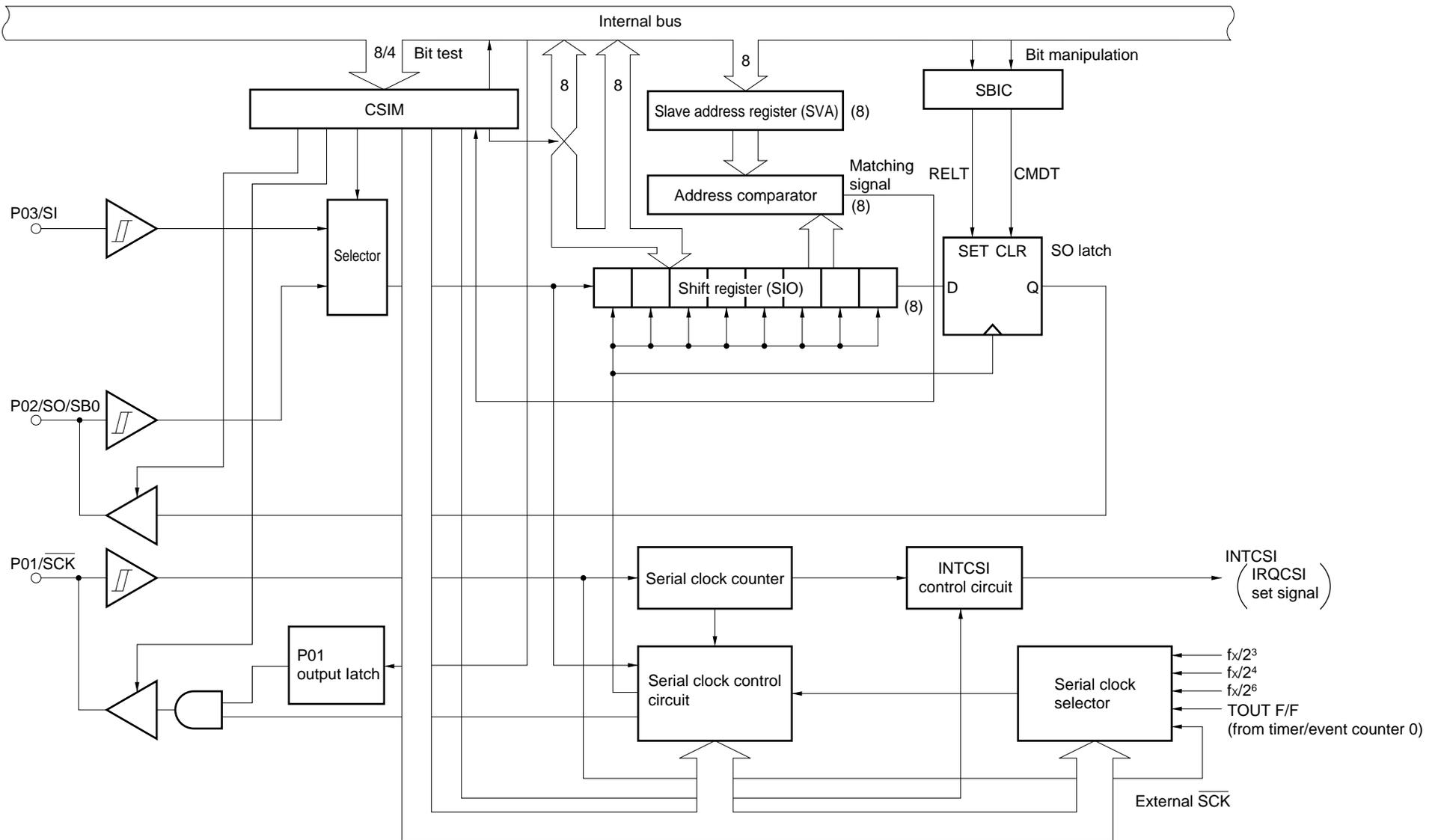


6.6 Serial Interface

The μ PD754304 incorporates the clocked 8-bit serial interface, and the following three modes are provided.

- Operation stop mode
- 3-wire serial I/O mode
- 2-wire serial I/O mode

Figure 6-6. Serial Interface Block Diagram

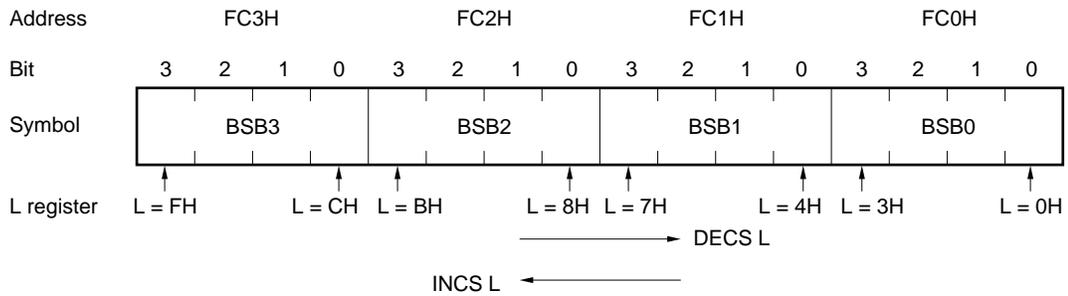


6.7 Bit Sequential Buffer 16 Bits

The bit sequential buffer (BSB) is a special data memory for bit manipulation and the bit manipulation can be easily performed by changing the address specification and bit specification in sequence, therefore it is useful when processing a long data bit-wise.

The data memory is composed of 16 bits and the pmem.@L addressing of a bit manipulation instruction is possible. The bit can be specified indirectly by the L register. In this case, processing can be done by moving the specified bit in sequence by incrementing and decrementing the L register in the program loop.

Figure 6-7. Bit Sequential Buffer Format



- Remarks 1.** In the pmem.@L addressing, the specified bit moves corresponding to the L register.
- 2.** In the pmem.@L addressing, the BSB can be manipulated regardless of MBE/MSB specification.

7. INTERRUPT FUNCTION AND TEST FUNCTION

The μ PD754304 has seven kinds of interrupt sources and one kind of test source. Two types of edge detection testable inputs are provided for INT2 of the test source.

The interrupt control circuit of the μ PD754304 has the following functions.

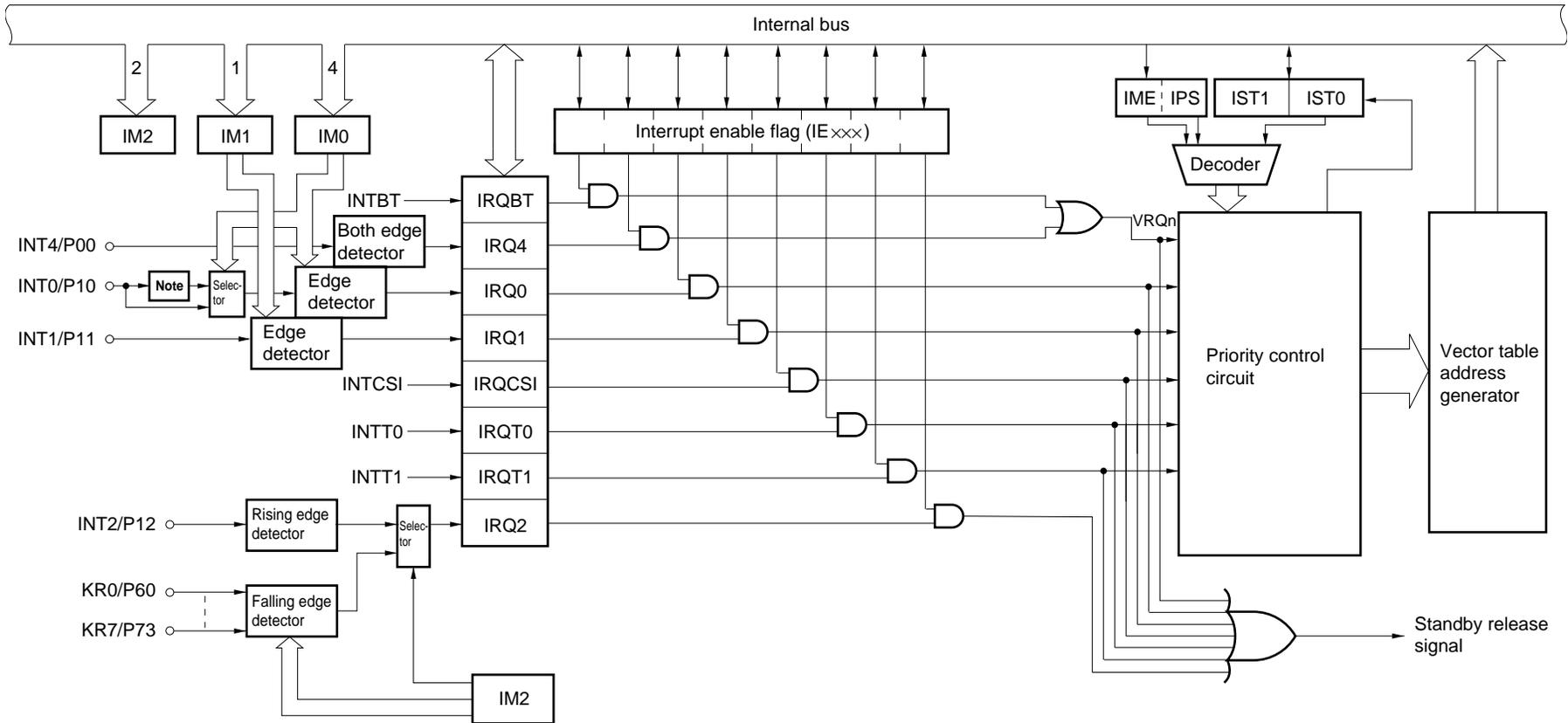
(1) Interrupt function

- Vectored interrupt function for hardware control, enabling/disabling the interrupt acceptance by the interrupt enable flag (IE_{xxx}) and interrupt master enable flag (IME).
- Can set any interrupt start address.
- Multiple interrupts wherein the order of priority can be specified by the interrupt priority select register (IPS).
- Test function of interrupt request flag (IRQ_{xxx}). An interrupt generated can be checked by software.
- Release the standby mode. A release interrupt can be selected by the interrupt enable flag.

(2) Test function

- Test request flag (IRQ_{xxx}) generation can be checked by software.
- Release the standby mode. The test source to be released can be selected by the test enable flag.

Figure 7-1. Interrupt Control Circuit Block Diagram



Note Noise eliminator (Standby release is disabled when noise eliminator is selected.)

8. STANDBY FUNCTION

In order to save dissipation power while a program is in a standby mode, two types of standby modes (STOP mode and HALT mode) are provided for the μPD754304.

Table 8-1. Operation Status in Standby Mode

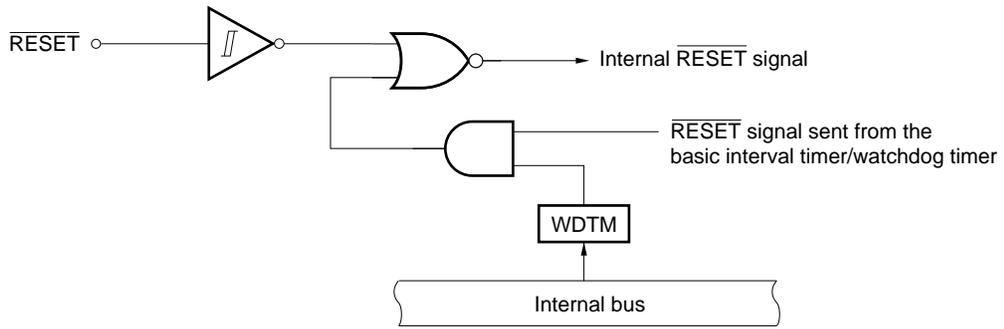
| Item \ Mode | | STOP mode | HALT mode |
|------------------|--------------------------------------|---|--|
| Set instruction | | STOP instruction | HALT instruction |
| Operation status | Clock generator | The system clock stops oscillation. | Only the CPU clock Φ halts (oscillation continues). |
| | Basic interval timer/ Watchdog timer | Operation stops. | Operable (The IRQBT is set in the reference interval). |
| | Serial interface | Operable only when an external \overline{SCK} input is selected as the serial clock. | Operable |
| | Timer/event counter | Operable only when a signal input to the T10 and T11 pins are specified as the count clock. | Operable |
| | External interrupt | The INT1, 2, and 4 are operable. Only the INT0 is not operated ^{Note} . | |
| | CPU | The operation stops. | |
| Release signal | | Interrupt request signal sent from the operable hardware enabled by the interrupt enable flag or \overline{RESET} signal input. | |

Note Operable only when the noise eliminator is not used (IM02 = 1) by bit 2 of the edge detection mode register (IM0).

9. RESET FUNCTION

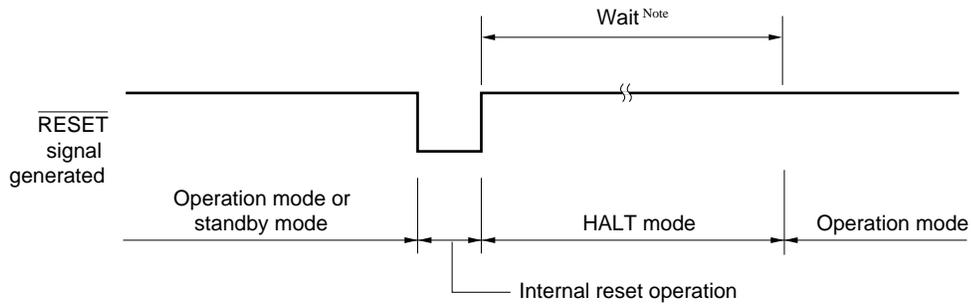
There are two reset inputs: external $\overline{\text{RESET}}$ signal and $\overline{\text{RESET}}$ signal sent from the basic interval timer/watchdog timer. When either one of the $\overline{\text{RESET}}$ signals are input, an internal $\overline{\text{RESET}}$ signal is generated. Figure 9-1 shows the circuit diagram of the above two inputs.

Figure 9-1. Configuration of Reset Function



Generation of the $\overline{\text{RESET}}$ signal initializes each hardware as listed in Table 9-1. Figure 9-2 shows the timing chart of the reset operation.

Figure 9-2. Reset Operation by $\overline{\text{RESET}}$ Signal Generation



Note The following two times can be selected by the mask option.

$2^{17}/f_x$ (21.8 ms : @ 6.0 MHz, 31.3 ms: @ 4.19 MHz)

$2^{15}/f_x$ (5.46 ms : @ 6.0 MHz, 7.81 ms: @ 4.19 MHz)

Table 9-1. Status of Each Hardware After Reset (1/2)

| Hardware | | RESET signal generation in the standby mode | RESET signal generation in operation |
|---|--|---|---|
| Program counter (PC) | μPD754302 | Sets the low-order 3 bits of program memory's address 0000H to the PC10-PC8 and the contents of address 0001H to the PC7-PC0. | Sets the low-order 3 bits of program memory's address 0000H to the PC10-PC8 and the contents of address 0001H to the PC7-PC0. |
| | μPD754304 | Sets the low-order 4 bits of program memory's address 0000H to the PC11-PC8 and the contents of address 0001H to the PC7-PC0. | Sets the low-order 4 bits of program memory's address 0000H to the PC11-PC8 and the contents of address 0001H to the PC7-PC0. |
| PSW | Carry flag (CY) | Held | Undefined |
| | Skip flag (SK0-SK2) | 0 | 0 |
| | Interrupt status flag (IST0, IST1) | 0 | 0 |
| | Bank enable flag (MBE, RBE) | Sets the bit 6 of program memory's address 0000H to the RBE and bit 7 to the MBE. | Sets the bit 6 of program memory's address 0000H to the RBE and bit 7 to the MBE. |
| Stack pointer (SP) | | Undefined | Undefined |
| Stack bank select register (SBS) | | 1000B | 1000B |
| Data memory (RAM) | | Held | Undefined |
| General-purpose register (X, A, H, L, D, E, B, C) | | Held | Undefined |
| Bank select register (MBS, RBS) | | 0, 0 | 0, 0 |
| Basic interval timer/watchdog timer | Counter (BT) | Undefined | Undefined |
| | Mode register (BTM) | 0 | 0 |
| | Watchdog timer enable flag (WDTM) | 0 | 0 |
| Timer/event counter (T0) | Counter (T0) | 0 | 0 |
| | Modulo register (TMOD0) | FFH | FFH |
| | Mode register (TM0) | 0 | 0 |
| | TOE0, TOUT F/F | 0, 0 | 0, 0 |
| Timer/event counter (T1) | Counter (T1) | 0 | 0 |
| | Modulo register (TMOD1) | FFH | FFH |
| | Mode register (TM1) | 0 | 0 |
| | TOE1, TOUT F/F | 0, 0 | 0, 0 |
| Serial interface | Shift register (SIO) | Held | Undefined |
| | Operation mode register (CSIM) | 0 | 0 |
| | SBI control register (SBIC) | 0 | 0 |
| | Slave address register (SVA) | Held | Undefined |
| Clock generator, clock output circuit | Processor clock control register (PCC) | 0 | 0 |
| | Clock output mode register (CLOM) | 0 | 0 |

Table 9-1. Status of Each Hardware After Reset (2/2)

| Hardware | | $\overline{\text{RESET}}$ signal generation in the standby mode | $\overline{\text{RESET}}$ signal generation in operation |
|------------------------------------|--|--|---|
| Interrupt function | Interrupt request flag (IRQ _{xxx}) | Reset (0) | Reset (0) |
| | Interrupt enable flag (IE _{xxx}) | 0 | 0 |
| | Interrupt priority select register (IPS) | 0 | 0 |
| | INT0, 1, 2 mode registers (IM0, IM1, IM2) | 0, 0, 0 | 0, 0, 0 |
| Digital port | Output buffer | Off | Off |
| | Output latch | Cleared (0) | Cleared (0) |
| | I/O mode registers (PMGA, B, C) | 0 | 0 |
| | Pull-up resistor setting registers (POGA, B) | 0 | 0 |
| Bit sequential buffers (BSB0-BSB3) | | Held | Undefined |

★ 10. MASK OPTION

The μ PD754304 has the following mask options:

- **Mask option of P50 through P53**

Pull-up resistors can be connected to these pins.

- (1) Specify connection of a pull-up resistor in 1-bit units.
- (2) Do not specify connection of a pull-up resistor.

- **Standby function mask option**

The wait time when the $\overline{\text{RESET}}$ signal is input can be selected.

- (1) $2^{17}/f_x$ (21.8 ms: $f_x = 6.0$ MHz, 31.3 ms: $f_x = 4.19$ MHz)
- (2) $2^{15}/f_x$ (5.46 ms: $f_x = 6.0$ MHz, 7.81 ms: $f_x = 4.19$ MHz)

11. INSTRUCTION SETS

(1) Expression formats and description methods of operands

The operand is described in the operand column of each instruction in accordance with the description method for the operand expression format of the instruction. For details, refer to **RA75X ASSEMBLER PACKAGE USERS' MANUAL—LANGUAGE (EEU-1363)**. If there are several elements, one of them is selected. Capital letters and the + and – symbols are key words and are described as they are.

For immediate data, appropriate numbers and labels are described.

Instead of the labels such as mem, fmem, pmem, and bit, the symbols of the register flags can be described. However, there are restrictions in the labels that can be described for fmem and pmem.

For details, refer to the **μPD754304 USER'S MANUAL (U10123E)**.

| Representation format | Description method |
|-----------------------|---|
| reg | X, A, B, C, D, E, H, L |
| reg1 | X, B, C, D, E, H, L |
| rp | XA, BC, DE, HL |
| rp1 | BC, DE, HL |
| rp2 | BC, DE |
| rp' | XA, BC, DE, HL, XA', BC', DE', HL' |
| rp'1 | BC, DE, HL, XA', BC', DE', HL' |
| rpa | HL, HL+, HL–, DE, DL |
| rpa1 | DE, DL |
| n4 | 4-bit immediate data or label |
| n8 | 8-bit immediate data or label |
| mem | 8-bit immediate data or label ^{Note} |
| bit | 2-bit immediate data or label |
| fmem | FB0H-FBFH, FF0H-FFFH immediate data or label |
| pmem | FC0H-FFFH immediate data or label |
| addr | 0000H-07FFH immediate data or label (μPD754302) |
| addr1 | 0000H-0FFFH immediate data or label (μPD754304) |
| caddr | 0000H-07FFH immediate data or label (μPD754302) |
| faddr | 0000H-0FFFH immediate data or label (μPD754304) |
| taddr | 12-bit immediate data or label |
| faddr | 11-bit immediate data or label |
| taddr | 20H-7FH immediate data (where bit 0 = 0) or label |
| PORTn | PORT0-PORT3, PORT5-PORT8 |
| IExxx | IEBT, IET0, IET1, IE0-IE2, IE4, IECSI |
| RBn | RB0-RB3 |
| MBn | MB0, MB15 |

Note mem can be only used for even address in 8-bit data processing.

(2) Legend in explanation of operation

| | |
|-------------------|---------------------------------------|
| A | : A register; 4-bit accumulator |
| B | : B register |
| C | : C register |
| D | : D register |
| E | : E register |
| H | : H register |
| L | : L register |
| X | : X register |
| XA | : XA register pair; 8-bit accumulator |
| BC | : BC register pair |
| DE | : DE register pair |
| HL | : HL register pair |
| XA' | : XA' expanded register pair |
| BC' | : BC' expanded register pair |
| DE' | : DE' expanded register pair |
| HL' | : HL' expanded register pair |
| PC | : Program counter |
| SP | : Stack pointer |
| CY | : Carry flag; bit accumulator |
| PSW | : Program status word |
| MBE | : Memory bank enable flag |
| RBE | : Register bank enable flag |
| PORT _n | : Port n (n = 0-3, 5-8) |
| IME | : Interrupt master enable flag |
| IPS | : Interrupt priority select register |
| IE _{xxx} | : Interrupt enable flag |
| RBS | : Register bank select register |
| MBS | : Memory bank select register |
| PCC | : Processor clock control register |
| . | : Separation between address and bit |
| (xx) | : The contents addressed by xx |
| xxH | : Hexadecimal data |

(3) Explanation of symbols under addressing area column

| | | | |
|-----|---|--|---------------------------|
| *1 | MB = MBE•MBS (MBS = 0, 15) | | Data memory addressing |
| *2 | MB = 0 | | |
| *3 | MBE = 0 : MB = 0 (000H-07FH) MB = 15 (F80H-FFFH) MBE = 1 : MB = MBS (MBS = 0, 15) | | |
| *4 | MB = 15, fmem = FB0H-FBFH, FF0H-FFFH | | |
| *5 | MB = 15, pmem = FC0H-FFFH | | |
| *6 | μPD754302 | addr = 0000H-07FFH | Program memory addressing |
| | μPD754304 | addr = 0000H-0FFFH | |
| *7 | addr = (Current PC) – 15 to (Current PC) – 1 (Current PC) + 2 to (Current PC) + 16 | | |
| | addr1 = (Current PC) – 15 to (Current PC) – 1 (Current PC) + 2 to (Current PC) + 16 | | |
| *8 | μPD754302 | caddr = 0000H-07FFH | |
| | μPD754304 | caddr = 0000H-0FFFH (PC ₁₂ = 0) | |
| *9 | faddr = 0000H-07FFH | | |
| *10 | taddr = 0020H-007FH | | |
| *11 | μPD754302 | addr1 = 0000H-07FFH | |
| | μPD754304 | addr1 = 0000H-0FFFH | |

- Remarks**
1. MB indicates memory bank that can be accessed.
 2. In *2, MB = 0 independently of how MBE and MBS are set.
 3. In *4 and *5, MB = 15 independently of how MBE and MBS are set.
 4. *6 to *11 indicate the areas that can be addressed.

(4) Explanation of number of machine cycles column

S denotes the number of machine cycles required by skip operation when a skip instruction is executed. The value of S varies as follows.

- When no skip is made: S = 0
- When the skipped instruction is a 1- or 2-byte instruction: S = 1
- When the skipped instruction is a 3-byte instruction ^{Note}: S = 2

Note 3-byte instruction: BR !addr, BRA !addr1, CALL !addr or CALLA !addr1 instruction

Caution The GETI instruction is skipped in one machine cycle.

One machine cycle is equal to one cycle of CPU clock (= tcy); time can be selected from among four types by setting PCC.

| Instruction group | Mnemonic | Operand | Number of bytes | Number of machine cycles | Operation | Addressing area | Skip condition | |
|-------------------|-----------------|-----------|-----------------|--------------------------|--|--|-----------------|--------|
| Transfer | MOV | A, #n4 | 1 | 1 | $A \leftarrow n4$ | | String effect A | |
| | | reg1, #n4 | 2 | 2 | $reg1 \leftarrow n4$ | | | |
| | | XA, #n8 | 2 | 2 | $XA \leftarrow n8$ | | String effect A | |
| | | HL, #n8 | 2 | 2 | $HL \leftarrow n8$ | | String effect B | |
| | | rp2, #n8 | 2 | 2 | $rp2 \leftarrow n8$ | | | |
| | | A, @HL | 1 | 1 | $A \leftarrow (HL)$ | | *1 | |
| | | A, @HL+ | 1 | 2+S | $A \leftarrow (HL)$, then $L \leftarrow L+1$ | | *1 | L = 0 |
| | | A, @HL- | 1 | 2+S | $A \leftarrow (HL)$, then $L \leftarrow L-1$ | | *1 | L = FH |
| | | A, @rpa | 1 | 1 | $A \leftarrow (rpa)$ | | *2 | |
| | | XA, @HL | 2 | 2 | $XA \leftarrow (HL)$ | | *1 | |
| | | @HL, A | 1 | 1 | $(HL) \leftarrow A$ | | *1 | |
| | | @HL, XA | 2 | 2 | $(HL) \leftarrow XA$ | | *1 | |
| | | A, mem | 2 | 2 | $A \leftarrow (mem)$ | | *3 | |
| | | XA, mem | 2 | 2 | $XA \leftarrow (mem)$ | | *3 | |
| | | mem, A | 2 | 2 | $(mem) \leftarrow A$ | | *3 | |
| | | mem, XA | 2 | 2 | $(mem) \leftarrow XA$ | | *3 | |
| | | A, reg1 | 2 | 2 | $A \leftarrow reg1$ | | | |
| | | XA, rp' | 2 | 2 | $XA \leftarrow rp'$ | | | |
| | | reg1, A | 2 | 2 | $reg1 \leftarrow A$ | | | |
| | | rp'1, XA | 2 | 2 | $rp'1 \leftarrow XA$ | | | |
| | XCH | A, @HL | 1 | 1 | $A \leftrightarrow (HL)$ | | *1 | |
| | | A, @HL+ | 1 | 2+S | $A \leftrightarrow (HL)$, then $L \leftarrow L+1$ | | *1 | L = 0 |
| | | A, @HL- | 1 | 2+S | $A \leftrightarrow (HL)$, then $L \leftarrow L-1$ | | *1 | L = FH |
| | | A, @rpa | 1 | 1 | $A \leftrightarrow (rpa)$ | | *2 | |
| | | XA, @HL | 2 | 2 | $XA \leftrightarrow (HL)$ | | *1 | |
| | | A, mem | 2 | 2 | $A \leftrightarrow (mem)$ | | *3 | |
| | | XA, mem | 2 | 2 | $XA \leftrightarrow (mem)$ | | *3 | |
| | | A, reg1 | 1 | 1 | $A \leftrightarrow reg1$ | | | |
| | Table reference | MOVT | XA, @PCDE | 1 | 3 | <ul style="list-style-type: none"> ● μPD754302 $XA \leftarrow (PC_{10-8}+DE)_{ROM}$ | | |
| | | | | | | <ul style="list-style-type: none"> ● μPD754304 $XA \leftarrow (PC_{11-8}+DE)_{ROM}$ | | |
| | | | XA, @PCXA | 1 | 3 | <ul style="list-style-type: none"> ● μPD754302 $XA \leftarrow (PC_{10-8}+XA)_{ROM}$ | | |
| | | | | | | <ul style="list-style-type: none"> ● μPD754304 $XA \leftarrow (PC_{11-8}+XA)_{ROM}$ | | |
| | | XA, @BCDE | 1 | 3 | $XA \leftarrow (BCDE)_{ROM}$ <small>Note</small> | | *6 | |
| | | XA, @BCXA | 1 | 3 | $XA \leftarrow (BCXA)_{ROM}$ <small>Note</small> | | *6 | |

Note To use the μPD754302, clear the most significant bit of the register C and register B to “0”. To use the μPD754304, clear the register B to “0”.

| Instruction group | Mnemonic | Operand | Number of bytes | Number of machine cycles | Operation | Addressing area | Skip condition |
|--------------------------|----------|----------------|-----------------|----------------------------------|--|-----------------|----------------|
| Bit transfer | MOV1 | CY, fmem.bit | 2 | 2 | $CY \leftarrow (fmem.bit)$ | *4 | |
| | | CY, pmem.@L | 2 | 2 | $CY \leftarrow (pmem_{7-2+L_{3-2}.bit(L_{1-0}))}$ | *5 | |
| | | CY, @H+mem.bit | 2 | 2 | $CY \leftarrow (H+mem_{3-0}.bit)$ | *1 | |
| | | fmem.bit, CY | 2 | 2 | $(fmem.bit) \leftarrow CY$ | *4 | |
| | | pmem.@L, CY | 2 | 2 | $(pmem_{7-2+L_{3-2}.bit(L_{1-0}))} \leftarrow CY$ | *5 | |
| | | @H+mem.bit, CY | 2 | 2 | $(H+mem_{3-0}.bit) \leftarrow CY$ | *1 | |
| Operation | ADDS | A, #n4 | 1 | 1+S | $A \leftarrow A+n4$ | | carry |
| | | XA, #n8 | 2 | 2+S | $XA \leftarrow XA+n8$ | | carry |
| | | A, @HL | 1 | 1+S | $A \leftarrow A+(HL)$ | *1 | carry |
| | | XA, rp' | 2 | 2+S | $XA \leftarrow XA+rp'$ | | carry |
| | | rp'1, XA | 2 | 2+S | $rp'1 \leftarrow rp'1+XA$ | | carry |
| | ADDC | A, @HL | 1 | 1 | $A, CY \leftarrow A+(HL)+CY$ | *1 | |
| | | XA, rp' | 2 | 2 | $XA, CY \leftarrow XA+rp'+CY$ | | |
| | | rp'1, XA | 2 | 2 | $rp'1, CY \leftarrow rp'1+XA+CY$ | | |
| | SUBS | A, @HL | 1 | 1+S | $A \leftarrow A-(HL)$ | *1 | borrow |
| | | XA, rp' | 2 | 2+S | $XA \leftarrow XA-rp'$ | | borrow |
| | | rp'1, XA | 2 | 2+S | $rp'1 \leftarrow rp'1-XA$ | | borrow |
| | SUBC | A, @HL | 1 | 1 | $A, CY \leftarrow A-(HL)-CY$ | *1 | |
| | | XA, rp' | 2 | 2 | $XA, CY \leftarrow XA-rp'-CY$ | | |
| | | rp'1, XA | 2 | 2 | $rp'1, CY \leftarrow rp'1-XA-CY$ | | |
| | AND | A, #n4 | 2 | 2 | $A \leftarrow A \wedge n4$ | | |
| | | A, @HL | 1 | 1 | $A \leftarrow A \wedge (HL)$ | *1 | |
| | | XA, rp' | 2 | 2 | $XA \leftarrow XA \wedge rp'$ | | |
| | | rp'1, XA | 2 | 2 | $rp'1 \leftarrow rp'1 \wedge XA$ | | |
| | OR | A, #n4 | 2 | 2 | $A \leftarrow A \vee n4$ | | |
| | | A, @HL | 1 | 1 | $A \leftarrow A \vee (HL)$ | *1 | |
| | | XA, rp' | 2 | 2 | $XA \leftarrow XA \vee rp'$ | | |
| | | rp'1, XA | 2 | 2 | $rp'1 \leftarrow rp'1 \vee XA$ | | |
| | XOR | A, #n4 | 2 | 2 | $A \leftarrow A \oplus n4$ | | |
| | | A, @HL | 1 | 1 | $A \leftarrow A \oplus (HL)$ | *1 | |
| XA, rp' | | 2 | 2 | $XA \leftarrow XA \oplus rp'$ | | | |
| rp'1, XA | | 2 | 2 | $rp'1 \leftarrow rp'1 \oplus XA$ | | | |
| Accumulator manipulation | RORC | A | 1 | 1 | $CY \leftarrow A_0, A_3 \leftarrow CY, A_{n-1} \leftarrow A_n$ | | |
| | NOT | A | 2 | 2 | $A \leftarrow \bar{A}$ | | |
| Increment and decrement | INCS | reg | 1 | 1+S | $reg \leftarrow reg+1$ | | reg=0 |
| | | rp1 | 1 | 1+S | $rp1 \leftarrow rp1+1$ | | rp1=00H |
| | | @HL | 2 | 2+S | $(HL) \leftarrow (HL)+1$ | *1 | (HL)=0 |
| | | mem | 2 | 2+S | $(mem) \leftarrow (mem)+1$ | *3 | (mem)=0 |
| | DECS | reg | 1 | 1+S | $reg \leftarrow reg-1$ | | reg=FFH |
| | | rp' | 2 | 2+S | $rp' \leftarrow rp'-1$ | | rp'=FFH |

| Instruction group | Mnemonic | Operand | Number of bytes | Number of machine cycles | Operation | Addressing area | Skip condition |
|-------------------------|----------|----------------|-----------------|--------------------------|---|-----------------|------------------|
| Comparison | SKE | reg, #n4 | 2 | 2+S | Skip if reg = n4 | | reg=n4 |
| | | @HL, #n4 | 2 | 2+S | Skip if (HL) = n4 | *1 | (HL) = n4 |
| | | A, @HL | 1 | 1+S | Skip if A = (HL) | *1 | A = (HL) |
| | | XA, @HL | 2 | 2+S | Skip if XA = (HL) | *1 | XA = (HL) |
| | | A, reg | 2 | 2+S | Skip if A = reg | | A=reg |
| | | XA, rp' | 2 | 2+S | Skip if XA = rp' | | XA=rp' |
| Carry flag manipulation | SET1 | CY | 1 | 1 | $CY \leftarrow 1$ | | |
| | CLR1 | CY | 1 | 1 | $CY \leftarrow 0$ | | |
| | SKT | CY | 1 | 1+S | Skip if $CY = 1$ | | CY=1 |
| | NOT1 | CY | 1 | 1 | $CY \leftarrow \overline{CY}$ | | |
| Memory bit manipulation | SET1 | mem.bit | 2 | 2 | $(mem.bit) \leftarrow 1$ | *3 | |
| | | fmem.bit | 2 | 2 | $(fmem.bit) \leftarrow 1$ | *4 | |
| | | pmem.@L | 2 | 2 | $(pmem_{7-2+L_{3-2}.bit(L_{1-0}))} \leftarrow 1$ | *5 | |
| | | @H+mem.bit | 2 | 2 | $(H+mem_{3-0}.bit) \leftarrow 1$ | *1 | |
| | CLR1 | mem.bit | 2 | 2 | $(mem.bit) \leftarrow 0$ | *3 | |
| | | fmem.bit | 2 | 2 | $(fmem.bit) \leftarrow 0$ | *4 | |
| | | pmem.@L | 2 | 2 | $(pmem_{7-2+L_{3-2}.bit(L_{1-0}))} \leftarrow 0$ | *5 | |
| | | @H+mem.bit | 2 | 2 | $(H+mem_{3-0}.bit) \leftarrow 0$ | *1 | |
| | SKT | mem.bit | 2 | 2+S | Skip if $(mem.bit)=1$ | *3 | $(mem.bit)=1$ |
| | | fmem.bit | 2 | 2+S | Skip if $(fmem.bit)=1$ | *4 | $(fmem.bit)=1$ |
| | | pmem.@L | 2 | 2+S | Skip if $(pmem_{7-2+L_{3-2}.bit(L_{1-0}))}=1$ | *5 | $(pmem.@L)=1$ |
| | | @H+mem.bit | 2 | 2+S | Skip if $(H+mem_{3-0}.bit)=1$ | *1 | $(@H+mem.bit)=1$ |
| | SKF | mem.bit | 2 | 2+S | Skip if $(mem.bit)=0$ | *3 | $(mem.bit)=0$ |
| | | fmem.bit | 2 | 2+S | Skip if $(fmem.bit)=0$ | *4 | $(fmem.bit)=0$ |
| | | pmem.@L | 2 | 2+S | Skip if $(pmem_{7-2+L_{3-2}.bit(L_{1-0}))}=0$ | *5 | $(pmem.@L)=0$ |
| | | @H+mem.bit | 2 | 2+S | Skip if $(H+mem_{3-0}.bit)=0$ | *1 | $(@H+mem.bit)=0$ |
| | SKTCLR | fmem.bit | 2 | 2+S | Skip if $(fmem.bit)=1$ and clear | *4 | $(fmem.bit)=1$ |
| | | pmem.@L | 2 | 2+S | Skip if $(pmem_{7-2+L_{3-2}.bit(L_{1-0}))}=1$ and clear | *5 | $(pmem.@L)=1$ |
| | | @H+mem.bit | 2 | 2+S | Skip if $(H+mem_{3-0}.bit)=1$ and clear | *1 | $(@H+mem.bit)=1$ |
| | AND1 | CY, fmem.bit | 2 | 2 | $CY \leftarrow CY \wedge (fmem.bit)$ | *4 | |
| | | CY, pmem.@L | 2 | 2 | $CY \leftarrow CY \wedge (pmem_{7-2+L_{3-2}.bit(L_{1-0}))}$ | *5 | |
| | | CY, @H+mem.bit | 2 | 2 | $CY \leftarrow CY \wedge (H+mem_{3-0}.bit)$ | *1 | |
| | OR1 | CY, fmem.bit | 2 | 2 | $CY \leftarrow CY \vee (fmem.bit)$ | *4 | |
| | | CY, pmem.@L | 2 | 2 | $CY \leftarrow CY \vee (pmem_{7-2+L_{3-2}.bit(L_{1-0}))}$ | *5 | |
| | | CY, @H+mem.bit | 2 | 2 | $CY \leftarrow CY \vee (H+mem_{3-0}.bit)$ | *1 | |
| | XOR1 | CY, fmem.bit | 2 | 2 | $CY \leftarrow CY \vee (fmem.bit)$ | *4 | |
| | | CY, pmem.@L | 2 | 2 | $CY \leftarrow CY \vee (pmem_{7-2+L_{3-2}.bit(L_{1-0}))}$ | *5 | |
| | | CY, @H+mem.bit | 2 | 2 | $CY \leftarrow CY \vee (H+mem_{3-0}.bit)$ | *1 | |

| Instruction group | Mnemonic | Operand | Number of bytes | Number of machine cycles | Operation | Addressing area | Skip condition |
|-------------------|--------------------|---------|---|--------------------------|---|-----------------|----------------|
| Branch | BR ^{Note} | addr | - | - | <ul style="list-style-type: none"> ● μPD754302 PC₁₀₋₀ ← addr (Select appropriate instruction from among BR !addr, BRCB !caddr and BR \$addr according to the assembler being used.) | *6 | |
| | | | | | <ul style="list-style-type: none"> ● μPD754304 PC₁₁₋₀ ← addr (Select appropriate instruction from among BR !addr, BRCB !caddr and BR \$addr according to the assembler being used.) | | |
| | | addr1 | - | - | <ul style="list-style-type: none"> ● μPD754302 PC₁₀₋₀ ← addr (Select appropriate instruction from among BR !addr, BRA !addr1, BRCB !caddr and BR \$addr1 according to the assembler being used.) | *11 | |
| | | | | | <ul style="list-style-type: none"> ● μPD754304 PC₁₁₋₀ ← addr1 (Select appropriate instruction from among BR !addr, BRA !addr1, BRCB !caddr and BR \$addr1 according to the assembler being used.) | | |
| | | !addr | 3 | 3 | <ul style="list-style-type: none"> ● μPD754302 PC₁₀₋₀ ← addr | *6 | |
| | | | | | <ul style="list-style-type: none"> ● μPD754304 PC₁₁₋₀ ← addr | | |
| | | \$addr | 1 | 2 | <ul style="list-style-type: none"> ● μPD754302 PC₁₀₋₀ ← addr | *7 | |
| | | | | | <ul style="list-style-type: none"> ● μPD754304 PC₁₁₋₀ ← addr | | |
| | | \$addr1 | 1 | 2 | <ul style="list-style-type: none"> ● μPD754302 PC₁₀₋₀ ← addr1 | | |
| | | | | | <ul style="list-style-type: none"> ● μPD754304 PC₁₁₋₀ ← addr1 | | |
| PCDE | 2 | 3 | <ul style="list-style-type: none"> ● μPD754302 PC₁₀₋₀ ← PC₁₀₋₈+DE | | | | |
| | | | <ul style="list-style-type: none"> ● μPD754304 PC₁₁₋₀ ← PC₁₁₋₈+DE | | | | |
| PCXA | 2 | 3 | <ul style="list-style-type: none"> ● μPD754302 PC₁₀₋₀ ← PC₁₀₋₈+XA | | | | |
| | | | <ul style="list-style-type: none"> ● μPD754304 PC₁₁₋₀ ← PC₁₁₋₈+XA | | | | |

Note The above operations in the double boxes can be performed only in the Mk II mode.

| Instruction group | Mnemonic | Operand | Number of bytes | Number of machine cycles | Operation | Addressing area | Skip condition | |
|--------------------------|--------------------|------------------|-----------------|---|---|---|----------------|--|
| Branch | BR | BCDE | 2 | 3 | <ul style="list-style-type: none"> ● μPD754302 PC₁₀₋₀ ← BCDE <i>Note1</i> | *6 | | |
| | | | | | <ul style="list-style-type: none"> ● μPD754304 PC₁₁₋₀ ← BCDE <i>Note2</i> | | | |
| | | BCXA | 2 | 3 | <ul style="list-style-type: none"> ● μPD754302 PC₁₀₋₀ ← BCXA <i>Note1</i> | *6 | | |
| | | | | | <ul style="list-style-type: none"> ● μPD754304 PC₁₁₋₀ ← BCXA <i>Note2</i> | | | |
| | | BRA <i>Note3</i> | laddr1 | 3 | 3 | <ul style="list-style-type: none"> ● μPD754302 PC₁₀₋₀ ← addr1 | *11 | |
| | | | | | <ul style="list-style-type: none"> ● μPD754304 PC₁₁₋₀ ← addr1 | | | |
| | BRCB | lcaddr | 2 | 2 | <ul style="list-style-type: none"> ● μPD754302 PC₁₀₋₀ ← caddr₁₀₋₀ | *8 | | |
| | | | | <ul style="list-style-type: none"> ● μPD754304 PC₁₁₋₀ ← caddr₁₁₋₀ | | | | |
| Subroutine stack control | CALLA <i>Note3</i> | laddr1 | 3 | 3 | <ul style="list-style-type: none"> ● μPD754302 (SP-2) ← x, x, MBE, RBE (SP-6) (SP-3) (SP-4) ← PC₁₀₋₀ (SP-5) ← 0, 0, 0, 0 PC₁₀₋₀ ← addr1, SP ← SP-6 | *11 | | |
| | | | | <ul style="list-style-type: none"> ● μPD754304 (SP-2) ← x, x, MBE, RBE (SP-6) (SP-3) (SP-4) ← PC₁₁₋₀ (SP-5) ← 0, 0, 0, 0 PC₁₁₋₀ ← addr1, SP ← SP-6 | | | | |
| | CALL <i>Note3</i> | laddr | 3 | 3 | <ul style="list-style-type: none"> ● μPD754302 (SP-3) ← MBE, RBE, 0, 0 (SP-4) (SP-1) (SP-2) ← PC₁₀₋₀ PC₁₀₋₀ ← addr, SP ← SP-4 | *6 | | |
| | | | | | <ul style="list-style-type: none"> ● μPD754304 (SP-3) ← MBE, RBE, 0, 0 (SP-4) (SP-1) (SP-2) ← PC₁₁₋₀ PC₁₁₋₀ ← addr, SP ← SP-4 | | | |
| | | | | 4 | <ul style="list-style-type: none"> ● μPD754302 (SP-2) ← x, x, MBE, RBE (SP-6) (SP-3) (SP-4) ← PC₁₀₋₀ (SP-5) ← 0, 0, 0, 0 PC₁₀₋₀ ← addr, SP ← SP-6 | | | |
| | | | | | <ul style="list-style-type: none"> ● μPD754304 (SP-2) ← x, x, MBE, RBE (SP-6) (SP-3) (SP-4) ← PC₁₁₋₀ (SP-5) ← 0, 0, 0, 0 PC₁₁₋₀ ← addr, SP ← SP-6 | | | |

- Notes**
1. "0" must be set to the most significant bit of the register C and register B.
 2. "0" must be set to register B.
 3. The above operations in the double boxes can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.

| Instruction group | Mnemonic | Operand | Number of bytes | Number of machine cycles | Operation | Addressing area | Skip condition |
|--------------------------|-----------------------|---------|-----------------|--|---|-----------------|----------------|
| Subroutine stack control | CALLF ^{Note} | !faddr | 2 | 2 | <ul style="list-style-type: none"> ● μPD754302 (SP-3) ← MBE, RBE, 0, 0 (SP-4) (SP-1) (SP-2) ← PC₁₀₋₀ PC₁₀₋₀ ← faddr, SP ← SP-4 ● μPD754304 (SP-3) ← MBE, RBE, 0, 0 (SP-4) (SP-1) (SP-2) ← PC₁₁₋₀ PC₁₁₋₀ ← 0+faddr, SP ← SP-4 | *9 | |
| | | | | 3 | <ul style="list-style-type: none"> ● μPD754302 (SP-2) ← x, x, MBE, RBE (SP-6) (SP-3) (SP-4) ← PC₁₀₋₀ (SP-5) ← 0, 0, 0, 0 PC₁₀₋₀ ← faddr, SP ← SP-6 ● μPD754304 (SP-2) ← x, x, MBE, RBE (SP-6) (SP-3) (SP-4) ← PC₁₁₋₀ (SP-5) ← 0, 0, 0, 0 PC₁₁₋₀ ← 0+faddr, SP ← SP-6 | | |
| | | | 1 | 3 | <ul style="list-style-type: none"> ● μPD754302 PC₁₀₋₀ ← (SP) (SP+3) (SP+2) MBE, RBE, 0, 0 ← (SP+1), SP ← SP+4 ● μPD754304 PC₁₁₋₀ ← (SP) (SP+3) (SP+2) MBE, RBE, 0, 0 ← (SP+1), SP ← SP+4 ● μPD754302 x, x, MBE, RBE ← (SP+4) 0, 0, 0, 0, ← (SP+1) PC₁₀₋₀ ← (SP) (SP+3) (SP+2), SP ← SP+6 ● μPD754304 x, x, MBE, RBE ← (SP+4) 0, 0, 0, 0 ← (SP+1) PC₁₀₋₀ ← (SP) (SP+3) (SP+2), SP ← SP+6 | | |
| RETS ^{Note} | | 1 | 3+S | <ul style="list-style-type: none"> ● μPD754302 MBE, RBE, 0, 0 ← (SP+1) PC₁₀₋₀ ← (SP) (SP+3) (SP+2) SP ← SP+4 then skip unconditionally ● μPD754304 MBE, RBE, 0, 0 ← (SP+1) PC₁₁₋₀ ← (SP) (SP+3) (SP+2) SP ← SP+4 then skip unconditionally | | Unconditional | |

Note The above operations in the double boxes can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.

| Instruction group | Mnemonic | Operand | Number of bytes | Number of machine cycles | Operation | Addressing area | Skip condition | |
|--------------------------|-----------------------|------------------------|-----------------|--------------------------|---|---------------------------------------|----------------|--|
| Subroutine stack control | RETS ^{Note1} | | 1 | 3+S | <div style="border: 1px solid black; padding: 2px;"> <p>● μPD754302 0, 0, 0, 0 ← (SP+1) PC₁₀₋₀ ← (SP) (SP+3) (SP+2) X, X, MBE, RBE ← (SP+4) SP ← SP+6 then skip unconditionally</p> </div> <div style="border: 1px solid black; padding: 2px;"> <p>● μPD754304 0, 0, 0, 0 ← (SP+1) PC₁₁₋₀ ← (SP) (SP+3) (SP+2) X, X, MBE, RBE ← (SP+4) SP ← SP+6 then skip unconditionally</p> </div> | | Unconditional | |
| | RETI ^{Note1} | | 1 | 3 | <div style="border: 1px solid black; padding: 2px;"> <p>● μPD754302 MBE, RBE, 0, 0 ← (SP+1) PC₁₀₋₀ ← (SP) (SP+3) (SP+2) PSW ← (SP+4) (SP+5), SP ← SP+6</p> </div> <div style="border: 1px solid black; padding: 2px;"> <p>● μPD754304 MBE, RBE, 0, 0 ← (SP+1) PC₁₁₋₀ ← (SP) (SP+3) (SP+2) PSW ← (SP+4) (SP+5), SP ← SP+6</p> </div> <div style="border: 1px solid black; padding: 2px;"> <p>● μPD754302 0, 0, 0, 0 ← (SP+1) PC₁₀₋₀ ← (SP) (SP+3) (SP+2) PSW ← (SP+4) (SP+5), SP ← SP+6</p> </div> <div style="border: 1px solid black; padding: 2px;"> <p>● μPD754304 0, 0, 0, 0 ← (SP+1) PC₁₁₋₀ ← (SP) (SP+3) (SP+2) PSW ← (SP+4) (SP+5), SP ← SP+6</p> </div> | | | |
| | PUSH | rp | | 1 | 1 | (SP-1)(SP-2) ← rp, SP ← SP-2 | | |
| | | BS | | 2 | 2 | (SP-1) ← MBS, (SP-2) ← RBS, SP ← SP-2 | | |
| | POP | rp | | 1 | 1 | rp ← (SP+1) (SP), SP ← SP+2 | | |
| | | BS | | 2 | 2 | MBS ← (SP+1), RBS ← (SP), SP ← SP+2 | | |
| Interrupt control | EI | | 2 | 2 | IME (IPS.3) ← 1 | | | |
| | | IE _{xxx} | 2 | 2 | IE _{xxx} ← 1 | | | |
| | DI | | 2 | 2 | IME (IPS.3) ← 0 | | | |
| | | IE _{xxx} | 2 | 2 | IE _{xxx} ← 0 | | | |
| Input/output | IN ^{Note2} | A, PORT _n | 2 | 2 | A ← PORT _n (n = 0-3, 5-8) | | | |
| | | XA, PORT _n | 2 | 2 | XA ← PORT _{n+1} , PORT _n (n = 6) | | | |
| | OUT ^{Note2} | PORT _n , A | 2 | 2 | PORT _n ← A (n = 2, 3, 5-8) | | | |
| | | PORT _n , XA | 2 | 2 | PORT _{n+1} , PORT _n ← XA (n = 6) | | | |

- Notes**
- The above operations in the double boxes can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.
 - While the IN instruction and OUT instruction are being executed, the MBE must be set to 0 or 1 and MBS must be set to 15.

| Instruction group | Mnemonic | Operand | Number of bytes | Number of machine cycles | Operation | Addressing area | Skip condition |
|---|----------------------------|---------|---|---|---|-----------------|--|
| CPU control | HALT | | 2 | 2 | Set HALT Mode (PCC.2 ← 1) | | |
| | STOP | | 2 | 2 | Set STOP Mode (PCC.3 ← 1) | | |
| | NOP | | 1 | 1 | No Operation | | |
| Special | SEL | RBn | 2 | 2 | RBS ← n (n = 0-3) | | |
| | | MBn | 2 | 2 | MBS ← n (n = 0, 15) | | |
| | GETI ^{Notes 1, 2} | taddr | 1 | 3 | <ul style="list-style-type: none"> • μPD754302 • When TBR instruction PC₁₀₋₀ ← (taddr)₂₋₀ + (taddr+1) | *10 | |
| | | | | | <ul style="list-style-type: none"> • When TCALL instruction (SP-4) (SP-1) (SP-2) ← PC₁₀₋₀ (SP-3) ← MBE, RBE, 0, 0 PC₁₀₋₀ ← (taddr)₂₋₀ + (taddr+1) SP ← SP-4 | | |
| | | | | | <ul style="list-style-type: none"> • When instruction other than TBR and TCALL instructions (taddr) (taddr+1) instruction is executed. | | Depending on the reference instruction |
| | | | | | <ul style="list-style-type: none"> • μPD754304 • When TBR instruction PC₁₁₋₀ ← (taddr)₃₋₀ + (taddr+1) | | |
| <ul style="list-style-type: none"> • When TCALL instruction (SP-4) (SP-1) (SP-2) ← PC₁₁₋₀ (SP-3) ← MBE, RBE, 0, 0 PC₁₁₋₀ ← (taddr)₃₋₀ + (taddr+1) SP ← SP-4 | | | | | | | |
| <ul style="list-style-type: none"> • When instruction other than TBR and TCALL instructions (taddr) (taddr+1) instruction is executed. | | | | | Depending on the reference instruction | | |
| | | | 3 | <ul style="list-style-type: none"> • μPD754302 • When TBR instruction PC₁₀₋₀ ← (taddr)₂₋₀ + (taddr+1) | *10 | | |
| | | 4 | <ul style="list-style-type: none"> • When TCALL instruction (SP-6) (SP-3) (SP-4) ← PC₁₀₋₀ (SP-5) ← 0, 0, 0, 0 (SP-2) ← x, x, MBE, RBE PC₁₀₋₀ ← (taddr)₂₋₀ + (taddr+1) SP ← SP-6 | | | | |
| | | 3 | <ul style="list-style-type: none"> • When instruction other than TBR and TCALL instructions (taddr) (taddr+1) instruction is executed. | Depending on the reference instruction | | | |

- Notes**
1. The TBR and TCALL instructions are the table definition assembler directives of the GETI instruction.
 2. The above operations in the double boxes can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.

| Instruction group | Mnemonic | Operand | Number of bytes | Number of machine cycles | Operation | Addressing area | Skip condition |
|-------------------|--------------------------------|---------|-----------------|--------------------------|--|-----------------|--|
| Special | GETI <small>Notes 1, 2</small> | taddr | 1 | 3 | <ul style="list-style-type: none"> • μPD754304 • When TBR instruction $PC_{11-0} \leftarrow (taddr)_{3-0} + (taddr+1)$ | *10 | |
| | | | | 4 | <ul style="list-style-type: none"> • When TCALL instruction $(SP-6) (SP-3) (SP-4) \leftarrow PC_{11-0}$ $(SP-5) \leftarrow 0, 0, 0, 0$ $(SP-2) \leftarrow x, x, MBE, RBE$ $PC_{11-0} \leftarrow (taddr)_{3-0} + (taddr+1)$ $SP \leftarrow SP-6$ | | |
| | | | | 3 | <ul style="list-style-type: none"> • When instruction other than TBR and TCALL instructions $(taddr) (taddr+1)$ instruction is executed. | | Depending on the reference instruction |

- Notes**
1. The TBR and TCALL instructions are the table definition assembler directives of the GETI instruction.
 2. The above operations in the double boxes can be performed only in the Mk II mode.

12. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25 °C)

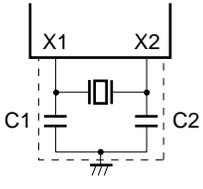
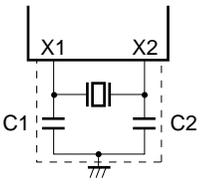
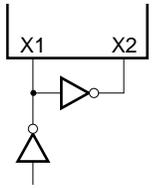
| Parameter | Symbol | Test Conditions | | Ratings | Unit |
|-------------------------------|-----------------------------|-----------------|-------------------------------|-------------------------------|------|
| Supply voltage | V _{DD} | | | -0.3 to +7.0 | V |
| Input voltage | V _{I1} | Except port 5 | | -0.3 to V _{DD} + 0.3 | V |
| | V _{I2} | Port 5 | Pull-up resistor incorporated | -0.3 to V _{DD} + 0.3 | V |
| | | | N-ch open-drain | -0.3 to +14 | V |
| Output voltage | V _O | | | -0.3 to V _{DD} + 0.3 | V |
| Output current, high | I _{OH} | Per pin | | -10 | mA |
| | | For all pins | | -30 | mA |
| Output current, low | I _{OL} Note | Per pin | | 30 | mA |
| | | For all pins | | 220 | mA |
| Operating ambient temperature | T _A | | | -40 to +85 | °C |
| Storage temperature | T _{stg} | | | -65 to +150 | °C |

Caution If any of the parameters exceeds the absolute maximum ratings, even momentarily, the quality of the product may be impaired. The absolute maximum ratings are values that may physically damage the products. Be sure to use the products within the ratings.

Capacitance (T_A = 25 °C, V_{DD} = 0 V)

| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit |
|--------------------|------------------|---------------------------------|------|------|------|------|
| Input capacitance | C _{IN} | f = 1 MHz | | | 15 | pF |
| Output capacitance | C _{OUT} | Unmeasured pins returned to 0 V | | | 15 | pF |
| I/O capacitance | C _{IO} | | | | 15 | pF |

System Clock Oscillator Characteristics (T_A = -40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

| Resonator | Recommended Constant | Parameter | Testing Conditions | MIN. | TYP. | MAX. | Unit |
|-------------------|---|--|---|------|------|----------------------|------|
| Ceramic resonator |  | Oscillation frequency (f _x) ^{Note1} | | 1.0 | | 6.0 ^{Note2} | MHz |
| | | Oscillation stabilization time ^{Note 3} | After V _{DD} reaches MIN. value of oscillation voltage range | | | 4 | ms |
| Crystal resonator |  | Oscillation frequency(f _x) ^{Note1} | | 1.0 | | 6.0 ^{Note2} | MHz |
| | | Oscillation stabilization time ^{Note3} | V _{DD} = 4.5 to 5.5 V | | | 10 | ms |
| | | | | | | 30 | ms |
| External clock |  | X1 input frequency (f _x) ^{Note1} | | 1.0 | | 6.0 ^{Note2} | MHz |
| | | X1 input high- and low-level widths (t _{xH} , t _{xL}) | | 83.3 | | 500 | ns |

- Notes**
1. Only the oscillator characteristics are shown. For the instruction execution time, refer to **AC Characteristics**.
 2. If the oscillation frequency is 4.19 MHz < f_x ≤ 6.0 MHz at 1.8 V ≤ V_{DD} < 2.7 V, set the processor control register (PCC) to a value other than 0011. If the PCC is set to 0011, the rated cycle time of 0.95 μs is not satisfied.
 3. Oscillation stabilization time is a time required for oscillation to stabilize after application of V_{DD}, or after the STOP mode has been released.

Caution When using the oscillation circuit of the main system clock, wire the portion enclosed in dotted lines in the figures as follows to avoid adverse influences on the wiring capacitance:

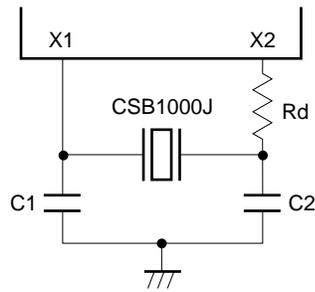
- Keep the wire length as short as possible.
- Do not cross other signal lines.
- Do not route the wiring in the vicinity of lines through which a high fluctuating current flows.
- Always keep the ground point of the capacitor of the oscillation circuit as the same potential as V_{SS}.
- Do not connect the power source pattern through which a high current flows.
- Do not extract signals from the oscillation circuit.

Recommended Oscillation Circuit Constants

Ceramic Resonator (T_A = -40 to +85 °C)

| Manufacturer | Product | Frequency (MHz) | Recommended Circuit Constants (pF) | | Oscillation Voltage Range (V _{DD}) | | Remarks |
|----------------------|--------------------------|-----------------|------------------------------------|--|--|------|--|
| | | | C1 | C2 | MIN. | MAX. | |
| Murata Mfg. Co., Ltd | CSB1000J ^{Note} | 1.0 | 100 | 100 | 2.7 | 5.5 | R _d = 5.6 kΩ |
| | CSA2.00MG | 2.0 | 30 | 30 | 1.8 | 5.5 | |
| | CST2.00MG | | - | - | | | Capacitor incorporated |
| | CSA3.58MG | 3.58 | 30 | 30 | 1.8 | 5.5 | |
| | CST3.58MGW | | - | - | | | Capacitor incorporated |
| | CSA3.58MGU | | 30 | 30 | | | |
| | CST3.58MGWU | | - | - | | | Capacitor incorporated |
| | CSA4.00MG | 4.0 | 30 | 30 | 2.0 | 5.5 | |
| | CST4.00MGW | | - | - | Capacitor incorporated | | |
| | CSA4.00MGU | | 30 | 30 | 1.8 | | |
| | CST4.00MGWU | | - | - | Capacitor incorporated | | |
| | CSA6.00MG | 6.0 | 30 | 30 | 2.9 | 5.5 | |
| | CST6.00MGW | | - | - | Capacitor incorporated | | |
| | CSA6.00MGU | | 30 | 30 | 1.8 | | |
| CST6.00MGWU | - | | - | Capacitor incorporated | | | |
| Kyocera Corp. | KBR-1000F/Y | 1.0 | 100 | 100 | 1.8 | 5.5 | T _A = -20 to +80 °C |
| | KBR-2.0MS | 2.0 | 47 | 47 | 2.0 | 5.5 | |
| | KBR-4.0MSA | 4.0 | 33 | 33 | 1.8 | 5.5 | |
| | KBR-4.0MKS | | - | - | | | Capacitor incorporated, T _A = -20 to +80 °C |
| | PBRC 4.00A | | 33 | 33 | | | T _A = -20 to +80 °C |
| | PBRC 4.00B | - | - | Capacitor incorporated, T _A = -20 to +80 °C | | | |
| | KBR-6.0MSA | 6.0 | 33 | 33 | 1.8 | 5.5 | T _A = -20 to +80 °C |
| | PBRC 6.00A | | | | | | |
| | PBRC 6.00B | | - | - | | | Capacitor incorporated, T _A = -20 to +80 °C |
| ★ TDK | CCR1000K2 | 1.0 | 100 | 100 | 1.8 | 5.5 | |
| | CCR2.0MC33 | 2.0 | - | - | | | Capacitor incorporated |
| | CCR4.19MC3 | 4.19 | | | | | |
| | FCR4.19MC5 | | | | | | |
| | CCR6.0MC3 | 6.0 | | | | | |

Note If using Murata's CSB1000J (1.0 MHz) as the ceramic resonator, a limited resistor ($R_d = 5.6\text{ k}\Omega$) is required (see figure below). If using any other recommended resonator, no limited resistor is needed.



Caution The oscillation circuit constants and oscillation voltage range indicate conditions for stable oscillation, but do not guarantee oscillation frequency accuracy. If oscillation frequency accuracy is required for actual circuits, it is necessary to adjust the oscillation frequency of the resonator in the circuit. Please inquire directly to the maker of the resonator for data as needed.

DC Characteristics (T_A = -40 to + 85 °C, V_{DD} = 1.8 to 5.5 V)

| Parameter | Symbol | Test Conditions | | MIN. | TYP. | MAX. | Unit | |
|---------------------------|-------------------|--|--|---------------------------------|---------------------|---------------------|------|----|
| Output current, low | I _{OL} | Per pin | | | | 15 | mA | |
| | | For all pins | | | | 150 | mA | |
| Input voltage, high | V _{IH1} | Ports 2, 3, 8 | | 2.7 V ≤ V _{DD} ≤ 5.5 V | 0.7 V _{DD} | V _{DD} | V | |
| | | | | 1.8 V ≤ V _{DD} < 2.7 V | 0.9 V _{DD} | V _{DD} | V | |
| | V _{IH2} | Ports 0, 1, 6, 7, RESET | | 2.7 V ≤ V _{DD} ≤ 5.5 V | 0.8 V _{DD} | V _{DD} | V | |
| | | | | 1.8 V ≤ V _{DD} < 2.7 V | 0.9 V _{DD} | V _{DD} | V | |
| | V _{IH3} | Port 5 | Pull-up resistor incorporated | 2.7 V ≤ V _{DD} ≤ 5.5 V | 0.7 V _{DD} | V _{DD} | V | |
| | | | | 1.8 V ≤ V _{DD} < 2.7 V | 0.9 V _{DD} | V _{DD} | V | |
| | | N-ch open drain | 2.7 V ≤ V _{DD} ≤ 5.5 V | 0.7 V _{DD} | 13 | V | | |
| | | | 1.8 V ≤ V _{DD} < 2.7 V | 0.9 V _{DD} | 13 | V | | |
| V _{IH4} | X1 | | V _{DD} -0.1 | | V _{DD} | V | | |
| Input voltage, low | V _{IL1} | Ports 2, 3, 5, 8 | | 2.7 V ≤ V _{DD} ≤ 5.5 V | 0 | 0.3 V _{DD} | V | |
| | | | | 1.8 V ≤ V _{DD} < 2.7 V | 0 | 0.1 V _{DD} | V | |
| | V _{IL2} | Ports 0, 1, 6, 7, RESET | | 2.7 V ≤ V _{DD} ≤ 5.5 V | 0 | 0.2 V _{DD} | V | |
| | | | | 1.8 V ≤ V _{DD} < 2.7 V | 0 | 0.1 V _{DD} | V | |
| | V _{IL3} | X1 | | 0 | | 0.1 | V | |
| Output voltage, high | V _{OH} | SCK, SO, ports 2, 3, 6, 7, 8 I _{OH} = -1 mA | | V _{DD} -0.5 | | | V | |
| Output voltage, low | V _{OL1} | SCK, SO, ports 2, 3, 5, 6, 7, 8 | | I _{OL} = 15 mA | 0.2 | 2.0 | V | |
| | | | | V _{DD} = 5 V ± 10% | | | | |
| | | | | I _{OL} = 1.6 mA | | | 0.4 | V |
| V _{OL2} | SB0 | N-ch open-drain pull-up resistor ≥ 1 kΩ | | | | 0.2 V _{DD} | V | |
| Input leak current, high | I _{LIH1} | V _I = V _{DD} | Pins other than X1 | | | 3 | μA | |
| | I _{LIH2} | | X1 | | | 20 | μA | |
| | I _{LIH3} | V _I = 13 V | Port 5 (N-ch open drain) | | | 20 | μA | |
| Input leak current, low | I _{LIL1} | V _I = 0 V | Pins other than X1 and port 5 | | | -3 | μA | |
| | I _{LIL2} | | X1 | | | -20 | μA | |
| | I _{LIL3} | | Port 5 (N-ch open drain) | | | | -3 | μA |
| | | | Other than input instruction execution time | | | | | |
| | | | Port 5 (N-ch open drain) Input | | | | -30 | μA |
| | | | Input instruction execution time | | | -10 | -27 | μA |
| Output leak current, high | I _{LOH1} | V _O = V _{DD} | SCK, SO/SB0, ports 2, 3, 6, 7, 8, port 5 (with on-chip pull-up resistor) | | | 3 | μA | |
| | I _{LOH2} | V _O = 13 V | Port 5 (N-ch open drain) | | | 20 | μA | |
| Output leak current, low | I _{LOL} | V _O = 0 V | | | | -3 | μA | |
| On-chip pull-up resistor | R _{L1} | V _I = 0 V | Ports 0 to 3 and 6 to 8 (except P00 pin) | | 50 | 100 | 200 | kΩ |
| | R _{L2} | | Port 5 | | 15 | 30 | 60 | kΩ |

DC Characteristics (T_A = -40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

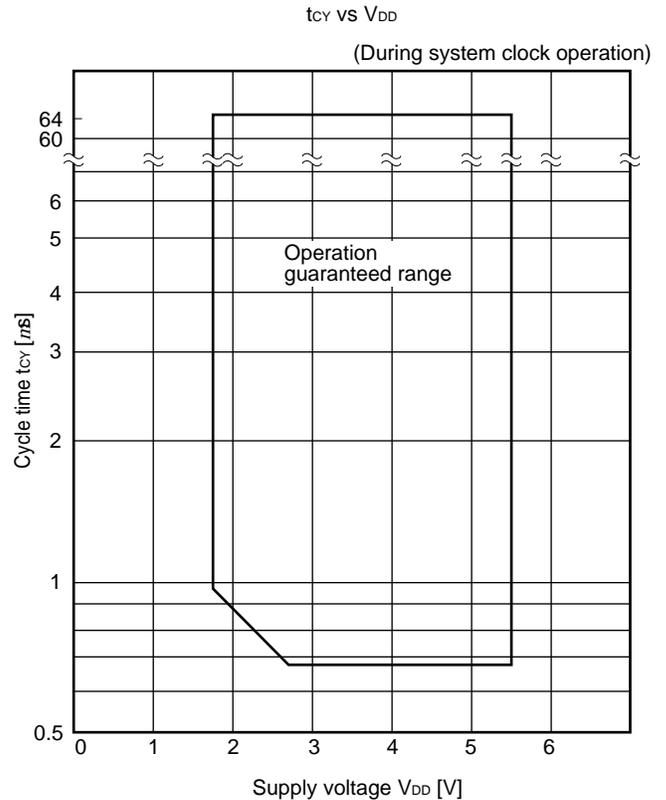
| Parameter | Symbol | Test Conditions | | MIN. | TYP. | MAX. | Unit | | |
|---------------------------------|------------------|-------------------|--|--|------|------|------|------|----|
| Supply current ^{Note1} | I _{DD1} | 6.00 MHz | V _{DD} = 5.0 V ± 10% ^{Note2} | | | 1.50 | 5.00 | mA | |
| | | Crystal resonator | V _{DD} = 3.0 V ± 10% ^{Note3} | | | 0.33 | 1.00 | mA | |
| | I _{DD2} | C1 = C2 = 22 pF | HALT mode | V _{DD} = 5.0 V ± 10% | | 0.61 | 1.85 | mA | |
| | | | | V _{DD} = 3.0 V ± 10% | | 0.24 | 0.75 | mA | |
| | I _{DD1} | 4.19 MHz | Crystal resonator | V _{DD} = 5.0 V ± 10% ^{Note2} | | | 1.20 | 3.50 | mA |
| | | | | V _{DD} = 3.0 V ± 10% ^{Note3} | | | 0.17 | 0.55 | mA |
| | I _{DD2} | C1 = C2 = 22 pF | HALT mode | V _{DD} = 5.0 V ± 10% | | | 0.40 | 1.50 | mA |
| | | | | V _{DD} = 3.0 V ± 10% | | | 0.13 | 0.50 | mA |
| | I _{DD5} | STOP mode | V _{DD} = 5.0 V ± 10% | | | 0.05 | 10.0 | μA | |
| | | | V _{DD} = 3.0 V ± 10% | | | 0.02 | 5.00 | μA | |
| T _A = 25 °C | | | | 0.02 | 3.00 | μA | | | |

- Notes**
- Does not include current fed to on-chip pull-up resistor.
 - When processor clock control register (PCC) is set to 0011, during high-speed mode.
 - When PCC is set to 0000, during low-speed mode.

AC Characteristics (T_A = -40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit | | |
|---|---------------------------------------|--------------------------------|--------------------------------|---------------|------|------|-----|----|
| CPU clock cycle time ^{Note1} (Minimum instruction execution time = 1 machine cycle) | t _{cy} | When system clock is used | V _{DD} = 2.7 to 5.5 V | 0.67 | | 64 | μs | |
| | | | | 0.95 | | 64 | μs | |
| TI0, TI1 input frequency | f _{TI} | V _{DD} = 2.7 to 5.5 V | | 0 | | 1 | MHz | |
| | | | | 0 | | 275 | kHz | |
| TI0, TI1 input high- and low-level width | t _{TIH} , t _{TIL} | V _{DD} = 2.7 to 5.5 V | | 0.48 | | | μs | |
| | | | | 1.8 | | | μs | |
| Interrupt input high- and low-level width | t _{INTH} , t _{INTL} | INT0 | IM02 = 0 | Note 2 | | | μs | |
| | | | IM02 = 1 | 10 | | | μs | |
| | | INT1, 2, 4 | | | 10 | | | μs |
| | | KR0-7 | | | 10 | | | μs |
| RESET low-level width | t _{RSL} | | 10 | | | μs | | |

- Notes 1.** The CPU clock (Φ) cycle time (minimum instruction execution time) is determined by the oscillation frequency of the connected resonator and the processor clock control register (PCC). The figure on the right shows the cycle time t_{cy} characteristics against the supply voltage V_{DD} when the system clock is used.
- 2.** 2t_{cy} or 128/f_x depending on the setting of the interrupt mode register (IM0).



Serial Transfer Operation

2-wire and 3-wire Serial I/O Mode ($\overline{\text{SCK}}$...Internal clock output) ($T_A = -40$ to $+85$ °C, $V_{DD} = 1.8$ to 5.5 V)

| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit |
|--|-------------------|---------------------------------------|---------------------------|------|------|------|
| $\overline{\text{SCK}}$ cycle time | t_{KCY1} | $V_{DD} = 2.7$ to 5.5 V | 1300 | | | ns |
| | | | 3800 | | | ns |
| $\overline{\text{SCK}}$ high- and low-level width | t_{KL1} | $V_{DD} = 2.7$ to 5.5 V | $t_{\text{KCY1}}/2-50$ | | | ns |
| | t_{KH1} | | $t_{\text{KCY1}}/2-150$ | | | ns |
| SI ^{Note1} setup time (to $\overline{\text{SCK}}\uparrow$) | t_{SIK1} | $V_{DD} = 2.7$ to 5.5 V | 150 | | | ns |
| | | | 500 | | | ns |
| SI ^{Note1} hold time (from $\overline{\text{SCK}}\uparrow$) | t_{KSI1} | $V_{DD} = 2.7$ to 5.5 V | 400 | | | ns |
| | | | 600 | | | ns |
| $\overline{\text{SCK}}\downarrow \rightarrow \text{SO}^{\text{Note1}}$ output delay time | t_{KSO1} | R = 1 kΩ, C = 100 pF ^{Note2} | $V_{DD} = 2.7$ to 5.5 V | | 250 | ns |
| | | | | 0 | 1000 | ns |

Notes 1. SB0 in the 2-wire serial I/O mode.

2. R and C are the load resistance and load capacitance of the SO output line.

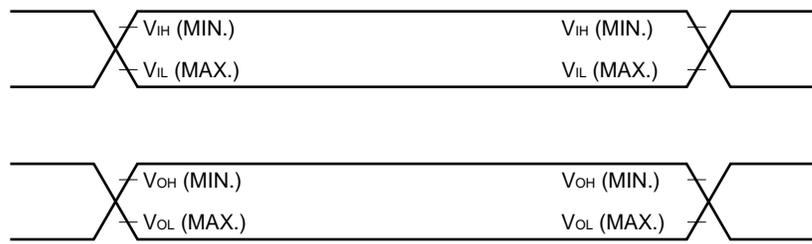
2-wire and 3-wire Serial I/O Mode ($\overline{\text{SCK}}$...External clock input) ($T_A = -40$ to $+85$ °C, $V_{DD} = 1.8$ to 5.5 V)

| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit |
|--|-------------------|---------------------------------------|---------------------------|------|------|------|
| $\overline{\text{SCK}}$ cycle time | t_{KCY2} | $V_{DD} = 2.7$ to 5.5 V | 800 | | | ns |
| | | | 3200 | | | ns |
| $\overline{\text{SCK}}$ high- and low-level width | t_{KL2} | $V_{DD} = 2.7$ to 5.5 V | 400 | | | ns |
| | t_{KH2} | | 1600 | | | ns |
| SI ^{Note1} setup time (to $\overline{\text{SCK}}\uparrow$) | t_{SIK2} | $V_{DD} = 2.7$ to 5.5 V | 100 | | | ns |
| | | | 150 | | | ns |
| SI ^{Note1} hold time (from $\overline{\text{SCK}}\uparrow$) | t_{KSI2} | $V_{DD} = 2.7$ to 5.5 V | 400 | | | ns |
| | | | 600 | | | ns |
| $\overline{\text{SCK}}\downarrow \rightarrow \text{SO}^{\text{Note1}}$ output delay time | t_{KSO2} | R = 1 kΩ, C = 100 pF ^{Note2} | $V_{DD} = 2.7$ to 5.5 V | | 300 | ns |
| | | | | 0 | 1000 | ns |

Notes 1. SB0 in the 2-wire serial I/O mode.

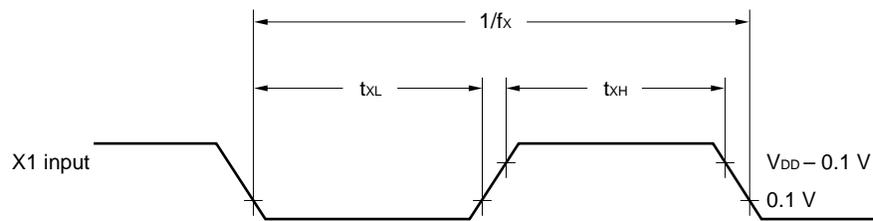
2. R and C are the load resistance and load capacitance of the SO output line.

AC Timing Test Points (Excluding X1 Input)

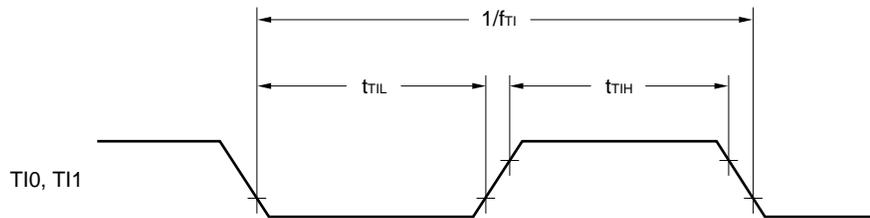


Note For the values, refer to the **DC Characteristics**.

Clock Timing

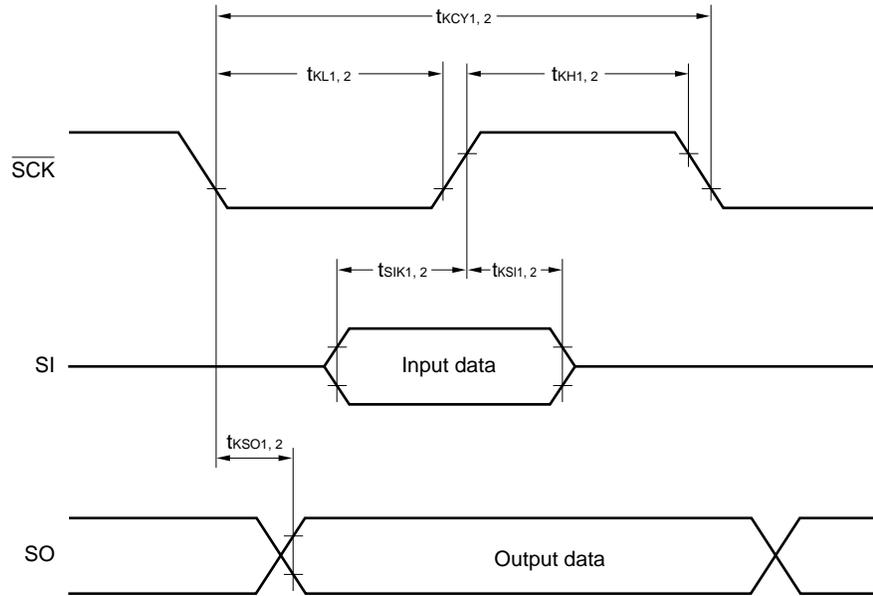


T10, T11 Timing

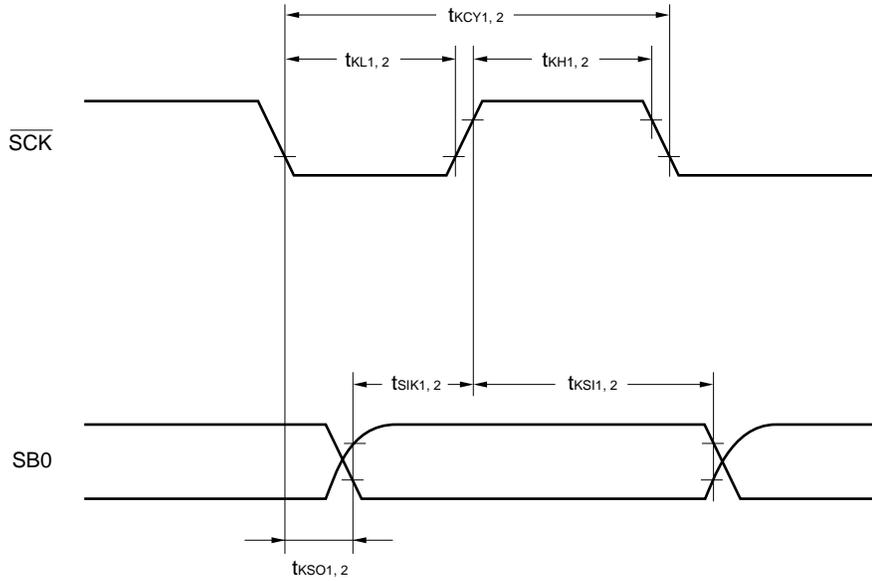


Serial Transfer Timing

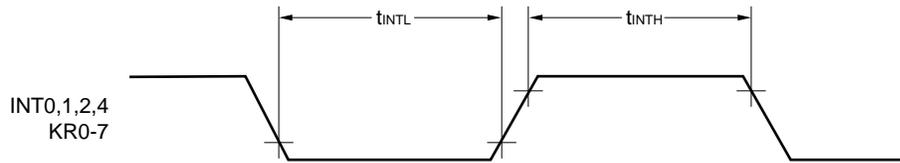
3-wire Serial I/O Mode



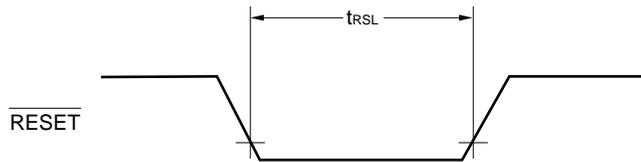
2-wire Serial I/O Mode



Interrupt Input Timing



RESET Input Timing



Data Memory STOP Mode Low-Supply Voltage Data Retention Characteristics (T_A = -40 to +85 °C)

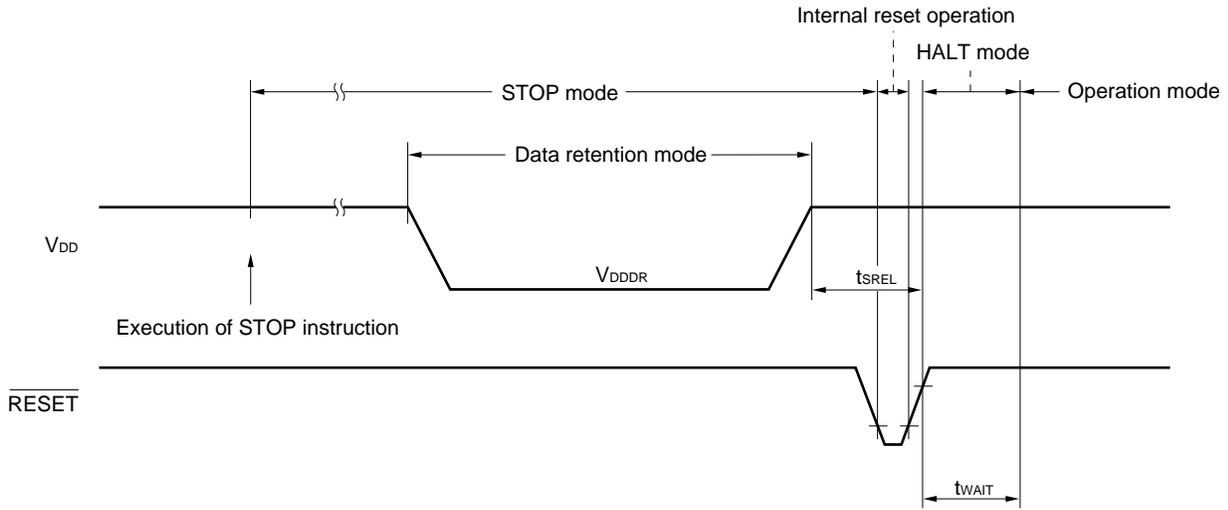
| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit |
|--|------------|-------------------------------|------|--------------|------|------|
| Release signal set time | t_{SREL} | | 0 | | | μs |
| Oscillation stabilization wait time ^{Note1} | t_{WAIT} | Release by \overline{RESET} | | Note2 | | ms |
| | | Release by interrupt request | | Note3 | | ms |

★

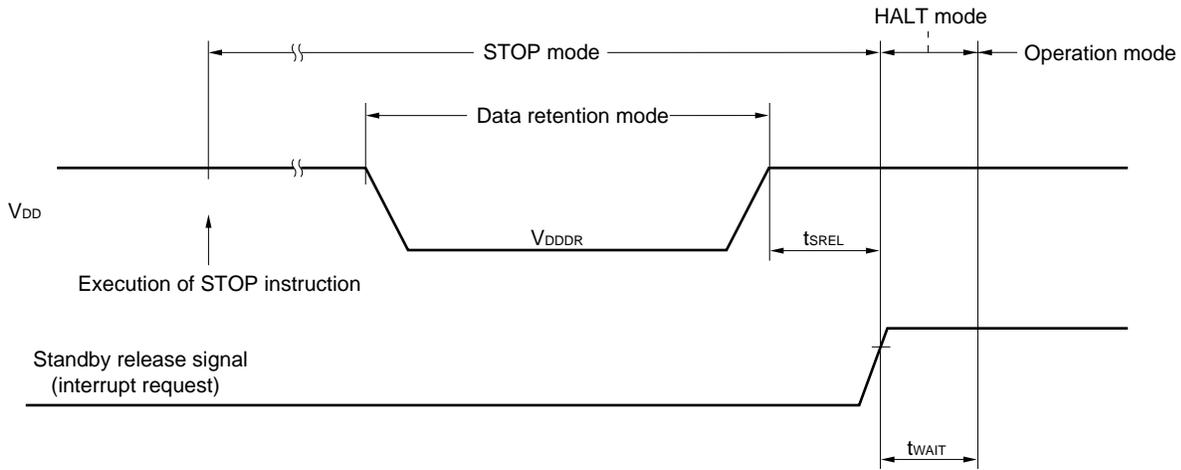
- Notes**
1. The oscillation stabilization wait time is the time during which the CPU operation is stopped to avoid unstable operation at oscillation start.
 2. $2^{17}/f_x$ and $2^{15}/f_x$ can be selected with mask option.
 3. Depends on setting of basic interval timer mode register (BTM) (see table below).

| BTM3 | BTM2 | BTM1 | BTM0 | Wait Time | |
|------|------|------|------|--------------------------------|--------------------------------|
| | | | | When $f_x = 4.19$ MHz | When $f_x = 6.0$ MHz |
| - | 0 | 0 | 0 | $2^{20}/f_x$ (Approx. 250 ms) | $2^{20}/f_x$ (Approx. 175 ms) |
| - | 0 | 1 | 1 | $2^{17}/f_x$ (Approx. 31.3 ms) | $2^{17}/f_x$ (Approx. 21.8 ms) |
| - | 1 | 0 | 1 | $2^{15}/f_x$ (Approx. 7.81 ms) | $2^{15}/f_x$ (Approx. 5.46 ms) |
| - | 1 | 1 | 1 | $2^{13}/f_x$ (Approx. 1.95 ms) | $2^{13}/f_x$ (Approx. 1.37 ms) |

★ Data Retention Timing (on releasing STOP mode by $\overline{\text{RESET}}$)



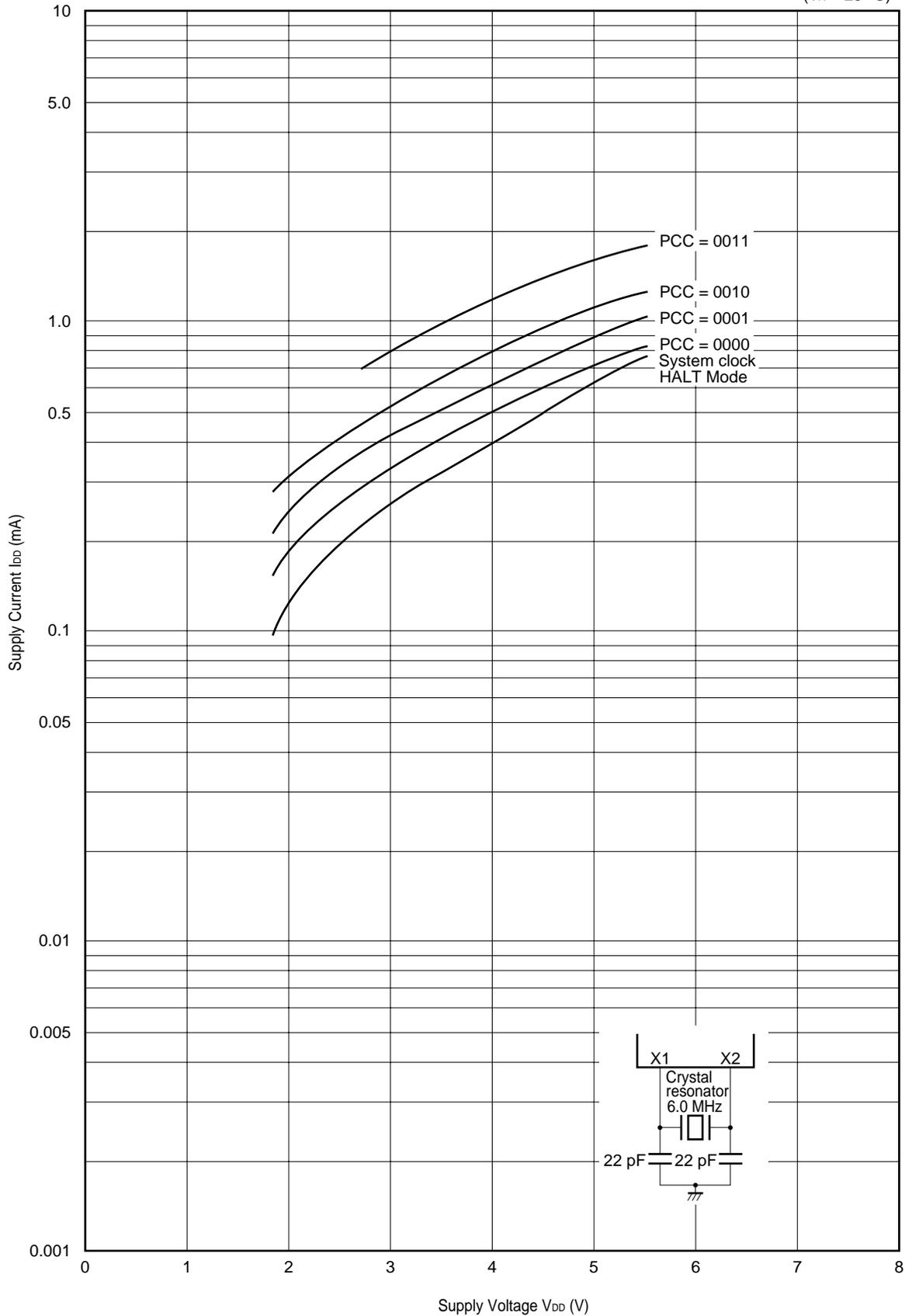
★ Data Retention Timing (Standby release signal: on releasing STOP mode by interrupt signal)



13. CHARACTERISTICS CURVES (REFERENCE VALUES)

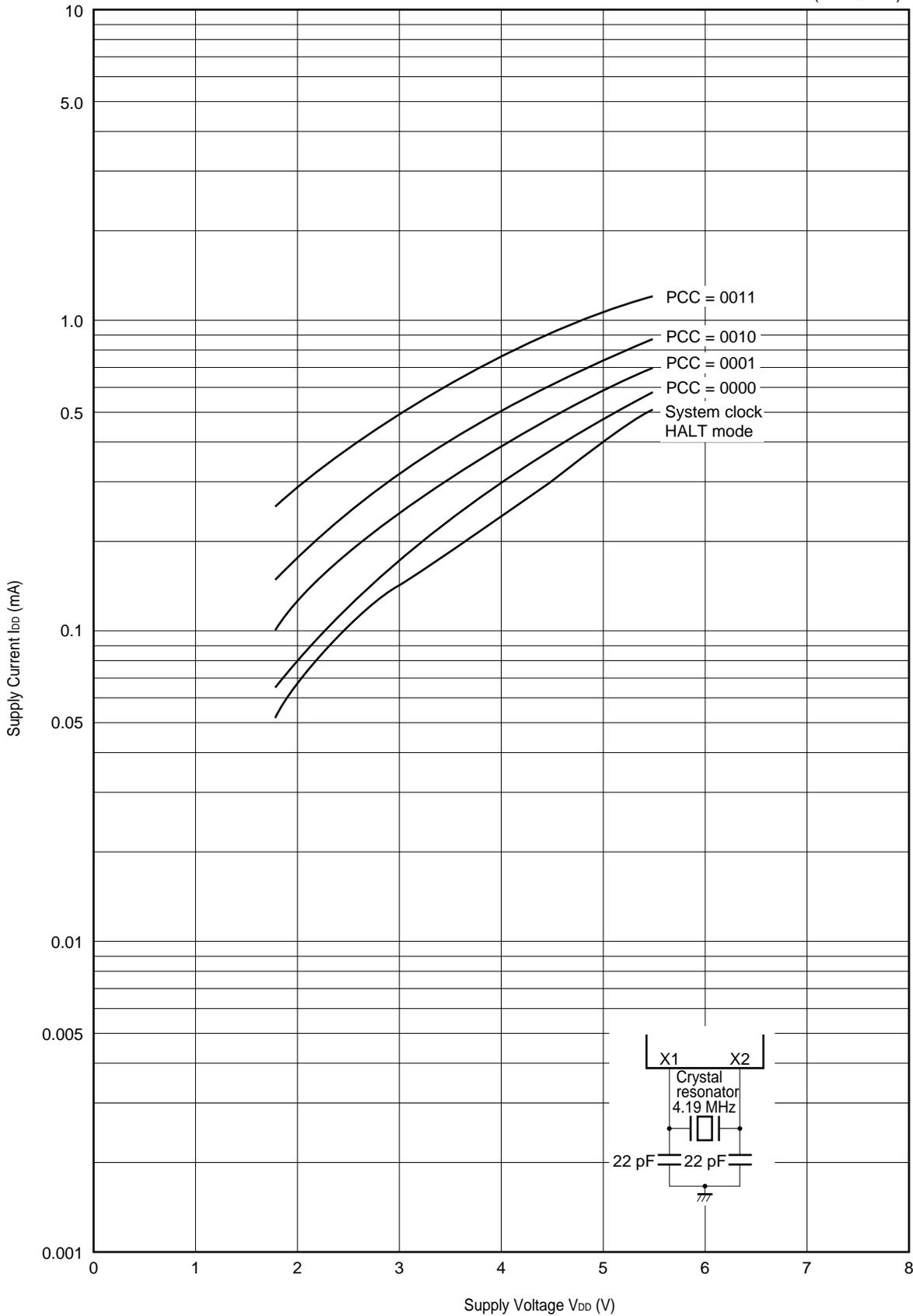
I_{DD} vs V_{DD} (System Clock: 6.0-MHz Crystal Resonator)

(T_A = 25 °C)



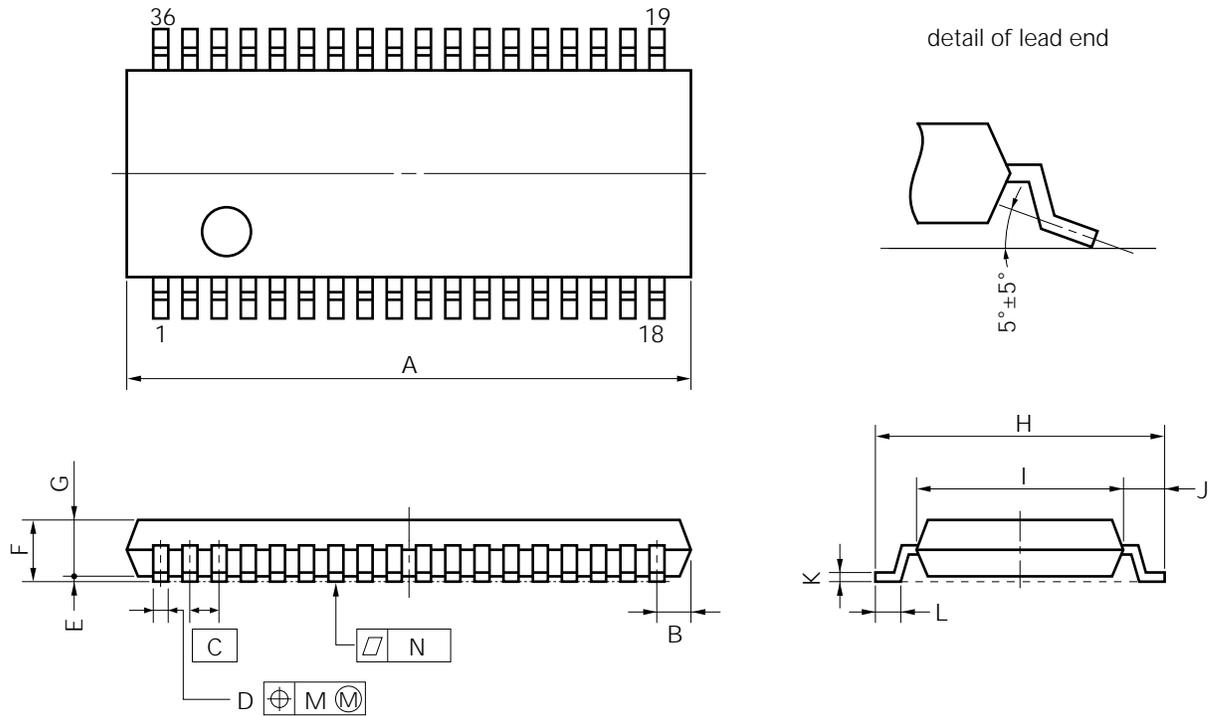
I_{DD} vs V_{DD} (System Clock: 4.19-MHz Crystal Resonator)

(T_A = 25 °C)



14. PACKAGE DRAWING

36 PIN PLASTIC SHRINK SOP (300 mil)



NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

P36GM-80-300B-3

| ITEM | MILLIMETERS | INCHES |
|------|--|---|
| A | 15.54 MAX. | 0.612 MAX. |
| B | 0.97 MAX. | 0.039 MAX. |
| C | 0.8 (T.P.) | 0.031 (T.P.) |
| D | 0.35 ^{+0.10} _{-0.05} | 0.014 ^{+0.004} _{-0.003} |
| E | 0.125±0.075 | 0.005±0.003 |
| F | 1.8 MAX. | 0.071 MAX. |
| G | 1.55 | 0.061 |
| H | 7.7±0.3 | 0.303±0.012 |
| I | 5.6 | 0.220 |
| J | 1.1 | 0.043 |
| K | 0.20 ^{+0.10} _{-0.05} | 0.008 ^{+0.004} _{-0.002} |
| L | 0.6±0.2 | 0.024 ^{+0.008} _{-0.009} |
| M | 0.10 | 0.004 |
| N | 0.10 | 0.004 |

15. RECOMMENDED SOLDERING CONDITIONS

The μPD754304 should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 15-1. Surface Mounting Type Soldering Conditions

μPD754302GS-xxx: 36-pin plastic shrink SOP (300 mil, 0.8-mm pitch)

μPD754304GS-xxx: 36-pin plastic shrink SOP (300 mil, 0.8-mm pitch)

μPD754302GS(A)-xxx: 36-pin plastic shrink SOP (300 mil, 0.8-mm pitch)

μPD754304GS(A)-xxx: 36-pin plastic shrink SOP (300 mil, 0.8-mm pitch)

| Soldering Method | Soldering Conditions | Symbol |
|----------------------|---|-----------|
| Infrared rays reflow | Package peak temperature: 235 °C, Time: 30 seconds max. (at 210 °C or higher), Count: Twice or less | IR35-00-2 |
| VPS | Package peak temperature: 215 °C, Time: 40 seconds max. (at 200 °C or higher), Count: Twice or less | VP15-00-2 |
| Wave soldering | Solder temperature: 260 °C or below, Time: 10 seconds max., Count: Once, Preheating temperature: 120 °C MAX. (package surface temperature) | WS60-00-1 |
| Partial heating | Pin temperature: 300 °C or below, Time: 3 seconds max. (per pin row) | — |

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX A. COMPARISON OF FUNCTIONS AMONG μPD750004, 754304, AND 75P4308

| Item | | μPD750004 | μPD754304 | μPD75P4308 |
|---|--------------------------------------|---|---|---|
| Program memory | | Mask ROM 0000H-0FFFH (4096 × 8 bits) | Mask ROM 0000H-0FFFH (4096 × 8 bits) | One-time PROM 0000H-1FFFH (8192 × 8 bits) |
| Data memory | | 000H-1FFFH (512 × 4 bits) | | |
| CPU | | 75XL CPU | | |
| Instruction execution time | w/main system clock | <ul style="list-style-type: none"> • 0.67, 1.33, 2.67, or 10.7 μs (at 6.0 MHz) • 0.95, 1.91, 3.81, or 15.3 μs (at 4.19 MHz) | | |
| | w/subsystem clock | • 122 μs (at 32.768 kHz) | No subsystem clock | |
| I/O port | CMOS input | 8 (of which 7 can be connected with on-chip pull-up resistor via software) | | |
| | CMOS I/O | 18 (on-chip pull-up resistor can be connected via software) | | |
| | N-ch open-drain I/O (withstand 13 V) | 8 (pull-up resistor can be connected by mask option) | 4 (pull-up resistor can be connected by mask option) | 4 (no mask option) |
| | Total | 34 | 30 (no port 4 pins) | |
| Timer | | 4 channels <ul style="list-style-type: none"> • Basic interval timer/watchdog timer • 8-bit timer/event counter • 8-bit timer • Watch timer | 3 channels <ul style="list-style-type: none"> • Basic interval timer/watchdog timer • 8-bit timer/event counter 0 (fx/2² added) • 8-bit timer/event counter 1 (TI1, fx/2² added) (can be used as 16-bit timer/event counter) | |
| Clock output (PCL) | | <ul style="list-style-type: none"> • Φ, 524, 262, or 65.5 kHz (main system clock: 4.19 MHz) • Φ, 750, 375, or 93.8 kHz (main system clock: 6.0 MHz) | | |
| BUZ output | | Provided | None | |
| Serial interface | | 3 modes are supported <ul style="list-style-type: none"> • 3-wire serial I/O mode ... MSB/LSB first selectable • 2-wire serial I/O mode • SBI mode | 2 modes are supported <ul style="list-style-type: none"> • 3-wire serial I/O mode ... MSB/LSB first selectable • 2-wire serial I/O mode | |
| Watch mode register (WM) | | Provided | None | |
| System clock control register (SCC) | | | | |
| Suboscillation circuit control register (SOS) | | | | |
| MBS register | | MB0, 1 | MB0 only | |
| Stack area (SBS1, 0) | | | | |

| Item | μPD750004 | μPD754304 | μPD75P4308 |
|-------------------------------|--|---|------------|
| TM0, 1 registers | Bits 0, 1, and 7 are fixed to 0 | | – |
| Vectored interrupt | External: 3, internal: 4 | | |
| Test input | External: 1, internal: 1 | External: 1 | |
| Test enable flag (IEW) | Provided | None | |
| Test request flag (IRQW) | | | |
| Supply voltage | V _{DD} = 2.2 to 5.5 V | V _{DD} = 1.8 to 5.5 V | |
| Operating ambient temperature | T _A = –40 to +85 °C | | |
| Package | <ul style="list-style-type: none"> • 42-pin plastic shrink DIP (600 mil) • 44-pin plastic QFP (10 × 10 mm) | <ul style="list-style-type: none"> • 36-pin plastic shrink SOP (300 mil, 0.8-mm pitch) | |

APPENDIX B. DEVELOPMENT TOOLS

The following development tools are available for development of application systems using the μPD754304. In the 75XL Series, a common relocatable assembler is used in combination with a device file dedicated to each model.

Language processor

| RA75X relocatable assembler | Host machine | | Order code (part number) | |
|----------------------------------|--------------|---------------------------------------|--------------------------|-------------|
| | | OS | Supply media | |
| PC-9800 series | | MS-DOS™ | 3.5" 2HD | μS5A13RA75X |
| | | (Ver. 3.30 to Ver. 6.2 Note) | 5" 2HD | μS5A10RA75X |
| IBM PC/AT™ or compatible machine | | Refer to "OS for IBM PC" | 3.5" 2HC | μS7B13RA75X |
| | | | 5" 2HC | μS7B10RA75X |

| Device file | Host machine | | Order code (part number) | |
|---------------------------------|--------------|---------------------------------------|--------------------------|----------------|
| | | OS | Supply media | |
| PC-9800 series | | MS-DOS | 3.5" 2HD | μS5A13DF754304 |
| | | (Ver. 3.30 to Ver. 6.2 Note) | 5" 2HD | μS5A10DF754304 |
| IBM PC/AT or compatible machine | | Refer to "OS for IBM PC" | 3.5" 2HC | μS7B13DF754304 |
| | | | 5" 2HC | μS7B10DF754304 |

PROM writing tools

| Hardware | PG-1500 | The PG-1500 is a PROM programmer that can program PROM-contained single-chip microcontrollers in the standalone mode or under control of a host machine, when connected with an accessory board and an optional programmer adapter. It can also program representative PROMs including 256K-bit to 4M-bit models. | | | |
|---------------------------------|--------------------------|---|---------------------------------------|--------------------------|--------------|
| | PA-75P4308GS | This is a PROM programmer adapter dedicated to the μPD75P4308GS and connected to the PG-1500. | | | |
| Software | PG-1500 controller | This connects the PG-1500 and a host machine with a serial or parallel interface to control the PG-1500 from the host machine. | | | |
| | | Host machine | | Order code (part number) | |
| | | | OS | Supply media | |
| | | PC-9800 series | MS-DOS | 3.5" 2HD | μS5A13PG1500 |
| | | | (Ver. 3.30 to Ver. 6.2 Note) | 5" 2HD | μS5A10PG1500 |
| IBM PC/AT or compatible machine | Refer to "OS for IBM PC" | 3.5" 2HD | μS7B13PG1500 | | |
| | | 5" 2HC | μS7B10PG1500 | | |

Note Although Ver.5.00 and later have a task swap function, this function cannot be used with this software.

Remark The operation of the assembler, device file and PG-1500 controller is guaranteed only on the above host machine and OS.

Debugging tools

The in-circuit emulators (IE-75000-R and IE-75001-R) are available as the program debugging tool for the μPD754304.

The system configurations are described as follows.

| | | | | | |
|----------|------------------------------|--|--|--------------|--------------------------|
| Hardware | IE-75000-R ^{Note 1} | In-circuit emulator for debugging the hardware and software when developing the application systems that use the 75X series and 75XL series. When developing a μPD754304 subseries, the emulation board IE-75300-R-EM and emulation probe that are sold separately must be used with the IE-75000-R. By connecting with the host machine and the PROM programmer, efficient debugging can be made. It contains the emulation board IE-75000-R-EM which is connected. | | | |
| | IE-75001-R | In-circuit emulator for debugging the hardware and software when developing the application systems that use the 75X series and 75XL series. When developing a μPD754304 subseries, the emulation board IE-75300-R-EM and emulation probe which are sold separately must be used with the IE-75001-R. It can debug the system efficiently by connecting the host machine and PROM programmer. | | | |
| | IE-75300-R-EM | Emulation board for evaluating the application systems that use a μPD754304 subseries. It must be used with the IE-75000-R or IE-75001-R. | | | |
| | EP-754304GS-R | Emulation probe for the μPD754304GS. It must be connected to IE-75000-R (or IE-75001-R) and IE-75300-R-EM. It is supplied with the flexible board EV-9500GS-36 which facilitates connection to a target system. | | | |
| Software | IE control program | Connects the IE-75000-R or IE-75001-R to a host machine via RS-232-C and Centronix I/F and controls the IE-75000-R or IE-75001-R on a host machine. | | | |
| | | Host machine | OS | Supply media | Order code (Part number) |
| | | PC-9800 series | MS-DOS (Ver. 3.30 to Ver. 6.2 ^{Note 2}) | 3.5" 2HD | μS5A13IE75X |
| | | | | 5" 2HD | μS5A10IE75X |
| | | IBM PC/AT or compatible machine | Refer to "OS for IBM PC" | 3.5" 2HC | μS7B13IE75X |
| 5" 2HC | μS7B10IE75X | | | | |

Notes 1. Maintenance parts

2. Although Ver.5.00 and later have a task swap function, this function cannot be used with this software.

Remark Operation of the IE control program is guaranteed only on the above host machines and OSs.

OS for IBM PC

The following IBM PC OS's are supported.

| OS | Version |
|----------|---|
| PC DOS™ | Ver. 5.02 to Ver. 6.3 J6.1/V Note to J6.3/V Note |
| MS-DOS | Ver. 5.0 to Ver. 6.22 5.0/V Note to 6.2/V Note |
| IBM DOS™ | J5.02/V Note |

Note Only English version is supported.

Caution Ver. 5.0 and later have the task swap function, but this function cannot be used for this software.

APPENDIX C. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Device related documents

| Document Name | Document Number | |
|------------------------------|-----------------|---------------|
| | Japanese | English |
| μPD754302, 754304 Data Sheet | U10797J | This document |
| μPD75P4308 Data Sheet | U10909J | U10909E |
| μPD754304 User's Manual | U10123J | U10123E |
| μPD754304 Instruction Table | IEM-5605 | — |
| 75XL Series Selection Guide | U10453J | U10453E |

Development tool related documents

| Document Name | | | Document Number | |
|---------------|---------------------------------------|------------------------------|-----------------|----------|
| | | | Japanese | English |
| Hardware | IE-75000-R/IE-75001-R User's Manual | | EEU-846 | EEU-1416 |
| | IE-75300-R-EM User's Manual | | U11354J | EEU-1493 |
| | EP-754304GS-R User's Manual | | U10677J | U10677E |
| | PG-1500 User's Manual | | EEU-651 | EEU-1335 |
| Software | RA75X Assembler Package User's Manual | Operation | EEU-731 | EEU-1346 |
| | | Language | EEU-730 | EEU-1363 |
| | PG-1500 Controller User's Manual | PC-9800 series (MS-DOS) base | EEU-704 | EEU-1291 |
| | | PC-9800 series (PC DOS) base | EEU-5008 | U10540E |

Other related documents

| Document Name | Document Number | |
|---|-----------------|----------|
| | Japanese | English |
| IC Package Manual | C10943X | |
| Semiconductor Device Mounting Technology Manual | C10535J | C10535E |
| Quality Grades on NEC Semiconductor Devices | C11531J | IEI-1209 |
| NEC Semiconductor Device Reliability/Quality Control System | C10983J | C10983E |
| Static Electricity Discharge (ESD) Test | MEM-539 | — |
| Guide to Quality Assurance for Semiconductor Devices | MEI-603 | MEI-1202 |
| Microcomputer Related Product Guide - Other Manufacturers | MEI-604 | — |

Caution These documents are subject to change without notice. Be sure to read the latest documents.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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