NEC

MOS INTEGRATED CIRCUIT

μPD75P0116

4-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD75P0116 replaces the μPD750108's internal mask ROM with a one-time PROM and features expanded ROM capacity.

Because the μPD75P0116 supports programming by users, it is suitable for use in prototype testing for system development using the μPD750104, 750106, or 750108 products, and for use in small-lot production.

Detailed information about product features and specifications can be found in the following document
μPD750108 User's Manual: U11330E

FEATURES

- Compatible with μPD750108
- Memory capacity:
  - PROM : 16384 × 8 bits
  - RAM : 512 × 4 bits
- Can operate in same power supply voltage as the mask ROM version μPD750108
  - V_{DD} = 1.8 to 5.5 V

ORDERING INFORMATION

Part number	Package	ROM (× 8 bits)
μPD75P0116CU	42-pin plastic shrink DIP (600 mil, 1.778-mm pitch)	16384
μPD75P0116GB-3BS-MTX	44-pin plastic QFP (10 × 10 mm, 0.8-mm pitch)	16384

Caution On-chip pull-up resistors by mask option cannot be provided.

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FUNCTION LIST

Item		Function	
Instruction execution time		• 4, 8, 16, 64 μs (main system clock: at 1.0 MHz operation) • 2, 4, 8, 32 μs (main system clock: at 2.0 MHz operation) • 122 μs (subsystem clock: at 32.768 kHz operation)	
On-chip memory	PROM	16384 × 8 bits	
	RAM	512 × 4 bits	
General register		• In 4-bit operation: 8 × 4 banks • In 8-bit operation: 4 × 4 banks	
I/O port	CMOS input	8	Connection of on-chip pull-up resistor specifiable by software: 7
	CMOS I/O	18	Direct LED drive capability Connection of on-chip pull-up resistor specifiable by software: 18
	N-ch open drain I/O	8	Direct LED drive capability 13 V withstand voltage
	Total	34	
Timer		4 channels • 8-bit timer/event counter: 1 channel • 8-bit timer counter: 1 channel (with watch timer output function) • Basic interval timer/watchdog timer: 1 channel • Watch timer: 1 channel	
Serial interface		• 3-wire serial I/O mode ... Switching of MSB/LSB-first • 2-wire serial I/O mode • SBI mode	
Bit sequential buffer (BSB)		16 bits	
Clock output (PCL)		• Φ, 125, 62.5, 15.6 kHz (main system clock: at 1.0 MHz operation) • Φ, 250, 125, 31.3 kHz (main system clock: at 2.0 MHz operation)	
Buzzer output (BUZ)		• 2, 4, 32 kHz (subsystem clock: at 32.768 kHz operation) • 0.488, 0.977, 7.813 kHz (main system clock: at 1.0 MHz operation) • 0.977, 1.953, 15.625 kHz (main system clock: at 2.0-MHz operation)	
Vectored interrupt		External: 3 Internal: 4	
Test input		External: 1 Internal: 1	
System clock oscillation circuit		• Main system clock oscillation RC oscillation circuit (with external resistor and capacitor) • Subsystem clock oscillation crystal oscillation circuit	
Standby function		STOP/HALT mode	
Operating ambient temperature		T_A = –40 to +85 °C	
Supply voltage		V_{DD} = 1.8 to 5.5 V	
Package		42-pin plastic shrink DIP (600 mil, 1.778-mm pitch) 44-pin plastic QFP (10 × 10 mm, 0.8-mm pitch)	

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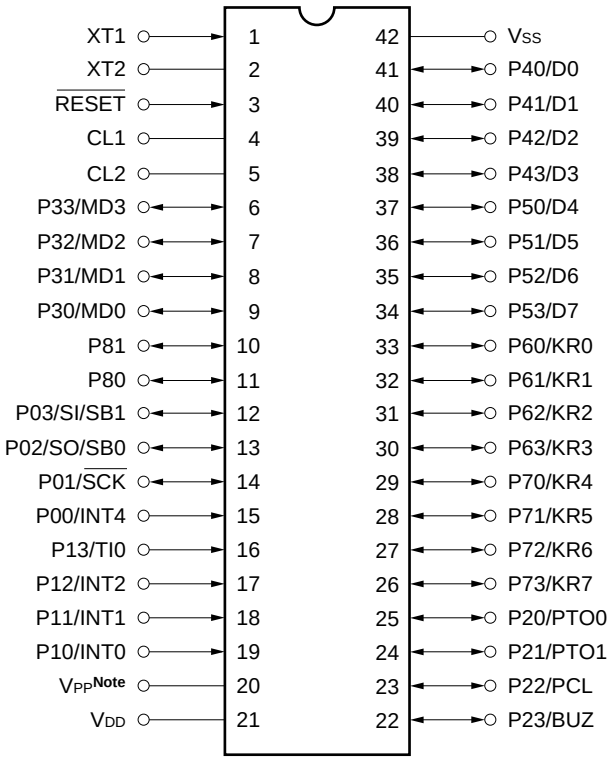
1. PIN CONFIGURATION (Top View)

- 42-pin plastic shrink DIP (600 mil, 1.778-mm pitch)

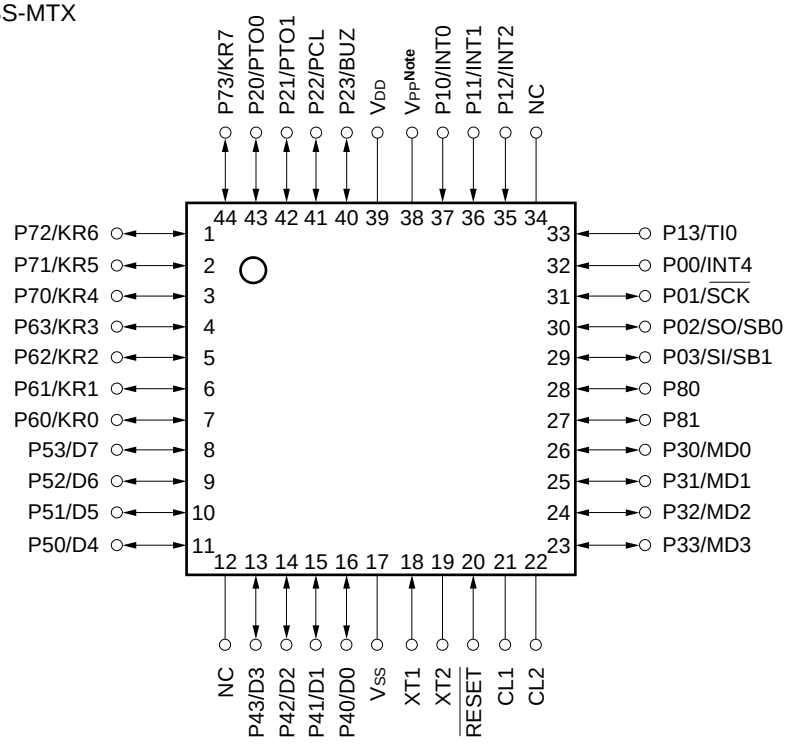
  μPD75P0116CU



Note Directly connect V_{PP} to V_{DD} in the normal operation mode.

- 44-pin plastic QFP (10 × 10 mm, 0.8-mm pitch)

  μPD75P0116GB-3BS-MTX

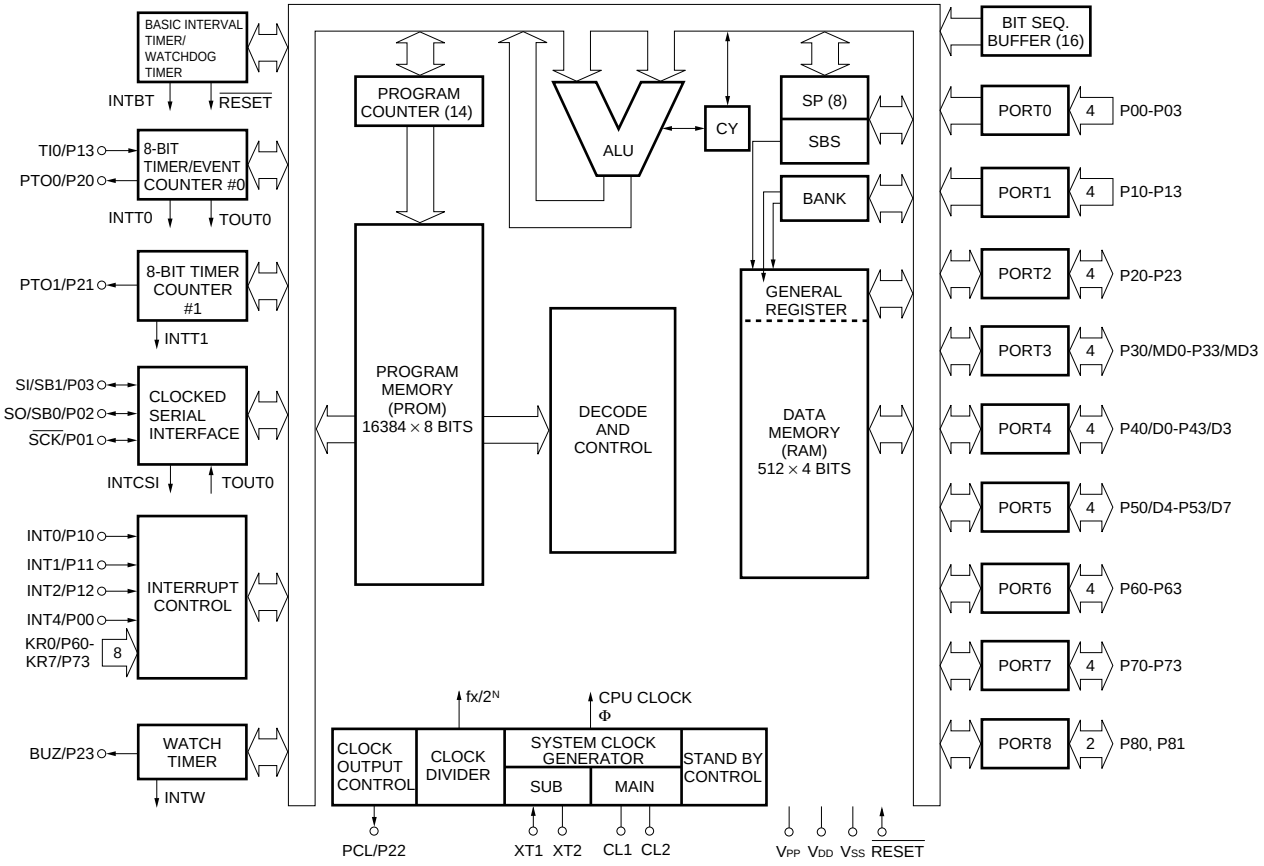


Note Directly connect V_{PP} to V_{DD} in the normal operation mode.

PIN NAMES

BUZ	: Buzzer Clock	P70-P73	: Port7
CL1, CL2	: Main System Clock (RC)	P80, P81	: Port8
D0-D7	: Data Bus 0-7	PCL	: Programmable Clock
INT0, 1, 4	: External Vectored Interrupt 0, 1, 4	PTO0, PTO1	: Programmable Timer Output 0, 1
INT2	: External Test Input 2	$\overline{\text{RESET}}$	: Reset
KR0-KR7	: Key Return 0-7	SB0, SB1	: Serial Data Bus 0, 1
MD0-MD3	: Mode Selection 0-3	$\overline{\text{SCK}}$	: Serial Clock
NC	: No Connection	SI	: Serial Input
P00-P03	: Port0	SO	: Serial Output
P10-P13	: Port1	TI0	: Timer Input 0
P20-P23	: Port2	V_{DD}	: Positive Power Supply
P30-P33	: Port3	V_{PP}	: Programming Power Supply
P40-P43	: Port4	V_{SS}	: Ground
P50-P53	: Port5	XT1, XT2	: Subsystem Clock (Crystal)
P60-P63	: Port6		

2. BLOCK DIAGRAM



3. PIN FUNCTIONS

3.1 Port Pins

Pin name	I/O	Shared by	Function	8-bit I/O	When reset	I/O circuit type Note 1
P00	I	INT4	This is a 4-bit input port (PORT0). For P01 to P03, on-chip pull-up resistor connections are software-specifiable in 3-bit units.	×	Input	<B>
P01	I/O	$\overline{SCK}$				<F>-A
P02	I/O	SO/SB0				<F>-B
P03	I/O	SI/SB1				<M>-C
P10	I	INT0	This is a 4-bit input port (PORT1). On-chip pull-up resistor connections are software-specifiable in 4-bit units. P10/INT0 can select noise elimination circuit.	×	Input	<B>-C
P11		INT1				
P12		INT2				
P13		TI0				
P20	I/O	PTO0	This is a 4-bit I/O port (PORT2). On-chip pull-up resistor connections are software-specifiable in 4-bit units.	×	Input	E-B
P21		PTO1				
P22		PCL				
P23		BUZ				
P30	I/O	MD0	This is a programmable 4-bit I/O port (PORT3). Input and output can be specified in single-bit units. On-chip pull-up resistor connections are software-specifiable in 4-bit units.	×	Input	E-B
P31		MD1				
P32		MD2				
P33		MD3				
P40 Note 2	I/O	D0	This is an N-ch open-drain 4-bit I/O port (PORT4). In the open-drain mode, withstands up to 13 V.	○	High-impedance	M-E
P41 Note 2		D1				
P42 Note 2		D2				
P43 Note 2		D3				
P50 Note 2	I/O	D4	This is an N-ch open-drain 4-bit I/O port (PORT5). In the open-drain mode, withstands up to 13 V.		High-impedance	M-E
P51 Note 2		D5				
P52 Note 2		D6				
P53 Note 2		D7				
P60	I/O	KR0	This is a programmable 4-bit I/O port (PORT6). Input and output can be specified in single-bit units. On-chip pull-up resistor connections are software-specifiable in 4-bit units.	○	Input	<F>-A
P61		KR1				
P62		KR2				
P63		KR3				
P70	I/O	KR4	This is a 4-bit I/O port (PORT7). On-chip pull-up resistor connections are software-specifiable in 4-bit units.		Input	<F>-A
P71		KR5				
P72		KR6				
P73		KR7				
P80	I/O	—	This is a 2-bit I/O port (PORT8). On-chip pull-up resistor connections are software-specifiable in 2-bit units.	×	Input	E-B
P81		—				

Notes 1. Circuit types enclosed in brackets indicate Schmitt triggered inputs.

2. Low-level input current leakage increases when input instructions or bit manipulation instructions are executed.

3.2 Non-port Pins

Pin name	I/O	Shared by	Function		When reset	I/O circuit type Note 1
TI0	I	P13	External event pulse input to timer/event counter		Input	<B>-C
PTO0	O	P20	Timer/event counter output		Input	E-B
PTO1		P21	Timer counter output			
PCL		P22	Clock output			
BUZ		P23	Outputs any frequency (for buzzer or system clock trimming)			
$\overline{SCK}$	I/O	P01	Serial clock I/O		Input	<F>-A
SO/SB0		P02	Serial data output Serial data bus I/O			<F>-B
SI/SB1		P03	Serial data input Serial data bus I/O			<M>-C
INT4	I	P00	Edge-triggered vectored interrupt input (Detects both rising and falling edges).			<B>
INT0	I	P10	Edge-triggered vectored interrupt input (detected edge is selectable). INT0/P10 can select noise elimination circuit.	With noise eliminator /asynch selectable	Input	<B>-C
INT1		P11		Asynchronous		
INT2		P12	Rising edge-triggered testable input	Asynchronous		
KR0-KR3	I	P60-P63	Falling edge-triggered testable input		Input	<F>-A
KR4-KR7	I	P70-P73	Falling edge-triggered testable input		Input	<F>-A
CL1	—	—	Resistor (R) and capacitor (C) connection for main system clock oscillation. External clock cannot be input.		—	—
CL2	—					
XT1	I	—	Crystal resonator connection for subsystem clock. If using an external clock, input it to XT1 and input the inverted clock to X2. XT1 can be used as a 1-bit (test) input.		—	—
XT2	—					
$\overline{RESET}$	I	—	System reset input (low level active)		—	<B>
MD0-MD3	I	P30-P33	Mode selection for program memory (PROM) write/verify.		Input	E-B
D0-D3	I/O	P40-P43	Data bus pin for program memory (PROM) write/verify.		Input	M-E
D4-D7		P50-P53				
V_{PP} Note 2	—	—	Programmable voltage supply in program memory (PROM) write/verify mode. In normal operation mode, connect directly to V_{DD}. Apply +12.5 V in PROM write/verify mode.		—	—
V_{DD}	—	—	Positive power supply		—	—
V_{SS}	—	—	Ground potential		—	—

Notes 1. Circuit types enclosed in brackets indicate Schmitt triggered inputs.

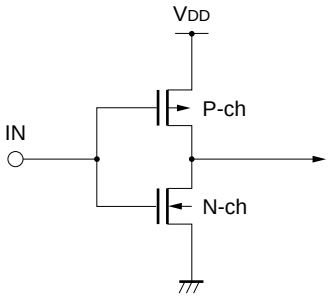
2. During normal operation, the V_{PP} pin will not operate normally unless connected to V_{DD} pin.

3.3 I/O Circuits for Pins

The I/O circuits for the μPD75P0116's pin are shown in schematic diagrams below.

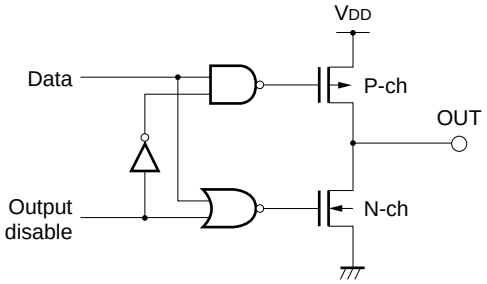
(1/2)

TYPE A



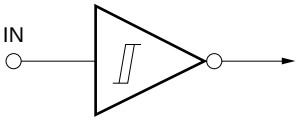
CMOS standard input buffer

TYPE D



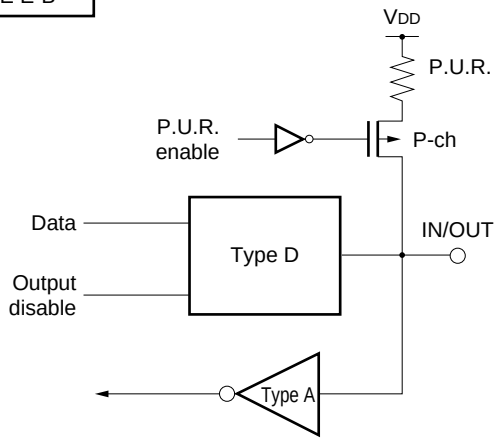
Push-pull output that can be set to high impedance output (with both P-ch and N-ch OFF).

TYPE B



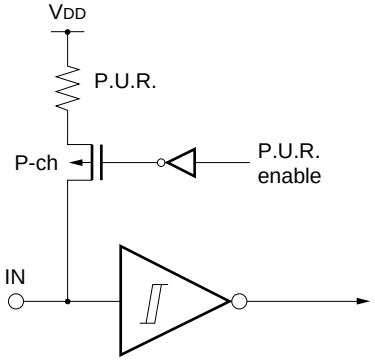
Schmitt trigger input with hysteresis characteristics.

TYPE E-B



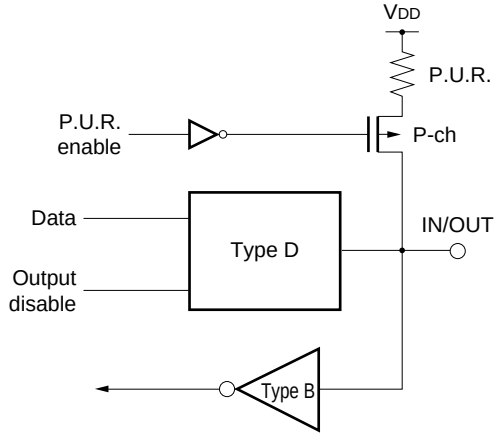
P.U.R. : Pull-Up Resistor

TYPE B-C



P.U.R. : Pull-Up Resistor

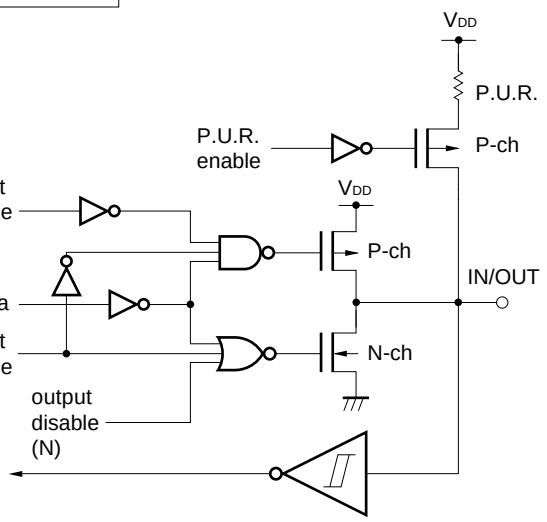
TYPE F-A



P.U.R. : Pull-Up Resistor

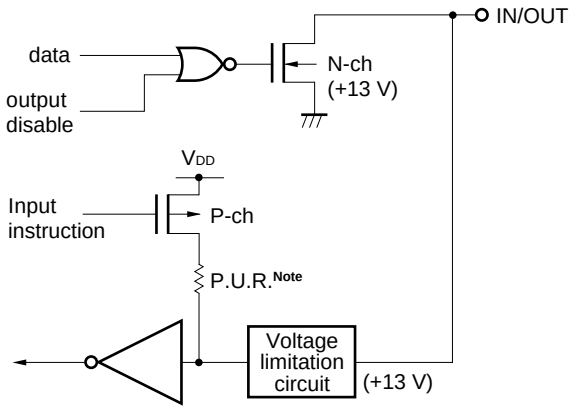
(2/2)

TYPE F-B



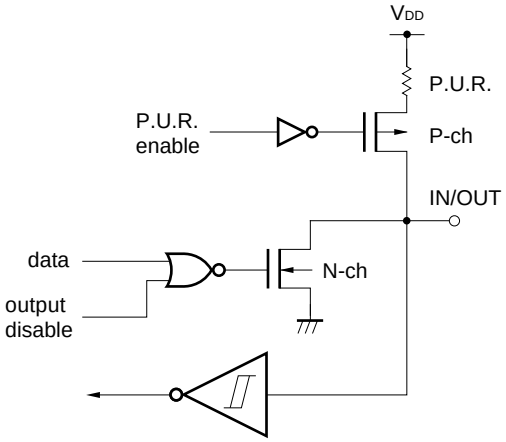
P.U.R. : Pull-Up Resistor

TYPE M-E



Note Pull-up resistor that operates only when an input instruction has been executed. (Current flows from V_{DD} to the pins when at low level)

TYPE M-C



P.U.R. : Pull-Up Resistor

3.4 Handling of Unused Pins

Table 3-1. Handling of Unused Pins

Pin	Recommended connection
P00/INT4	Connect to V_{SS} or V_{DD}
P01/$\overline{SCK}$	Individually connect to V_{SS} or V_{DD} via resistor
P02/SO/SB0	
P03/SI/SB1	Connect to V_{SS}
P10/INT0-P12/INT2	Connect to V_{SS} or V_{DD}
P13/TI0	
P20/PTO0	Input mode : individually connect to V_{SS} or V_{DD} via resistor Output mode : open
P21/PTO1	
P22/PCL	
P23/BUZ	
P30/MD0-P33/MD3	
P40/D0-P43/D3	Connect to V_{SS}
P50/D4-P53/D7	
P60/KR0-P63/KR3	Input mode : individually connect to V_{SS} or V_{DD} via resistor Output mode : open
P70/KR4-P73/KR7	
P80, P81	
XT1[Note]	Connect to V_{SS} or V_{DD}
XT2[Note]	Open
V_{PP}	Make sure to connect directly to V_{DD}

Note When the subsystem clock is not used, set SOS. 0 to 1 (not to use the internal feedback resistor).

4. SWITCHING BETWEEN MK I AND MK II MODES

Setting a stack bank selection (SBS) register for the μPD75P0116 enables the program memory to be switched between the Mk I mode and the Mk II mode. This capability enables the evaluation of the μPD750104, 750106, or 750108 using the μPD75P0116.

When the SBS bit 3 is set to 1: sets Mk I mode (corresponds to Mk I mode of μPD750104, 750106, and 750108)
When the SBS bit 3 is set to 0: sets Mk II mode (corresponds to Mk II mode of μPD750104, 750106, and 750108)

4.1 Differences between Mk I Mode and Mk II Mode

Table 4-1 lists the differences between the Mk I mode and the Mk II mode of the μPD75P0116.

Table 4-1. Differences between Mk I Mode and Mk II Mode

Item		Mk I mode	Mk II mode
Program counter		PC_{13-0}	
Program memory (bytes)		16384	
Data memory (bits)		512 × 4	
Stack	Stack bank	Selectable from memory banks 0 and 1	
	Stack bytes	2 bytes	3 bytes
Instruction	BRA !addr1 CALLA !addr1	None	Provided
Instruction execution time	CALL !addr	3 machine cycles	4 machine cycles
	CALLF !faddr	2 machine cycles	3 machine cycles
Supported mask ROM versions and mode		Mk I mode of μPD750104, 750106, and 750108	Mk II mode of μPD750104, 750106, and 750108

Caution The Mk II mode supports a program area which exceeds 16K bytes in the 75X and 75XL series. This mode enhances the software compatibility with products which have more than 16K bytes.
When the Mk II mode is selected, the number of stack bytes (usable area) used in execution of a subroutine call instruction increases by 1 per stack compared to the Mk I mode. Furthermore, when a CALL !addr, or CALLF !faddr instruction is used, each instruction takes another machine cycle. Therefore, when more importance is attached to RAM utilization or throughput than software compatibility, use the Mk I mode.

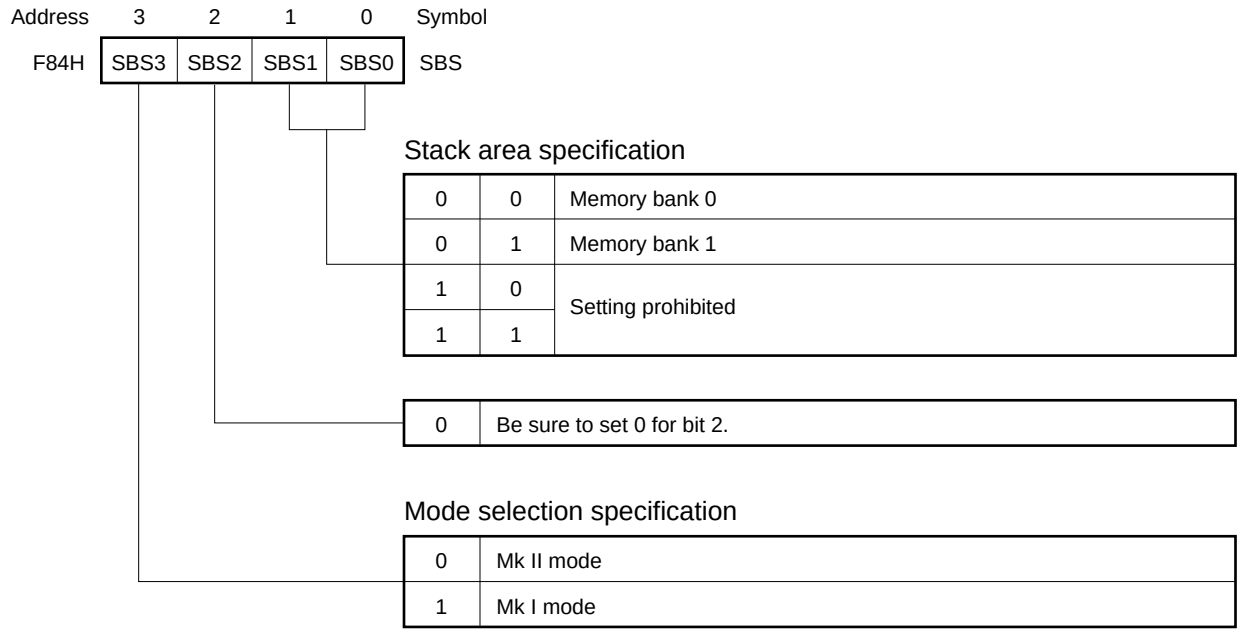
4.2 Setting of Stack Bank Selection (SBS) Register

Use the stack bank selection register to switch between the Mk I mode and the Mk II mode. Figure 4-1 shows the format for doing this.

The stack bank selection register is set using a 4-bit memory manipulation instruction. When using the Mk I mode, be sure to initialize the stack bank selection register to 100×B **Note** at the beginning of the program. When using the Mk II mode, be sure to initialize it to 000×B **Note**.

Note Set the desired value for ×.

Figure 4-1. Format of Stack Bank Selection Register



Caution SBS3 is set to "1" after $\overline{\text{RESET}}$ input, and consequently the CPU operates in the Mk I mode. When using instructions for the Mk II mode, set SBS3 to "0" to enter the Mk II mode before using the instructions.

5. DIFFERENCES BETWEEN μPD75P0116 AND μPD750104, 750106, AND 750108

The μPD75P0116 replaces the internal mask ROM in the μPD750104, 750106, and 750108 with a one-time PROM and features expanded ROM capacity. The μPD75P0116's Mk I mode supports the Mk I mode in the μPD750104, 750106, and 750108 and the μPD75P0116's Mk II mode supports the Mk II mode in the μPD750104, 750106, and 750108.

Table 5-2 lists differences among the μPD75P0116 and the μPD750104, 750106, and 750108. Be sure to check the differences between corresponding versions beforehand, especially when a PROM version is used for debugging or prototype testing of application systems and later the corresponding mask ROM version is used for full-scale production.

Please refer to the **μPD750108 User's Manual (U11330E)** for details on CPU functions and on-chip hardware.

Table 5-1. Differences between μPD75P0116 and μPD750104, 750106, and 750108

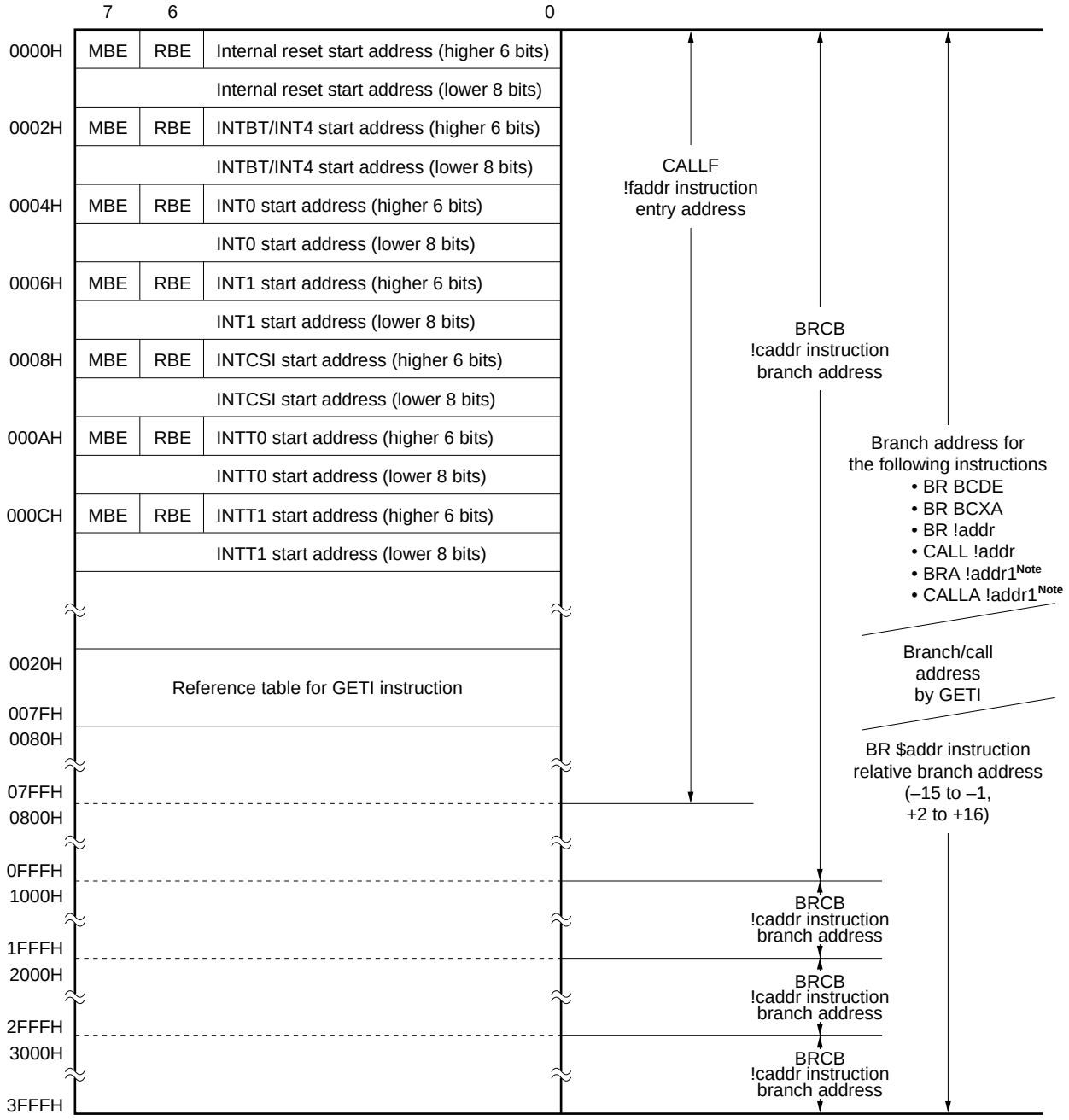
Item		μPD750104	μPD750106	μPD750108	μPD75P0116
Program counter		12-bit	13-bit		14-bit
Program memory (bytes)		Mask ROM 4096	Mask ROM 6144	Mask ROM 8192	One-time PROM 16384
Data memory (× 4 bits)		512			
Mask options	Pull-up resistor for port 4 and port 5	Yes (On-chip/not on-chip can be specified.)			No (On-chip not possible)
	Wait time when releasing STOP mode by interrupt generation	Yes ($2^9/f_{CC}$ or none) Note			No (fixed at $2^9/f_{CC}$) Note
	Feedback resistor for subsystem clock	Yes (can select usable or unusable.)			No (usable)
Pin connection	Pins 6-9 (CU)	P33-P30			P33/MD3-P30/MD0
	Pins 23-26 (GB)				
	Pin 20 (CU)	IC			V_{PP}
	Pin 38 (GB)				
	Pins 34-37 (CU)	P53-P50			P53/D7-P50/D4
	Pins 8-11 (GB)				
	Pins 38-41 (CU)	P43-P40			P43/D3-P40/D0
	Pins 13-16 (GB)				
Other		Noise resistance and noise radiation may differ due to the different circuit complexities and mask layouts.			

Note $2^9/f_{CC}$: 256 μs at 2.0 MHz, 512 μs at 1.0 MHz

Caution Noise resistance and noise radiation are different in PROM version and mask ROM versions. If using a mask ROM version instead of the PROM version for processes between prototype development and full production, be sure to fully evaluate the CS of the mask ROM version (not ES).

6. MEMORY CONFIGURATION

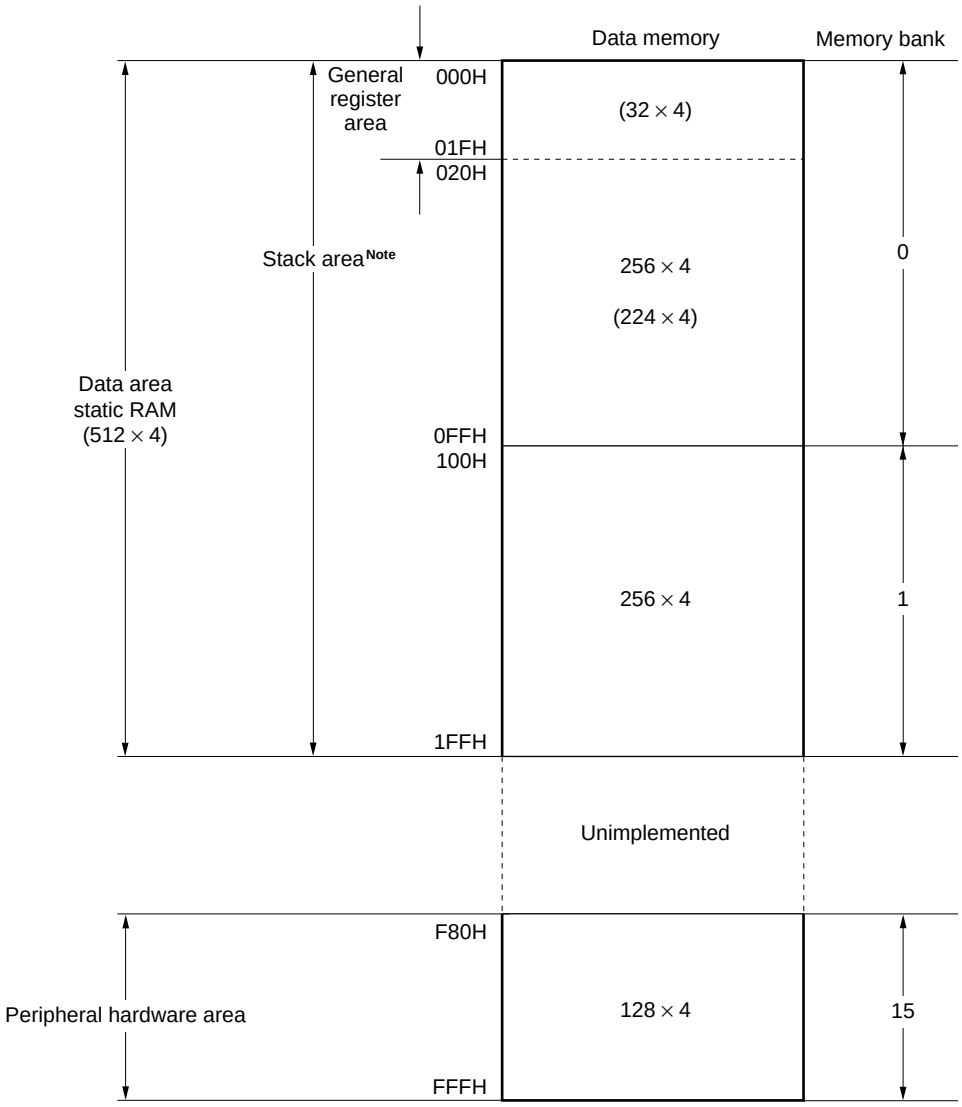
Figure 6-1. Program Memory Map



Note Can be used only at Mk II mode.

Remark For instructions other than those noted above, the “BR PCDE” and “BR PCXA” instructions can be used to branch to addresses with changes in the PC’s lower 8 bits only.

Figure 6-2. Data Memory Map



Note For the stack area, one memory bank can be selected from memory bank 0 or 1.

7. INSTRUCTION SET

(1) Representation and coding formats for operands

In the instruction's operand area, use the following coding format to describe operands corresponding to the instruction's operand representations (for further description, refer to the **RA75X Assembler Package User's Manual - Language (EEU-1363)**). When there are several codes, select and use just one. Upper-case letters, and + and – symbols are key words that should be entered as they are.

For immediate data, enter an appropriate numerical value or label.

Instead of mem, fmem, pmem, bit, etc, a register flag symbol can be described as a label descriptor. (For further description, refer to the **μPD750108 User's Manual (U11330E)**) Labels that can be entered for fmem and pmem are restricted.

Representation	Coding format
reg	X, A, B, C, D, E, H, L
reg1	X, B, C, D, E, H, L
rp	XA, BC, DE, HL
rp1	BC, DE, HL
rp2	BC, DE
rp'	XA, BC, DE, HL, XA', BC', DE', HL'
rp'1	BC, DE, HL, XA', BC', DE', HL'
rpa	HL, HL+, HL–, DE, DL
rpa1	DE, DL
n4	4-bit immediate data or label
n8	8-bit immediate data or label
mem	8-bit immediate data or label Note
bit	2-bit immediate data or label
fmem	FB0H-FBFH, FF0H-FFFH immediate data or label
pmem	FC0H-FFFH immediate data or label
addr	0000H-3FFFH immediate data or label
addr1	0000H-3FFFH immediate data or label (in Mk II mode only)
caddr	12-bit immediate data or label
faddr	11-bit immediate data or label
taddr	20H-7FH immediate data (however, bit0 = 0) or label
PORTn	PORT0-PORT8
IEXXX	IEBT, IECSI, IET0, IET1, IE0-IE2, IE4, IEW
RBn	RB0-RB3
MBn	MB0, MB1, MB15

Note When processing 8-bit data, only even addresses can be specified.

(2) Operation legend

A	: A register; 4-bit accumulator
B	: B register
C	: C register
D	: D register
E	: E register
H	: H register
L	: L register
X	: X register
XA	: Register pair (XA); 8-bit accumulator
BC	: Register pair (BC)
DE	: Register pair (DE)
HL	: Register pair (HL)
XA'	: Expansion register pair (XA')
BC'	: Expansion register pair (BC')
DE'	: Expansion register pair (DE')
HL'	: Expansion register pair (HL')
PC	: Program counter
SP	: Stack pointer
CY	: Carry flag; bit accumulator
PSW	: Program status word
MBE	: Memory bank enable flag
RBE	: Register bank enable flag
PORTn	: Port n (n = 0 to 8)
IME	: Interrupt master enable flag
IPS	: Interrupt priority select register
IE×××	: Interrupt enable flag
RBS	: Register bank select register
MBS	: Memory bank select register
PCC	: Processor clock control register
.	: Delimiter for address and bit
(××)	: Contents of address ××
××H	: Hexadecimal data

(3) Description of symbols used in addressing area

*1	MB = MBE • MBS MBS = 0, 1, 15	Data memory addressing
*2	MB = 0	
*3	MBE = 0 : MB = 0 (000H-07FH) MB = 15 (F80H-FFFH) MBE = 1 : MB = MBS MBS = 0, 1, 15	
*4	MB = 15, fmem = FB0H-FBFH, FF0H-FFFH	
*5	MB = 15, pmem = FC0H-FFFH	
*6	addr = 0000H-3FFFH	Program memory addressing
*7	addr, addr1 = (Current PC) –15 to (Current PC) –1 (Current PC) +2 to (Current PC) +16	
*8	caddr = 0000H-0FFFH ($PC_{13, 12}$ = 00B) or 1000H-1FFFH ($PC_{13, 12}$ = 01B) or 2000H-2FFFH ($PC_{13, 12}$ = 10B) or 3000H-3FFFH ($PC_{13, 12}$ = 11B)	
*9	faddr = 0000H-07FFH	
*10	taddr = 0020H-007FH	
*11	addr1 = 0000H-3FFFH (Mk II mode only)	

Remarks 1. MB indicates access-enabled memory banks.

2. In area *2, MB = 0 for both MBE and MBS.

3. In areas *4 and *5, MB = 15 for both MBE and MBS.

4. Areas *6 to *11 indicate corresponding address-enabled areas.

(4) Description of machine cycles

S indicates the number of machine cycles required for skipping of skip-specified instructions. The value of S varies as shown below.

- No skip ..... S = 0
- Skipped instruction is 1-byte or 2-byte instruction ..... S = 1
- Skipped instruction is 3-byte instruction **Note** ..... S = 2

Note 3-byte instructions: BR !addr, BRA !addr1, CALL !addr, CALLA !addr1

Caution The GETI instruction is skipped for one machine cycle.

One machine cycle equals one cycle (= t_{CY}) of the CPU clock Φ. Use the PCC setting to select among four cycle times.

Group	Mnemonic	Operand	No. of bytes	Machine cycle	Operation	Addressing area	Skip condition
Transfer	MOV	A, # n4	1	1	A ← n4		String-effect A
		reg1, # n4	2	2	reg1 ← n4		
		XA, # n8	2	2	XA ← n8		String-effect A
		HL, # n8	2	2	HL ← n8		String-effect B
		rp2, # n8	2	2	rp2 ← n8		
		A, @HL	1	1	A ← (HL)	*1	
		A, @HL+	1	2 + S	A ← (HL), then L ← L + 1	*1	L = 0
		A, @HL–	1	2 + S	A ← (HL), then L ← L – 1	*1	L = FH
		A, @rpa1	1	1	A ← (rpa1)	*2	
		XA, @HL	2	2	XA ← (HL)	*1	
		@HL, A	1	1	(HL) ← A	*1	
		@HL, XA	2	2	(HL) ← XA	*1	
		A, mem	2	2	A ← (mem)	*3	
		XA, mem	2	2	XA ← (mem)	*3	
		mem, A	2	2	(mem) ← A	*3	
		mem, XA	2	2	(mem) ← XA	*3	
		A, reg	2	2	A ← reg		
		XA, rp’	2	2	XA ← rp’		
		reg1, A	2	2	reg1 ← A		
		rp’1, XA	2	2	rp’1 ← XA		
	XCH	A, @HL	1	1	A ↔ (HL)	*1	
		A, @HL+	1	2 + S	A ↔ (HL), then L ← L + 1	*1	L = 0
		A, @HL–	1	2 + S	A ↔ (HL), then L ← L – 1	*1	L = FH
		A, @rpa1	1	1	A ↔ (rpa1)	*2	
		XA, @HL	2	2	XA ↔ (HL)	*1	
		A, mem	2	2	A ↔ (mem)	*3	
		XA, mem	2	2	XA ↔ (mem)	*3	
		A, reg1	1	1	A ↔ reg1		
		XA, rp’	2	2	XA ↔ rp’		
Table reference	MOVT	XA, @PCDE	1	3	XA ← $(PC_{13-8} + DE)_{ROM}$		
		XA, @PCXA	1	3	XA ← $(PC_{13-8} + XA)_{ROM}$		
		XA, @BCDE	1	3	XA ← $(BCDE)_{ROM}$ **Note**	*6	
		XA, @BCXA	1	3	XA ← $(BCXA)_{ROM}$ **Note**	*6	

Note As for the B register, only the lower 2 bits are valid.

Group	Mnemonic	Operand	No. of bytes	Machine cycle	Operation	Addressing area	Skip condition
Bit transfer	MOV1	CY, fmem.bit	2	2	CY ← (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← ($pmem_{7-2}$ + L_{3-2}.bit(L_{1-0}))	*5	
		CY, @H + mem.bit	2	2	CY ← (H + mem_{3-0}.bit)	*1	
		fmem.bit, CY	2	2	(fmem.bit) ← CY	*4	
		pmem.@L, CY	2	2	($pmem_{7-2}$ + L_{3-2}.bit(L_{1-0})) ← CY	*5	
		@H + mem.bit, CY	2	2	(H + mem_{3-0}.bit) ← CY	*1	
Operation	ADDS	A, #n4	1	1 + S	A ← A + n4		carry
		XA, #n8	2	2 + S	XA ← XA + n8		carry
		A, @HL	1	1 + S	A ← A + (HL)	*1	carry
		XA, rp'	2	2 + S	XA ← XA + rp'		carry
		rp'1, XA	2	2 + S	rp'1 ← rp'1 + XA		carry
	ADDC	A, @HL	1	1	A, CY ← A + (HL) + CY	*1	
		XA, rp'	2	2	XA, CY ← XA + rp' + CY		
		rp'1, XA	2	2	rp'1, CY ← rp'1 + XA + CY		
	SUBS	A, @HL	1	1 + S	A ← A – (HL)	*1	borrow
		XA, rp'	2	2 + S	XA ← XA – rp'		borrow
		rp'1, XA	2	2 + S	rp'1 ← rp'1 – XA		borrow
	SUBC	A, @HL	1	1	A, CY ← A – (HL) – CY	*1	
		XA, rp'	2	2	XA, CY ← XA – rp' – CY		
		rp'1, XA	2	2	rp'1, CY ← rp'1 – XA – CY		
	AND	A, #n4	2	2	A ← A ∧ n4		
		A, @HL	1	1	A ← A ∧ (HL)	*1	
		XA, rp'	2	2	XA ← XA ∧ rp'		
		rp'1, XA	2	2	rp'1 ← rp'1 ∧ XA		
	OR	A, #n4	2	2	A ← A ∨ n4		
		A, @HL	1	1	A ← A ∨ (HL)	*1	
		XA, rp'	2	2	XA ← XA ∨ rp'		
		rp'1, XA	2	2	rp'1 ← rp'1 ∨ XA		
	XOR	A, #n4	2	2	A ← A ∀ n4		
		A, @HL	1	1	A ← A ∀ (HL)	*1	
		XA, rp'	2	2	XA ← XA ∀ rp'		
		rp'1, XA	2	2	rp'1 ← rp'1 ∀ XA		

Group	Mnemonic	Operand	No. of bytes	Machine cycle	Operation	Addressing area	Skip condition
Accumulator	RORC	A	1	1	$CY \leftarrow A_0$, $A_3 \leftarrow CY$, $A_{n-1} \leftarrow A_n$		
manipulate	NOT	A	2	2	$A \leftarrow \overline{A}$		
Increment/	INCS	reg	1	1 + S	reg ← reg + 1		reg = 0
decrement		rp1	1	1 + S	rp1 ← rp1 + 1		rp1 = 00H
		@HL	2	2 + S	(HL) ← (HL) + 1	*1	(HL) = 0
		mem	2	2 + S	(mem) ← (mem) + 1	*3	(mem) = 0
	DECS	reg	1	1 + S	reg ← reg – 1		reg = FH
		rp’	2	2 + S	rp’ ← rp’ – 1		rp’ = FFH
Compare	SKE	reg, #n4	2	2 + S	Skip if reg = n4		reg = n4
		@HL, #n4	2	2 + S	Skip if (HL) = n4	*1	(HL) = n4
		A, @HL	1	1 + S	Skip if A = (HL)	*1	A = (HL)
		XA, @HL	2	2 + S	Skip if XA = (HL)	*1	XA = (HL)
		A, reg	2	2 + S	Skip if A = reg		A = reg
		XA, rp’	2	2 +S	Skip if XA = rp’		XA = rp’
Carry flag	SET1	CY	1	1	CY ← 1		
manipulate	CLR1	CY	1	1	CY ← 0		
	SKT	CY	1	1 + S	Skip if CY = 1		CY = 1
	NOT1	CY	1	1	$CY \leftarrow \overline{CY}$		

Group	Mnemonic	Operand	No. of bytes	Machine cycle	Operation	Addressing area	Skip condition
Memory bit manipulate	SET1	mem.bit	2	2	(mem.bit) ← 1	*3	
		fmem.bit	2	2	(fmem.bit) ←1	*4	
		pmem.@L	2	2	(pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$)) ← 1	*5	
		@H + mem.bit	2	2	(H + mem$_{3-0}$.bit) ← 1	*1	
	CLR1	mem.bit	2	2	(mem.bit) ← 0	*3	
		fmem.bit	2	2	(fmem.bit) ← 0	*4	
		pmem.@L	2	2	(pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$)) ← 0	*5	
		@H + mem.bit	2	2	(H + mem$_{3-0}$.bit) ← 0	*1	
	SKT	mem.bit	2	2 + S	Skip if(mem.bit) = 1	*3	(mem.bit) = 1
		fmem.bit	2	2 + S	Skip if(fmem.bit) = 1	*4	(fmem.bit) = 1
		pmem.@L	2	2 + S	Skip if(pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$)) = 1	*5	(pmem.@L) = 1
		@H + mem.bit	2	2 + S	Skip if(H + mem$_{3-0}$.bit) = 1	*1	(@H + mem.bit) = 1
	SKF	mem.bit	2	2 + S	Skip if(mem.bit) = 0	*3	(mem.bit) = 0
		fmem.bit	2	2 + S	Skip if(fmem.bit) = 0	*4	(fmem.bit) = 0
		pmem.@L	2	2 + S	Skip if(pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$)) = 0	*5	(pmem.@L) = 0
		@H + mem.bit	2	2 + S	Skip if(H + mem$_{3-0}$.bit) = 0	*1	(@H + mem.bit) = 0
	SKTCLR	fmem.bit	2	2 + S	Skip if(fmem.bit) = 1 and clear	*4	(fmem.bit) = 1
		pmem.@L	2	2 + S	Skip if(pmem$_{7-2}$ + L$_{3-2}$.bit (L$_{1-0}$)) = 1 and clear	*5	(pmem.@L) = 1
		@H + mem.bit	2	2 + S	Skip if(H + mem$_{3-0}$.bit) = 1 and clear	*1	(@H + mem.bit) = 1
	AND1	CY, fmem.bit	2	2	CY ← CY ∧ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ∧ (pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY, @H + mem.bit	2	2	CY ← CY ∧ (H + mem$_{3-0}$.bit)	*1	
	OR1	CY, fmem.bit	2	2	CY ← CY ∨ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ∨ (pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY, @H + mem.bit	2	2	CY ← CY ∨ (H + mem$_{3-0}$.bit)	*1	
	XOR1	CY, fmem.bit	2	2	CY ← CY ∀ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ∀ (pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY, @H + mem.bit	2	2	CY ← CY ∀ (H + mem$_{3-0}$.bit)	*1	

Group	Mnemonic	Operand	No. of bytes	Machine cycle	Operation	Addressing area	Skip condition
Branch	BR Note 1	addr	—	—	$PC_{13-0} \leftarrow$ addr (Assembler selects the most appropriate instruction among the following: • BR !addr • BRCB !caddr • BR $addr)	*6	
		addr1	—	—	$PC_{13-0} \leftarrow$ addr1 (Assembler selects the most appropriate instruction among the following: • BRA !addr1 • BR !addr • BRCB !caddr • BR $addr1)	*11	
		!addr	3	3	$PC_{13-0} \leftarrow$ addr	*6	
		$addr	1	2	$PC_{13-0} \leftarrow$ addr	*7	
		$addr1	1	2	$PC_{13-0} \leftarrow$ addr1		
		PCDE	2	3	$PC_{13-0} \leftarrow PC_{13-8}$ + DE		
		PCXA	2	3	$PC_{13-0} \leftarrow PC_{13-8}$ + XA		
		BCDE	2	3	$PC_{13-0} \leftarrow$ BCDE Note 2	*6	
		BCXA	2	3	$PC_{13-0} \leftarrow$ BCXA Note 2	*6	
	BRA Note 1	!addr1	3	3	$PC_{13-0} \leftarrow$ addr1	*11	
	BRCB	!caddr	2	2	$PC_{13-0} \leftarrow PC_{13, 12}$ + $caddr_{11-0}$	*8	

Notes 1. Shaded areas indicate support for the Mk II mode only. Other areas indicate support for the Mk I mode only.

2. As for the B register, only the lower 2 bits are valid.

Group	Mnemonic	Operand	No. of bytes	Machine cycle	Operation	Addressing area	Skip condition
Subroutine stack control	CALLA Note	!addr1	3	3	(SP – 5) ← 0, 0, $PC_{13,12}$ (SP – 6)(SP – 3)(SP – 4) ← PC_{11-0} (SP – 2) ← ×, ×, MBE, RBE PC_{13-0} ← addr1, SP ← SP – 6	*11	
	CALL Note	!addr	3	3	(SP – 4)(SP – 1)(SP – 2) ← PC_{11-0} (SP – 3) ← (MBE, RBE, $PC_{13, 12}$) PC_{13-0} ← addr, SP ← SP – 4	*6	
				4	(SP – 5) ← 0, 0, $PC_{13,12}$ (SP – 6)(SP – 3)(SP – 4) ← PC_{11-0} (SP – 2) ← ×, ×, MBE, RBE PC_{13-0} ← addr, SP ← SP – 6		
	CALLF Note	!faddr	2	2	(SP – 4)(SP – 1)(SP – 2) ← PC_{11-0} (SP – 3) ← (MBE, RBE, $PC_{13, 12}$) PC_{13-0} ← 000 + faddr, SP ← SP – 4	*9	
				3	(SP – 5) ← 0, 0, $PC_{13,12}$ (SP – 6)(SP – 3)(SP – 4) ← PC_{11-0} (SP – 2) ← ×, ×, MBE, RBE PC_{13-0} ← 000 + faddr,SP ← SP – 6		
	RET Note		1	3	(MBE, RBE, $PC_{13, 12}$) ← (SP + 1) PC_{11-0} → (SP)(SP + 3)(SP + 2) SP ← SP + 4		
					×, ×, MBE, RBE ← (SP + 4) 0, 0, PC_{13-12} ← (SP + 1) PC_{11-0} ← (SP)(SP + 3)(SP + 2) SP ← SP + 6		
	RETS Note		1	3 + S	(MBE, RBE, $PC_{13, 12}$) ← (SP + 1) PC_{11-0} ← (SP)(SP + 3)(SP + 2) SP ← SP + 4 then skip unconditionally		Unconditional
					×, ×, MBE, RBE ← (SP + 4) 0, 0, PC_{13-12} ← (SP + 1) PC_{11-0} ← (SP)(SP + 3)(SP + 2) SP ← SP + 6 then skip unconditionally		
	RETI Note		1	3	MBE, RBE, $PC_{13, 12}$ ← (SP + 1) PC_{11-0} ← (SP)(SP + 3)(SP + 2) PSW ← (SP + 4)(SP + 5), SP ← SP + 6		
					0, 0, $PC_{13, 12}$ ← (SP + 1) PC_{11-0} ← (SP)(SP + 3)(SP + 2) PSW ← (SP + 4)(SP + 5), SP ← SP + 6		

Note Shaded areas indicate support for the Mk II mode only. Other areas indicate support for the Mk I mode only.

Group	Mnemonic	Operand	No. of bytes	Machine cycle	Operation	Addressing area	Skip condition
Subroutine stack control	PUSH	rp	1	1	(SP – 1)(SP – 2) ← rp, SP ← SP – 2		
		BS	2	2	(SP – 1) ← MBS, (SP – 2) ← RBS, SP ← SP – 2		
	POP	rp	1	1	rp ← (SP + 1)(SP), SP ← SP + 2		
		BS	2	2	MBS ← (SP + 1), RBS ← (SP), SP ← SP + 2		
Interrupt control	EI		2	2	IME(IPS.3) ← 1		
		IE×××	2	2	IE××× ← 1		
	DI		2	2	IME(IPS.3) ← 0		
		IE×××	2	2	IE××× ← 0		
I/O	IN **Note 1**	A, PORTn	2	2	A ← PORTn (n = 0 - 8)		
		XA, PORTn	2	2	XA ← PORTn+1, PORTn (n = 4, 6)		
	OUT **Note 1**	PORTn, A	2	2	PORTn ← A (n = 2 - 8)		
		PORTn, XA	2	2	PORTn+1, PORTn ← XA (n = 4, 6)		
CPU control	HALT		2	2	Set HALT Mode(PCC.2 ← 1)		
	STOP		2	2	Set STOP Mode(PCC.3 ← 1)		
	NOP		1	1	No Operation		
Special	SEL	RBn	2	2	RBS ← n (n = 0 - 3)		
		MBn	2	2	MBS ← n (n = 0, 1, 15)		
	GETI **Note 2, 3**	taddr	1	3	• When using TBR instruction PC13-0 ← (taddr)5-0 + (taddr + 1)	*10	
					• When using TCALL instruction (SP – 4)(SP – 1)(SP – 2) ← PC11-0 (SP – 3) ← MBE, RBE, PC13, 12 PC13-0 ← (taddr)5-0 + (taddr + 1) SP ← SP – 4		
					• When using instruction other than TBR or TCALL Execute (taddr)(taddr + 1) instructions		Determined by referenced instruction
			1	3	• When using TBR instruction PC13-0 ← (taddr)5-0 + (taddr + 1)	*10	
				4	• When using TCALL instruction (SP – 5) ← 0, 0, PC13, 12 (SP – 6)(SP – 3)(SP – 4) ← PC11-0 (SP – 2) ← ×, ×, MBE, RBE PC13-0 ← (taddr)5-0 + (taddr + 1) SP ← SP – 6		
				3	• When using instruction other than TBR or TCALL Execute (taddr)(taddr + 1) instructions		Determined by referenced instruction

Notes 1. Before executing the IN or OUT instruction, set MBE to 0 or 1 and set MBS to 15.

2. TBR and TCALL are assembler directives for the GETI instruction's table definitions.

3. Shaded areas indicate support for the Mk II mode only. Other areas indicate support for the Mk I mode only.

8. ONE-TIME PROM (PROGRAM MEMORY) WRITE AND VERIFY

The program memory in the μPD75P0116 is a 16384 × 8-bit electronic write-enabled one-time PROM. The pins listed in the table below are used for this PROM's write/verify operations. Clock input from the CL1 pins is used instead of address input as a method for updating addresses.

Pin name	Function
V_{PP}	Pin (usually V_{DD}) where programming voltage is applied during program memory write/verify
CL1, CL2	Clock input to the CL1 pin for address updating during program memory write/verify. Leave the CL2 pin open.
MD0/P30-MD3/P33	Operation mode selection pin for program memory write/verify
D0/P40-D3/P43 (lower 4) D4/P50-D7/P53 (higher 4)	8-bit data I/O pin for program memory write/verify
V_{DD}	Pin where power supply voltage is applied. Power voltage range for normal operation is 1.8 to 5.5 V. Apply 6.0 V for program memory write/verify.

Caution Pins not used for program memory write/verify should be processed as follows.

- **All unused pins except XT2 ..... Connect to Vss via a pull-down resistor**
- **XT2 pin ..... Leave open**

8.1 Operation Modes for Program Memory Write/Verify

When +6 V is applied to the μPD75P0116's V_{DD} pin and +12.5 V is applied to its V_{PP} pin, program write/verify modes are in effect. Furthermore, the following detailed operation modes can be specified by setting pins MD0 to MD3 as shown below.

Operation mode specification						Operation mode
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
+12.5 V	+6 V	H	L	H	L	Zero-clear program memory address
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	×	H	H	Program inhibit mode

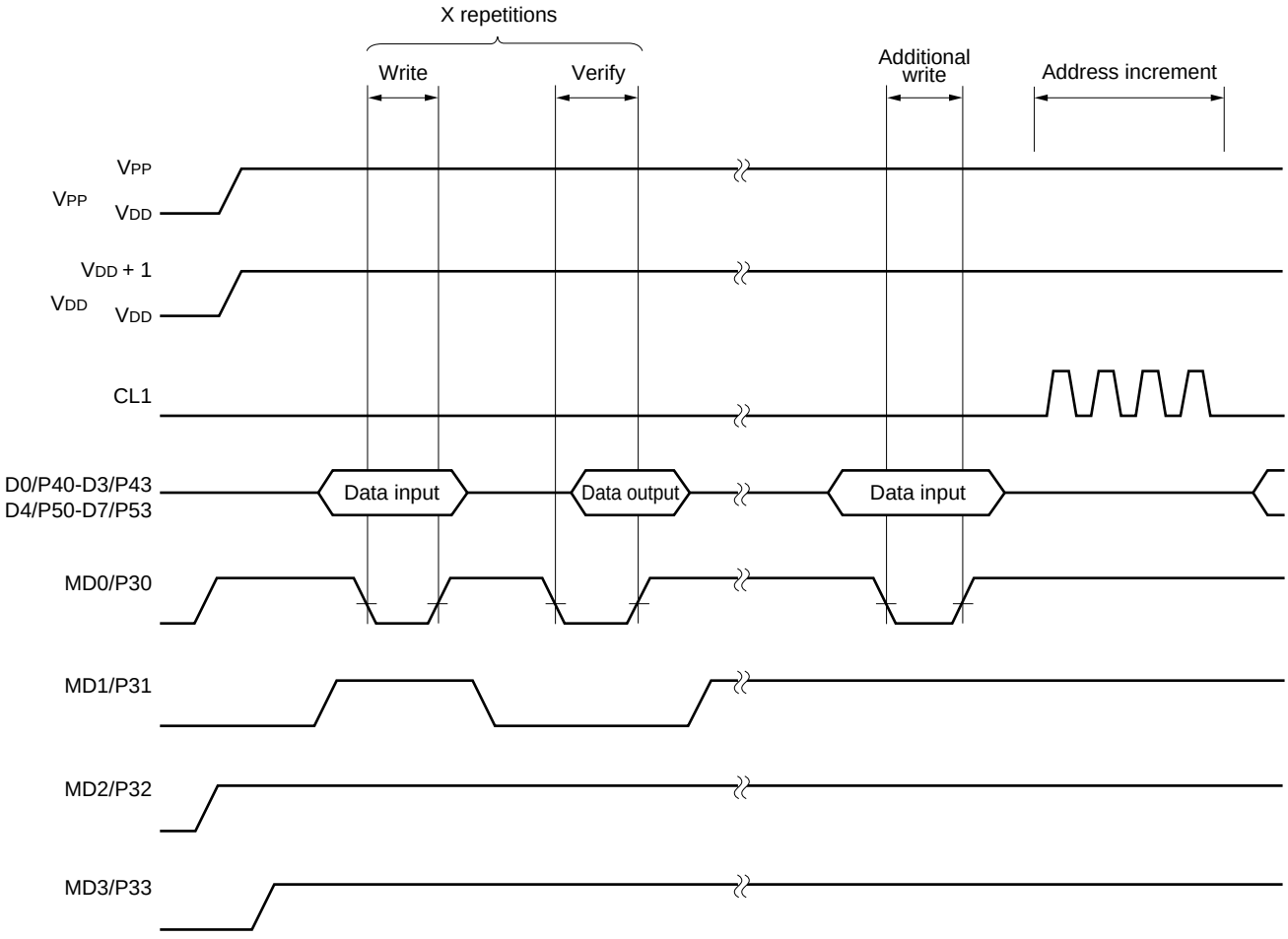
Remark ×: L or H

8.2 Steps in Program Memory Write Operation

High-speed program memory write can be executed via the following steps.

(1) Pull down unused pins to V_{SS} via resistors. Set the CL1 pin to low.
(2) Apply +5 V to the V_{DD} and V_{PP} pins.
(3) Wait 10 μs.
(4) Zero-clear mode for program memory addresses.
(5) Apply +6 V to V_{DD} and +12.5 V power to V_{PP}.
(6) Write data using 1-ms write mode.
(7) Verify mode. If write is verified, go to step (8) and if write is not verified, go back to steps (6) and (7).
(8) X [= number of write operations from steps (6) and (7)] × 1 ms additional write
(9) 4 pulse inputs to the CL1 pin updates (increments +1) the program memory address.
(10) Repeat steps (6) to (9) until the last address is completed.
(11) Zero-clear mode for program memory addresses.
(12) Apply +5 V to the V_{DD} and V_{PP} pins.
(13) Power supply OFF

The following diagram illustrates steps (2) to (9).

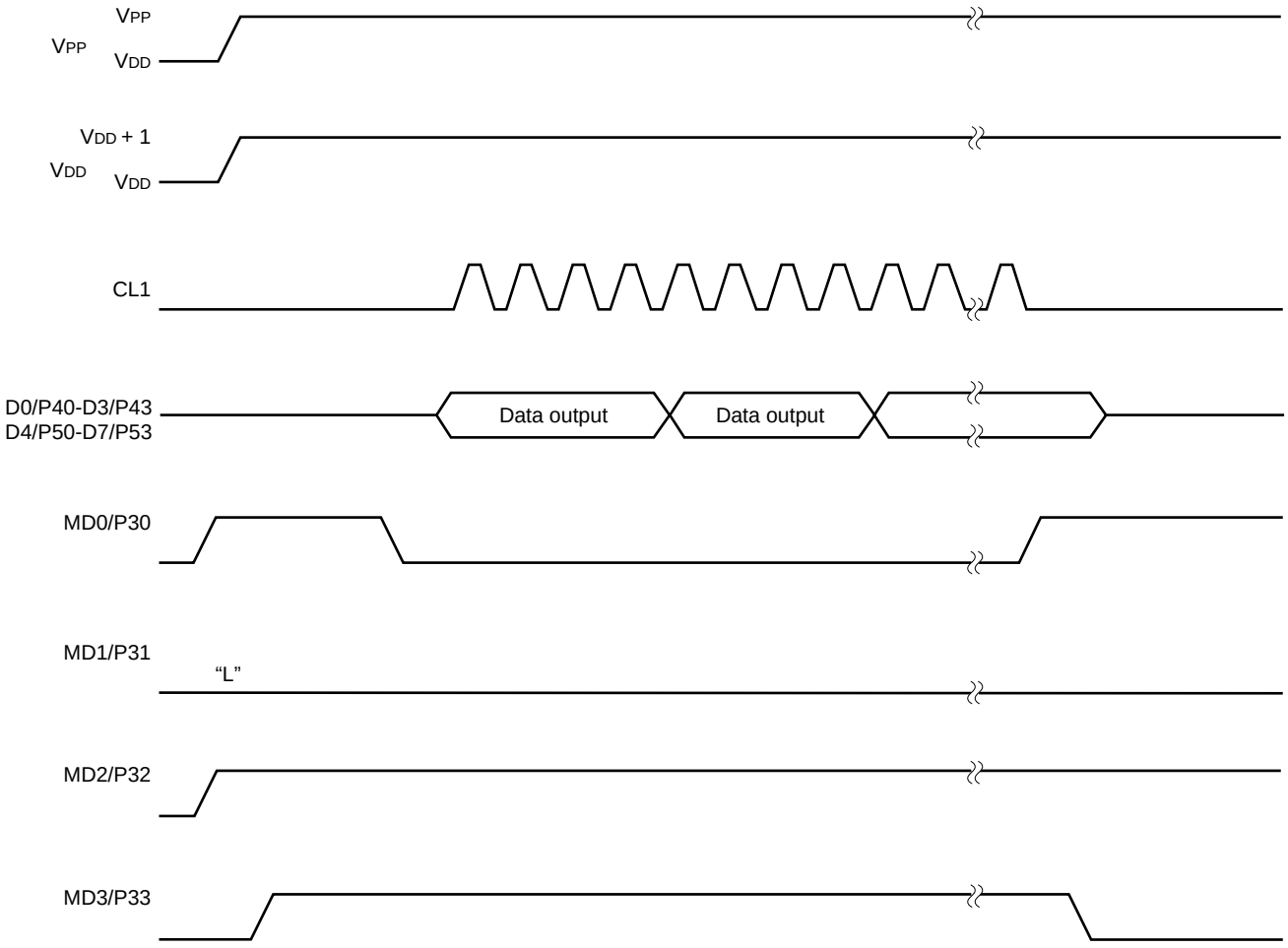


8.3 Steps in Program Memory Read Operation

The μPD75P0116 can read out the program memory contents via the following steps.

(1) Pull down unused pins to V_{SS} via resistors. Set the CL1 pin to low.
(2) Apply +5 V to the V_{DD} and V_{PP} pins.
(3) Wait 10 μs.
(4) Zero-clear mode for program memory addresses.
(5) Apply +6 V power to V_{DD} and +12.5 V to V_{PP}.
(6) Verify mode. When a clock pulse is input to the CL1 pin, data is output sequentially to one address at a time based on a cycle of four pulse inputs.
(7) Zero-clear mode for program memory addresses.
(8) Apply +5 V power to the V_{DD} and V_{PP} pins.
(9) Power supply OFF

The following diagram illustrates steps (2) to (7).



8.4 One-Time PROM Screening

Due to its structure, the one-time PROM cannot be fully tested before shipment by NEC. Therefore, NEC recommends the screening process, that is, after the required data is written to the PROM and the PROM is stored under the high-temperature conditions shown below, the PROM should be verified.

Storage temperature	Storage time
125 ˚C	24 hours

9. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25 °C)

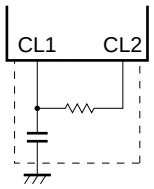
Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.3 to +7.0	V
PROM supply voltage	V_{PP}		–0.3 to + 13.5	V
Input voltage	V_{I1}	Other than ports 4, 5	–0.3 to V_{DD} +0.3	V
	V_{I2}	Ports 4, 5 (N-ch open drain)	–0.3 to + 14	V
Output voltage	V_O		–0.3 to V_{DD} + 0.3	V
High-level output current	I_{OH}	Per pin	–10	mA
		Total of all pins	–30	mA
Low-level output current	I_{OL}	Per pin	30	mA
		Total of all pins	220	mA
Operating ambient temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution If the absolute maximum rating of even one of the parameters is exceeded even momentarily, the quality of the product may be degraded. The absolute maximum ratings are therefore values which, when exceeded, can cause the product to be damaged. Be sure that these values are never exceeded when using the product.

Capacitance (T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz			15	pF
Output capacitance	C_{OUT}	Pins other than tested pins: 0 V			15	pF
I/O capacitance	C_{IO}				15	pF

Main System Clock Oscillation Circuit Characteristics (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended constants	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
RC oscillation		Oscillation frequency (f_{CC}) **Note**		0.4		2.0	MHz

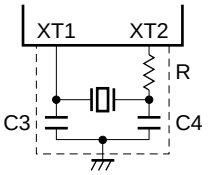
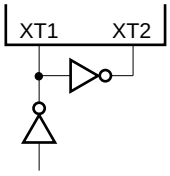
Note The oscillation frequency shown above indicates characteristics of the oscillation circuit only. For the instruction execution time and oscillation frequency characteristics, refer to **AC Characteristics**.

Caution When using the main system clock oscillation circuit, wire the portion enclosed in the dotted line in the above figure as follows to prevent adverse influences due to wiring capacitance:

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with other signal lines.**
- **Do not route the wiring in the vicinity of a line through which a high alternating current flows.**
- **Always keep the ground point of the capacitor of the oscillation circuit at the same potential as V_{DD}.**

  Do not ground to a power supply pattern through which a high current flows.
- **Do not extract signals from the oscillation circuit.**

Subsystem Clock Oscillation Circuit Characteristics (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended constants	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT}) **Note 1**		32	32.768	35	kHz
		Oscillation stabilization time **Note 2**	V_{DD} = 4.5 to 5.5 V		1.0	2	s
						10	s
External clock		XT1 input frequency (f_{XT}) **Note 1**		32		100	kHz
		XT1 input high-, low-level widths (t_{XTH}, t_{XTL})		5		15	μs

Notes 1. The oscillation frequency shown above indicate characteristics of the oscillation circuit only. For the instruction execution time, refer to **AC Characteristics**.

2. The oscillation stabilization time is the time required for oscillation to be stabilized after V_{DD} has been applied.

Caution When using the subsystem clock oscillation circuit, wire the portion enclosed in the dotted line in the above figure as follows to prevent adverse influences due to wiring capacitance:

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with other signal lines.**
- **Do not route the wiring in the vicinity of a line through which a high alternating current flows.**
- **Always keep the ground point of the capacitor of the oscillation circuit at the same potential as V_{DD}.**
  Do not ground to a power supply pattern through which a high current flows.
- **Do not extract signals from the oscillation circuit.**

The subsystem clock oscillation circuit has a low amplification factor to reduce current dissipation and is more susceptible to noise than the main system clock oscillation circuit. Therefore, exercise utmost care in wiring the subsystem clock oscillation circuit.

DC Characteristics (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-level output current	I_{OL}	Per pin				15	mA
		Total of all pins				150	mA
High-level input voltage	V_{IH1}	Ports 2, 3, 8	2.7 ≤ V_{DD} ≤ 5.5 V	0.7 V_{DD}		V_{DD}	V
			1.8 ≤ V_{DD} ≤ 2.7 V	0.9 V_{DD}		V_{DD}	V
	V_{IH2}	Ports 0, 1, 6, 7, $\overline{\text{RESET}}$	2.7 ≤ V_{DD} ≤ 5.5 V	0.8 V_{DD}		V_{DD}	V
			1.8 ≤ V_{DD} ≤ 2.7 V	0.9 V_{DD}		V_{DD}	V
	V_{IH3}	Ports 4, 5 (N-ch open drain)	2.7 ≤ V_{DD} ≤ 5.5 V	0.7 V_{DD}		13	V
			1.8 ≤ V_{DD} ≤ 2.7 V	0.9 V_{DD}		13	V
	V_{IH4}	XT1		V_{DD}–0.1		V_{DD}	V
Low-level input voltage	V_{IL1}	Ports 2-5, 8	2.7 ≤ V_{DD} ≤ 5.5 V	0		0.3 V_{DD}	V
			1.8 ≤ V_{DD} ≤ 2.7 V	0		0.1 V_{DD}	V
	V_{IL2}	Ports 0, 1, 6, 7, $\overline{\text{RESET}}$	2.7 ≤ V_{DD} ≤ 5.5 V	0		0.2 V_{DD}	V
			1.8 ≤ V_{DD} ≤ 2.7 V	0		0.1 V_{DD}	V
	V_{IL3}	XT1		0		0.1	V
High-level output voltage	V_{OH}	$\overline{\text{SCK}}$, SO, ports 2, 3, 6-8 I_{OH} = –1.0 mA		V_{DD}–0.5			V
Low-level output voltage	V_{OL1}	$\overline{\text{SCK}}$, SO, ports 2-8	I_{OL} = 15 mA, V_{DD} = 5.0 V ± 10 %		0.2	2.0	V
			I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1	N-ch open drain Pull-up resistor ≥ 1 kΩ			0.2 V_{DD}	V
High-level input leakage current	I_{LIH1}	V_{IN} = V_{DD}	Pins other than XT1			3	μA
	I_{LIH2}		XT1			20	μA
	I_{LIH3}	V_{IN} = 13 V	Ports 4, 5 (N-ch open drain)			20	μA
Low-level input leakage current	I_{LIL1}	V_{IN} = 0 V	Pins other than ports 4, 5, XT1			–3	μA
	I_{LIL2}		XT1			–20	μA
	I_{LIL3}		Ports 4, 5 (N-ch open drain) When input instruction is not executed			–3	μA
			Ports 4, 5 (N-ch open drain) When input instruction is executed			–30	μA
			V_{DD} = 5.0 V		–10	–27	μA
			V_{DD} = 3.0 V		–3	–8	μA
High-level output leakage current	I_{LOH1}	V_{OUT} = V_{DD}	$\overline{\text{SCK}}$, SO/SB0, SB1, Ports 2, 3, 6-8			3	μA
	I_{LOH2}	V_{OUT} = 13 V	Ports 4, 5 (N-ch open drain)			20	μA
Low-level output leakage current	I_{LOL}	V_{OUT} = 0 V				–3	μA
Internal pull-up resistor	R_L	V_{IN} = 0 V	Ports 0-3, 6-8 (except P00 pin)	50	100	200	kΩ

DC Characteristics (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	1.0 MHz Note 2 RC oscillation R = 22 kΩ, C = 22 pF	V_{DD} = 5.0 V ± 10 % Note 3			0.9	1.8	mA
			V_{DD} = 3.0 V ± 10 % Note 4			250	500	μA
	I_{DD2}		HALT mode	V_{DD} = 5.0 V ± 10 %		370	920	μA
				V_{DD} = 3.0 V ± 10 %		170	340	μA
	I_{DD3}	32.768 kHz Note 5 crystal oscillation	Low-voltage mode Note 6	V_{DD} = 3.0 V ± 10 %		55.0	200	μA
				V_{DD} = 2.0 V ± 10 %		22.0	70.0	μA
				V_{DD} = 3.0 V, T_A = 25 °C		55.0	90.0	μA
			Low current dissipation mode Note 7	V_{DD} = 3.0 V ± 10 %		50.0	150	μA
				V_{DD} = 3.0 V, T_A = 25 °C		50.0	85.0	μA
	I_{DD4}		HALT mode	Low-voltage mode Note 6	V_{DD} = 3.0 V ± 10 %	5.0	30.0	μA
					V_{DD} = 2.0 V ± 10 %	2.5	10.0	μA
					V_{DD} = 3.0 V, T_A = 25 °C	5.0	10.0	μA
				Low current consumption mode Note 7	V_{DD} = 3.0 V ± 10 %	4.0	15.0	μA
					V_{DD} = 3.0 V, T_A = 25 °C	4.0	7.0	μA
	I_{DD5}	XT1 = 0V Note 8 STOP mode	V_{DD} = 5.0 V ± 10 %			0.05	5.0	μA
			V_{DD} = 3.0 V ± 10 %			0.02	2.5	μA
				T_A = 25 °C		0.02	0.2	μA

Notes 1. The current flowing through the internal pull-up resistor is not included.

2. Including the case when the subsystem clock oscillates.

3. When the device operates in high-speed mode with the processor clock control register (PCC) set to 0011.

4. When the device operates in low-speed mode with PCC set to 0000.

5. When the device operates on the subsystem clock, with the system clock control register (SCC) set to 1001 and oscillation of the main system clock stopped.

6. When the suboscillation circuit control register (SOS) is set to 0000.

7. When SOS is set to 0010.

8. When SOS is set to 00×1, and the suboscillation circuit feedback resistor is not used (×: don't care).

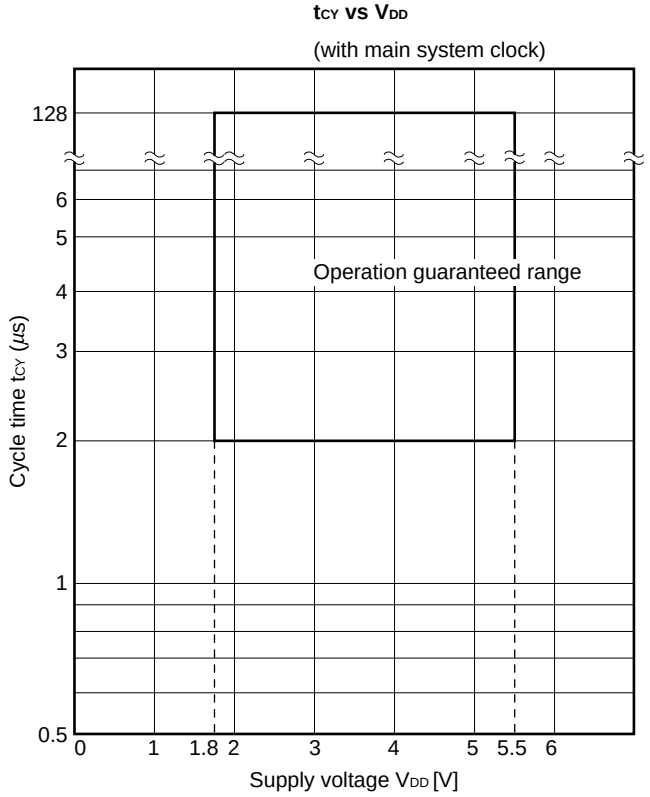
AC Characteristics (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
CPU clock cycle time[Note 1] (minimum instruction execution time = 1 machine cycle)	t_{CY}	Operates with main system clock		2.0		128	μs
		Operates with subsystem clock		114	122	125	μs
TI0 input frequency	f_{TI}	V_{DD} = 2.7 to 5.5 V		0		1.0	MHz
				0		275	kHz
TI0 high-, low-level widths	t_{TIH}, t_{TIL}	V_{DD} = 2.7 to 5.5 V		0.48			μs
				1.8			μs
Interrupt input high-, low-level widths	t_{INTH}, t_{INTL}	INT0	IM02 = 0	**Note 2**			μs
			IM02 = 1	10			μs
		INT1, 2, 4		10			μs
		KR0-KR7		10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			μs
RC oscillation frequency	f_{CC}	R = 22 kΩ, C = 22 pF	V_{DD} = 2.7 to 5.5 V	0.9	1.0	1.3	MHz
			V_{DD} = 1.8 to 5.5 V	0.55	1.0	1.3	MHz

Notes 1. The cycle time of the CPU clock (φ) (minimum instruction execution time) when the device operates with the main system clock is determined by the time constant of the connected resistor (R) and capacitor (C), and the value of the processor clock control register (PCC). When the device operates with the subsystem clock, the cycle time of the CPU clock (φ) is determined by the oscillation frequency of the connected oscillator (and external clock), and the values of the system clock control register (SCC) and processor clock control register (PCC).

The figure on the below shows the supply voltage V_{DD} vs. cycle time t_{CY} characteristics when the device operates with the main system clock.

2. $2t_{CY}$ or $128/f_{CC}$ depending on the setting of the interrupt mode register (IM0).



Serial Transfer Operation

2-wire and 3-wire serial I/O modes ($\overline{SCK}$ ⋯ internal clock output): (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY1}	V_{DD} = 2.7 to 5.5 V		1300			ns
				3800			ns
$\overline{SCK}$ high-, low-level widths	t_{KL1},	V_{DD} = 2.7 to 5.5 V		t_{KCY1}/2–50			ns
	t_{KH1}			t_{KCY1}/2–150			ns
SI**Note 1** setup time	t_{SIK1}	V_{DD} = 2.7 to 5.5 V		150			ns
(vs. $\overline{SCK}$ ↑)				500			ns
SI**Note 1** hold time	t_{KSI1}	V_{DD} = 2.7 to 5.5 V		400			ns
(vs. $\overline{SCK}$ ↑)				600			ns
$\overline{SCK}$ ↓ → SO**Note 1** output	t_{KSO1}	R_L = 1 kΩ**Note 2**	V_{DD} = 2.7 to 5.5 V	0		250	ns
delay time		C_L = 100 pF		0		1000	ns

Notes 1. Read as SB0 or SB1 when using the 2-wire serial I/O mode.

2. R_L and C_L respectively indicate the load resistance and load capacitance of the SO output line.

2-wire and 3-wire serial I/O modes ($\overline{SCK}$ ⋯ external clock input): (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY2}	V_{DD} = 2.7 to 5.5 V		800			ns
				3200			ns
$\overline{SCK}$ high-, low-level widths	t_{KL2},	V_{DD} = 2.7 to 5.5 V		400			ns
	t_{KH2}			1600			ns
SI**Note 1** setup time	t_{SIK2}	V_{DD} = 2.7 to 5.5 V		100			ns
(vs. $\overline{SCK}$ ↑)				150			ns
SI**Note 1** hold time	t_{KSI2}	V_{DD} = 2.7 to 5.5 V		400			ns
(vs. $\overline{SCK}$ ↑)				600			ns
$\overline{SCK}$ ↓ → SO**Note 1** output	t_{KSO2}	R_L = 1 kΩ **Note 2**	V_{DD} = 2.7 to 5.5 V	0		300	ns
delay time		C_L = 100 pF		0		1000	ns

Notes 1. Read as SB0 or SB1 when using the 2-wire serial I/O mode.

2. R_L and C_L respectively indicate the load resistance and load capacitance of the SO output line.

SBI mode ($\overline{SCK}$ ··· internal clock output (master)): (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY3}	V_{DD} = 2.7 to 5.5 V		1300			ns
				3800			ns
$\overline{SCK}$ high-, low-level widths	t_{KL3}	V_{DD} = 2.7 to 5.5 V		t_{KCY3}/2–50			ns
	t_{KH3}			t_{KCY3}/2–150			ns
SB0, 1 setup time	t_{SIK3}	V_{DD} = 2.7 to 5.5 V		150			ns
(vs. $\overline{SCK}$ ↑)				500			ns
SB0, 1 hold time (vs. $\overline{SCK}$ ↑)	t_{KSI3}			t_{KCY3}/2			ns
$\overline{SCK}$ ↓ → SB0, 1 output	t_{KSO3}	R_L = 1 kΩ **Note**	V_{DD} = 2.7 to 5.5 V	0		250	ns
delay time		C_L = 100 pF		0		1000	ns
$\overline{SCK}$ ↑ → SB0, 1 ↓	t_{KSB}			t_{KCY3}			ns
SB0, 1 ↓ → $\overline{SCK}$ ↓	t_{SBK}			t_{KCY3}			ns
SB0, 1 low-level width	t_{SBL}			t_{KCY3}			ns
SB0, 1 high-level width	t_{SBH}			t_{KCY3}			ns

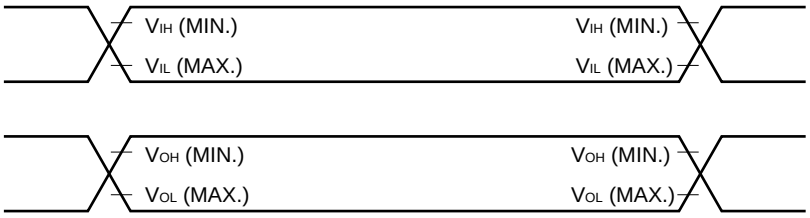
Note R_L and C_L respectively indicate the load resistance and load capacitance of the SB0 and 1 output lines.

SBI mode ($\overline{SCK}$ ··· external clock input (slave)): (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

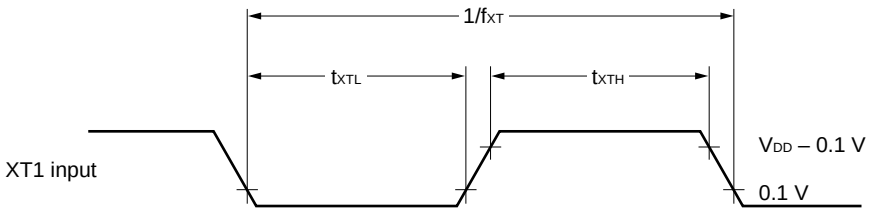
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY4}	V_{DD} = 2.7 to 5.5 V		800			ns
				3200			ns
$\overline{SCK}$ high-, low-level widths	t_{KL4}	V_{DD} = 2.7 to 5.5 V		400			ns
	t_{KH4}			1600			ns
SB0, 1 setup time	t_{SIK4}	V_{DD} = 2.7 to 5.5 V		100			ns
(vs. $\overline{SCK}$ ↑)				150			ns
SB0, 1 hold time (vs. $\overline{SCK}$ ↑)	t_{KSI4}			t_{KCY4}/2			ns
$\overline{SCK}$ ↓ → SB0, 1 output	t_{KSO4}	R_L = 1 kΩ **Note**	V_{DD} = 2.7 to 5.5 V	0		300	ns
delay time		C_L = 100 pF		0		1000	ns
$\overline{SCK}$ ↑ → SB0, 1 ↓	t_{KSB}			t_{KCY4}			ns
SB0, 1 ↓ → $\overline{SCK}$ ↓	t_{SBK}			t_{KCY4}			ns
SB0, 1 low-level width	t_{SBL}			t_{KCY4}			ns
SB0, 1 high-level width	t_{SBH}			t_{KCY4}			ns

Note R_L and C_L respectively indicate the load resistance and load capacitance of the SB0 and 1 output lines.

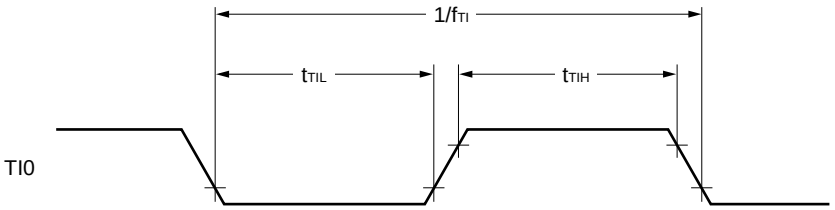
AC Timing Test Points (except XT1 input)



Clock timing

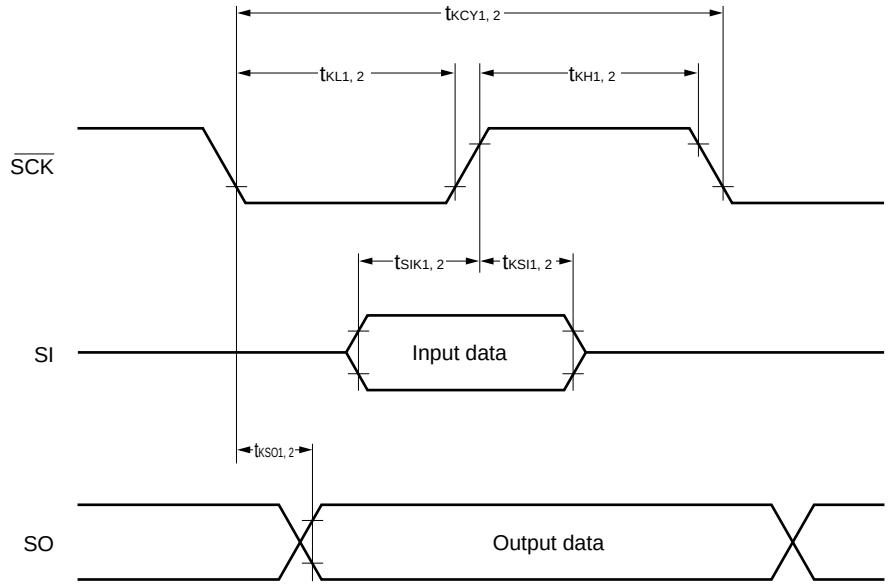


TI0 timing

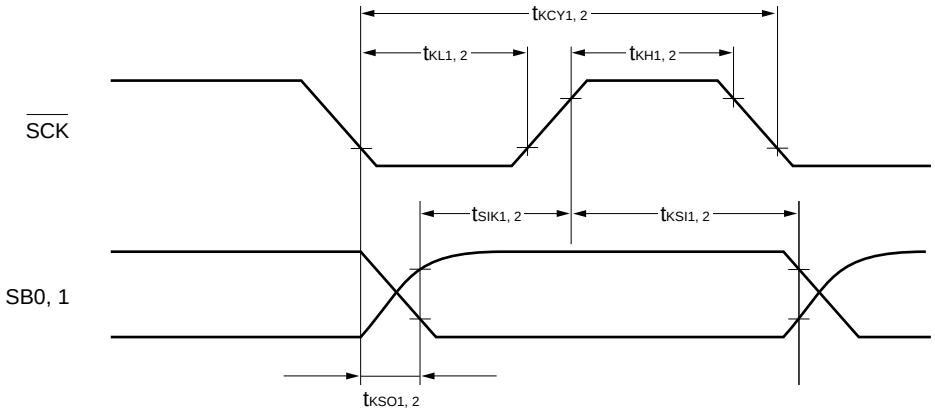


Serial Transfer Timing

3-wire serial I/O mode

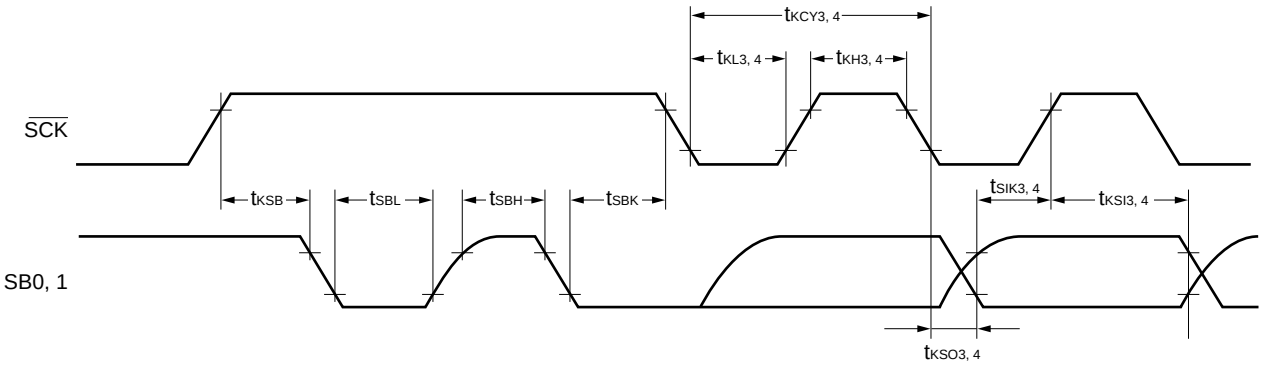


2-wire serial I/O mode

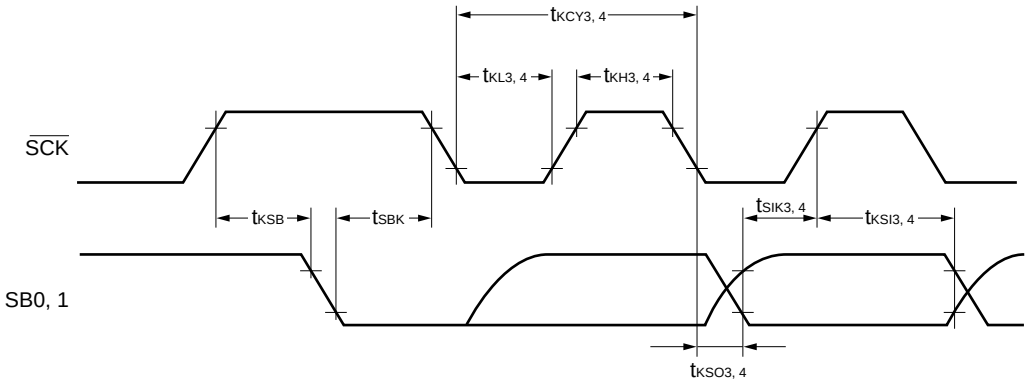


Serial Transfer Timing

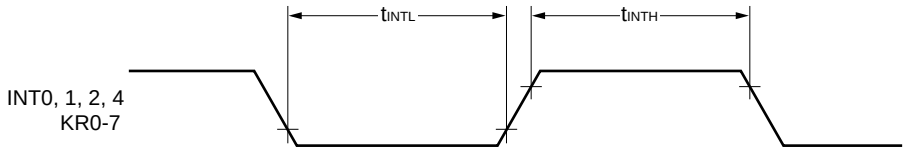
Bus release signal transfer



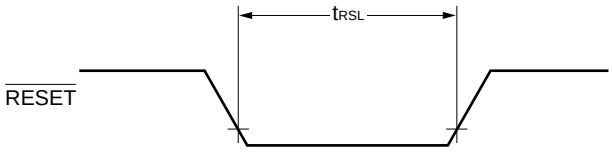
Command signal transfer



Interrupt input timing



$\overline{\text{RESET}}$ input timing

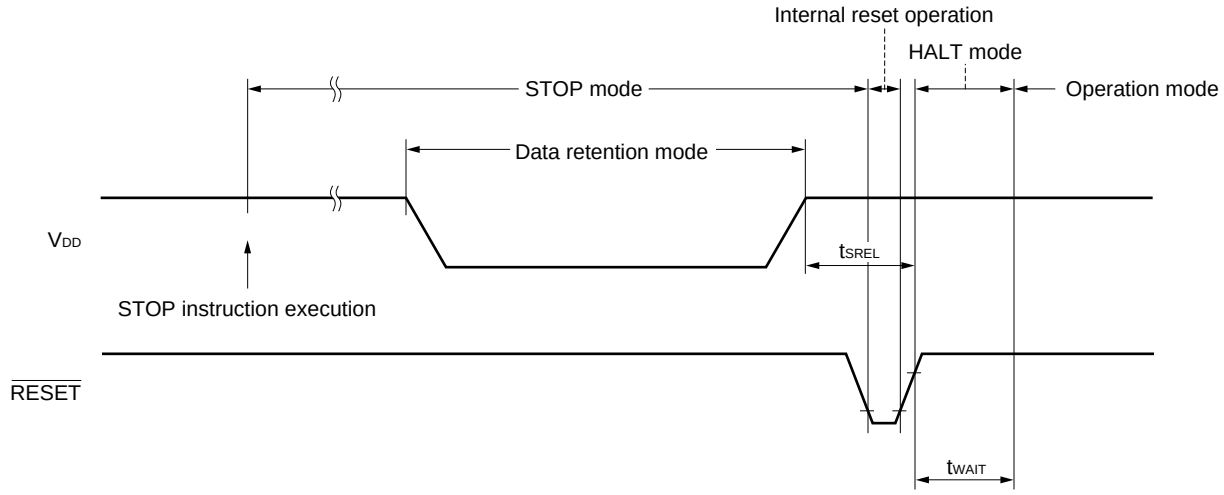


Data Retention Characteristics of Data Memory in STOP Mode and at Low Supply Voltage (T_A = –40 to +85 °C)

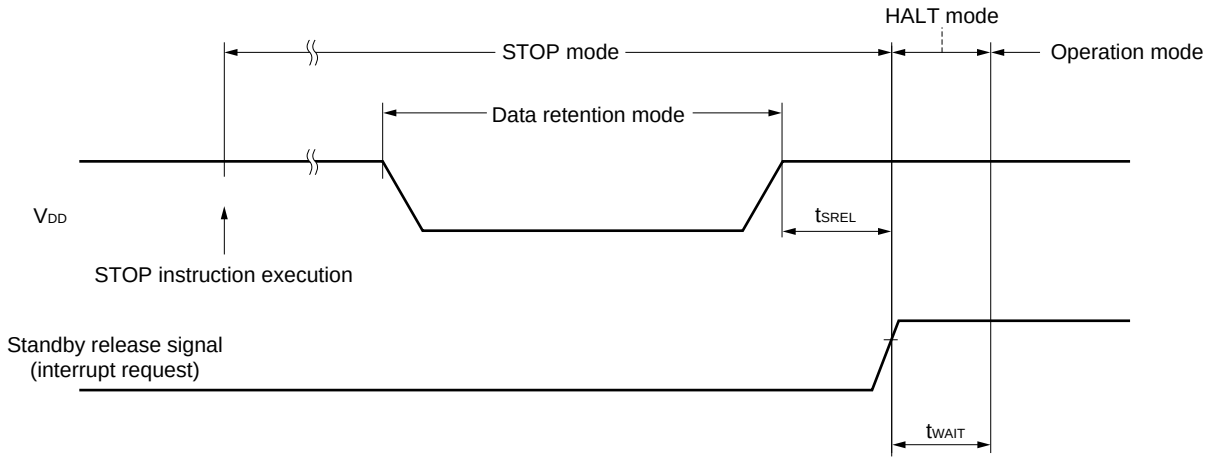
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Release signal setup time	t_{SREL}		0			μs
Oscillation stabilization wait time Note 1	t_{WAIT}	Released by $\overline{RESET}$		56/f_{CC}		μs
		Released by interrupt request		512/f_{CC}		μs

Note The oscillation stabilization wait time is the time during which the CPU stops operating to prevent unstable operation when oscillation is started.

Data retention timing (when STOP mode released by $\overline{RESET}$)



Data retention timing (standby release signal: when STOP mode released by interrupt signal)



DC Programming Characteristics (T_A = 25 ± 5 °C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V, V_{SS} = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	Other than CL1 pin	0.7 V_{DD}		V_{DD}	V
	V_{IH2}	CL1	V_{DD} – 0.5		V_{DD}	V
Input voltage, low	V_{IL1}	Other than CL1 pin	0		0.3 V_{DD}	V
	V_{IL2}	CL1	0		0.4	V
Input leakage current	I_{LI}	V_{IN} = V_{IL} or V_{IH}			10	μA
Output voltage, high	V_{OH}	I_{OH} = – 1 mA	V_{DD} – 1.0			V
Output voltage, low	V_{OL}	I_{OL} = 1.6 mA			0.4	V
V_{DD} supply current	I_{DD}				30	mA
V_{PP} supply current	I_{PP}	MD0 = V_{IL}, MD1 = V_{IH}			30	mA

Cautions 1. Keep V_{PP} to within +13.5 V, including overshoot.

2. Apply V_{DD} before V_{PP} and turn it off after V_{PP}.

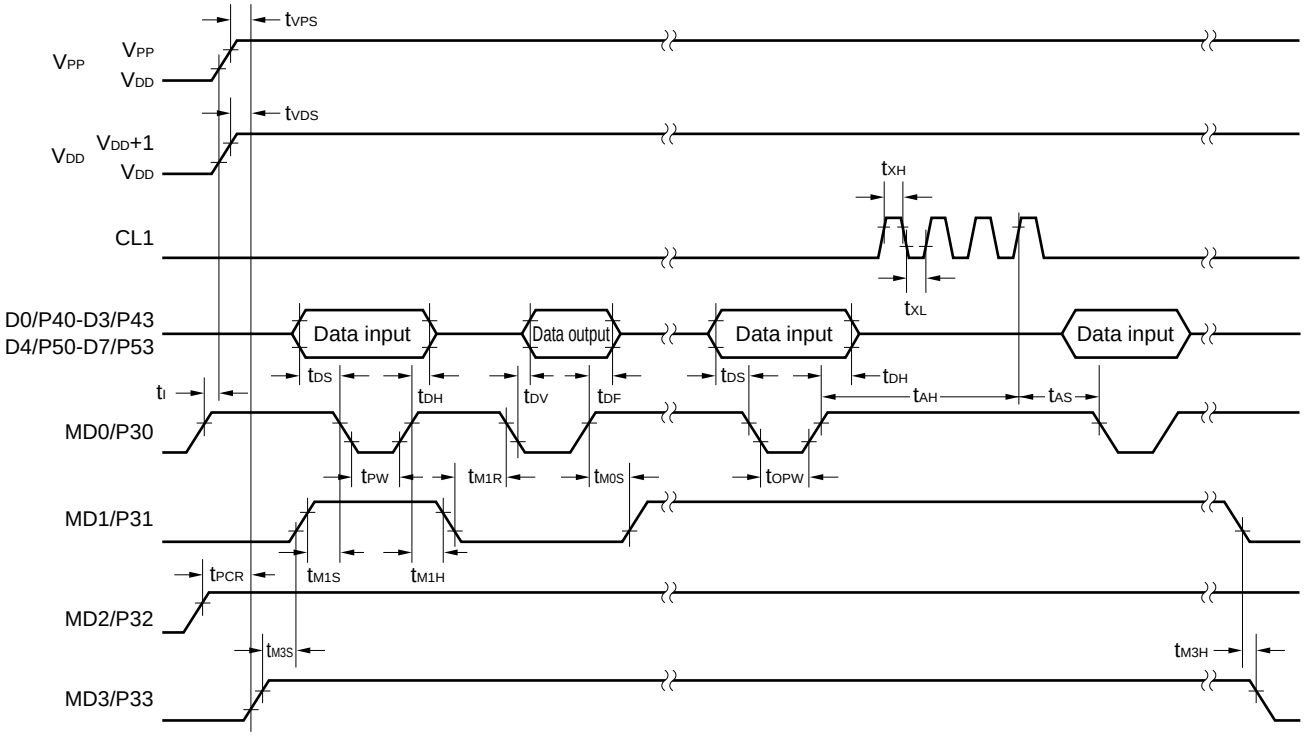
AC Programming Characteristics (T_A = 25 ± 5 °C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V, V_{SS} = 0 V)

Parameter	Symbol	**Note 1**	Conditions	MIN.	TYP.	MAX.	Unit
Address setup time **Note 2** (vs. MD0 ↓)	t_{AS}	t_{AS}		2			μs
MD1 setup time (vs. MD0 ↓)	t_{M1S}	t_{OES}		2			μs
Data setup time (vs. MD0 ↓)	t_{DS}	t_{DS}		2			μs
Address hold time **Note 2** (vs. MD0 ↑)	t_{AH}	t_{AH}		2			μs
Data hold time (vs. MD0 ↑)	t_{DH}	t_{DH}		2			μs
MD0 ↑ → data output float delay time	t_{DF}	t_{DF}		0		130	ns
V_{PP} setup time (vs. MD3 ↑)	t_{VPS}	t_{VPS}		2			μs
V_{DD} setup time (vs. MD3 ↑)	t_{VDS}	t_{VCS}		2			μs
Initial program pulse width	t_{PW}	t_{PW}		0.95	1.0	1.05	ms
Additional program pulse width	t_{OPW}	t_{OPW}		0.95		21.0	ms
MD0 setup time (vs. MD1 ↑)	t_{M0S}	t_{CES}		2			μs
MD0 ↓ → data output delay time	t_{DV}	t_{DV}	MD0 = MD1 = V_{IL}			1	μs
MD1 hold time (vs. MD0 ↑)	t_{M1H}	t_{OEH}	t_{M1H} + t_{M1R} ≥ 50 μs	2			μs
MD1 recovery time (vs. MD0 ↓)	t_{M1R}	t_{OR}		2			μs
Program counter reset time	t_{PCR}	—		10			μs
CL1 input high-, low-level width	t_{XH}, t_{XL}	—		0.125			μs
CL1 input frequency	f_{CC}	—				4.19	MHz
Initial mode set time	t_I	—		2			μs
MD3 setup time (vs. MD1 ↑)	t_{M3S}	—		2			μs
MD3 hold time (vs. MD1 ↓)	t_{M3H}	—		2			μs
MD3 setup time (vs. MD0 ↓)	t_{M3SR}	—	When program memory is read	2			μs
Address **Note 2** → data output delay time	t_{DAD}	t_{ACC}	When program memory is read			2	μs
Address **Note 2** → data output hold time	t_{HAD}	t_{OH}	When program memory is read	0		130	ns
MD3 hold time (vs. MD0 ↑)	t_{M3HR}	—	When program memory is read	2			μs
MD3 ↓ → data output float delay time	t_{DFR}	—	When program memory is read			2	μs

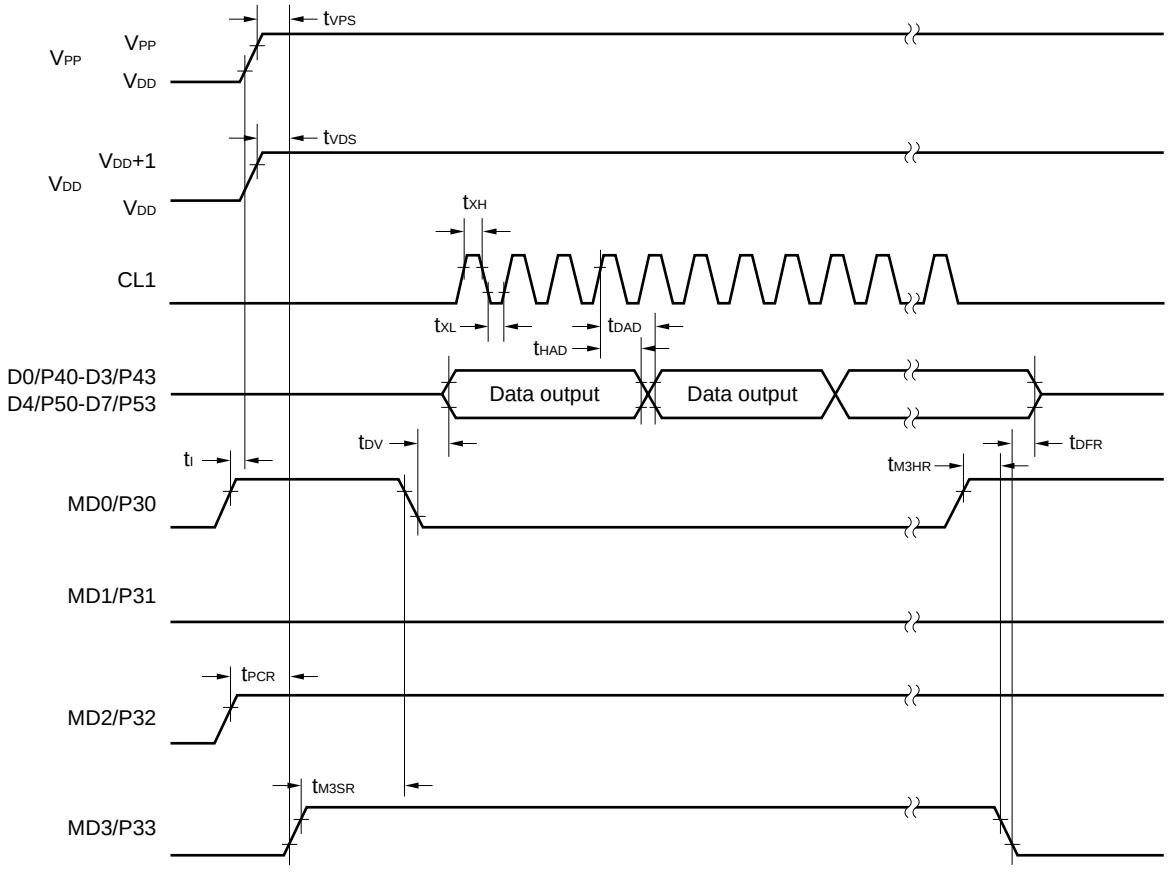
Notes 1. Symbol of corresponding μPD27C256A

2. The internal address signal is incremented by one at the rising edge of the fourth CL1 input and is not connected to a pin.

Program Memory Write Timing

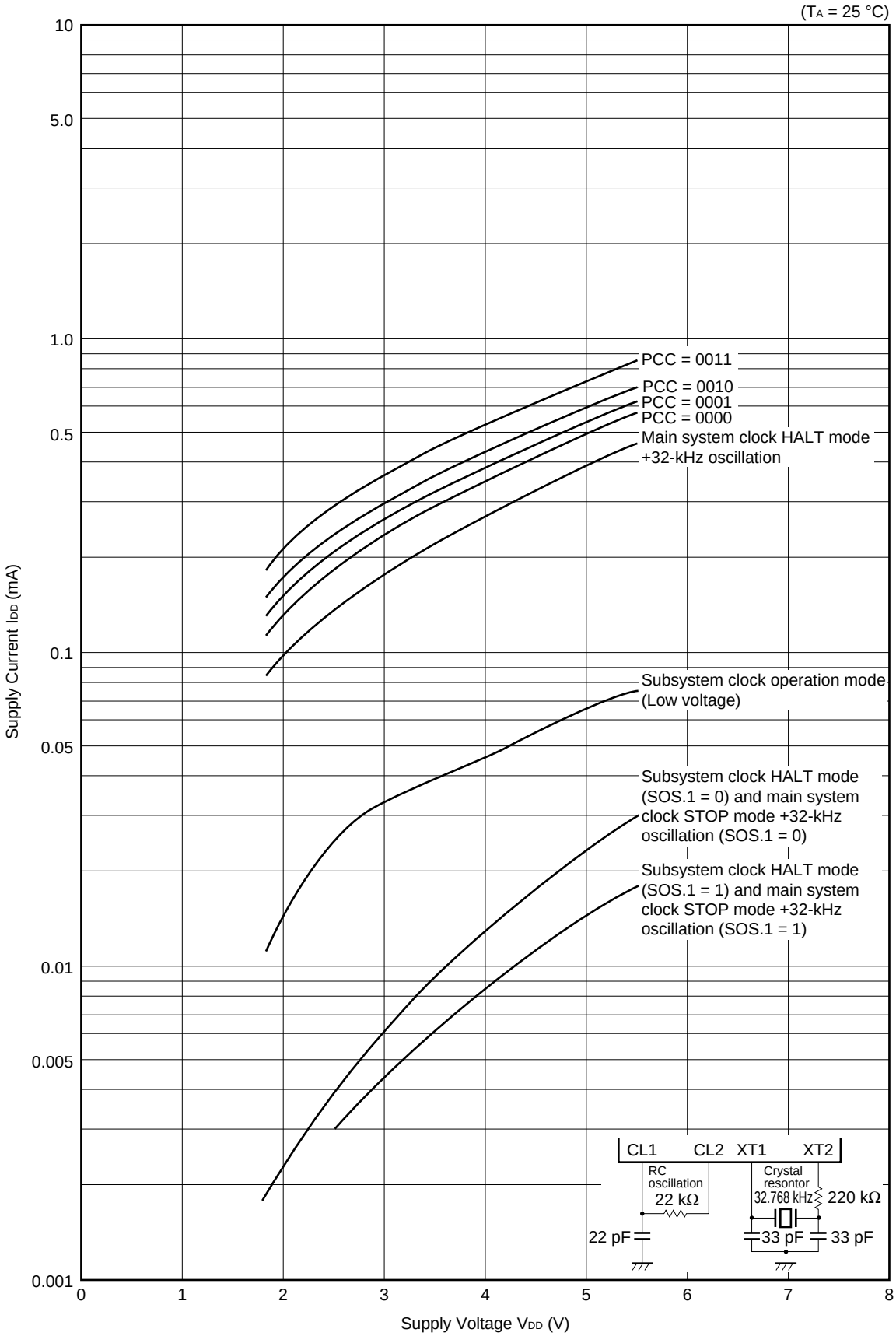


Program Memory Read Timing



10. CHARACTERISTICS CURVES (REFERENCE VALUE)

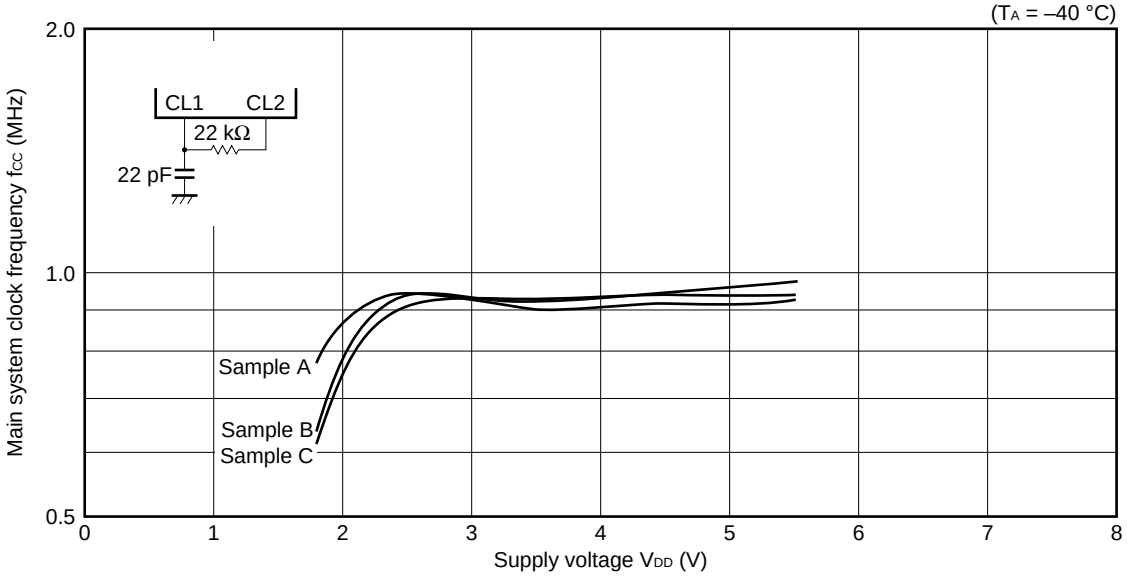
I_{DD} vs V_{DD} (Main system clock : 1.0 MHz RC oscillation)



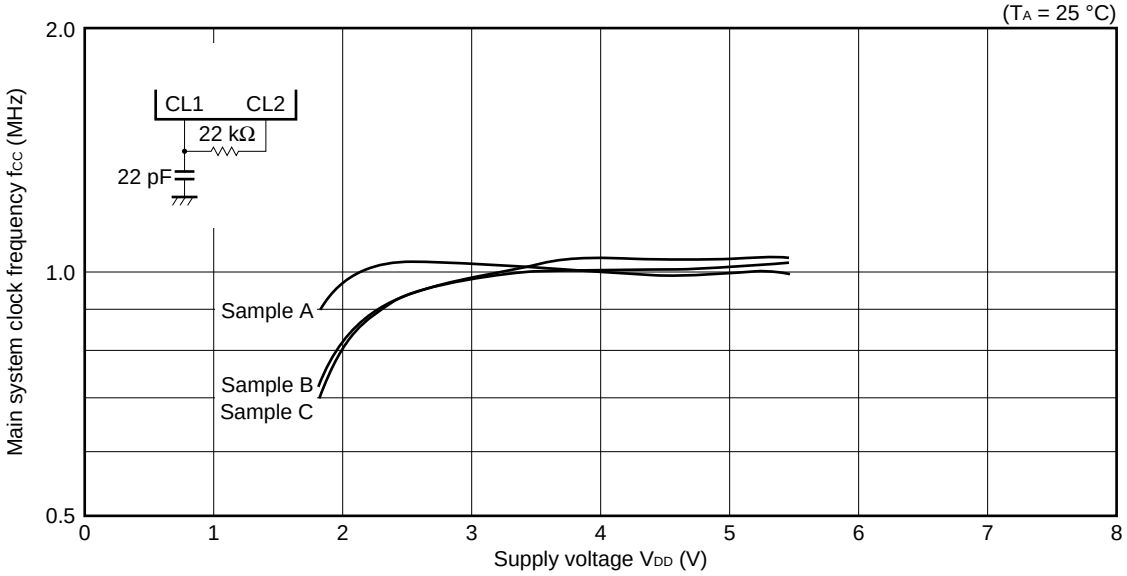
11. RC OSCILLATION FREQUENCY CHARACTERISTICS EXAMPLES (REFERENCE VALUE)

f_{CC} vs V_{DD} (RC oscillation, R = 22kΩ, C = 22 pF)

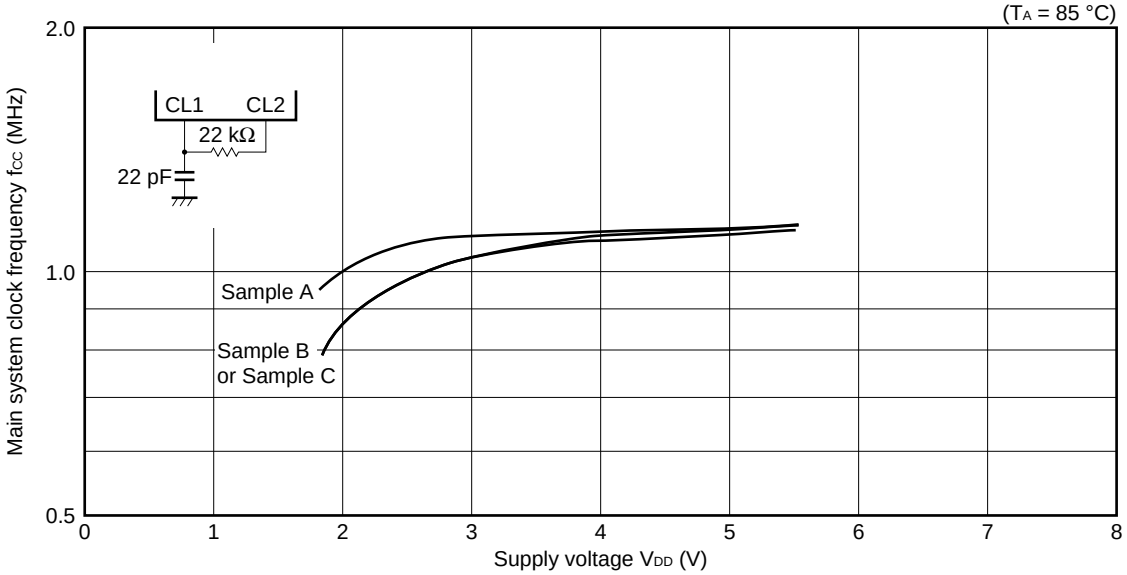
(T_A = –40 °C)



(T_A = 25 °C)

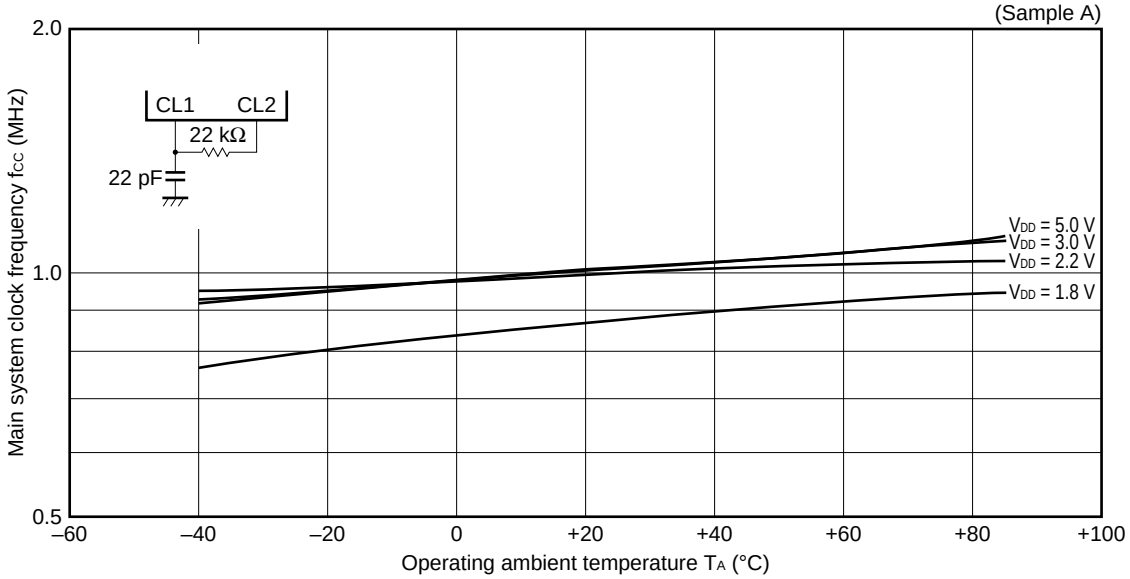


(T_A = 85 °C)

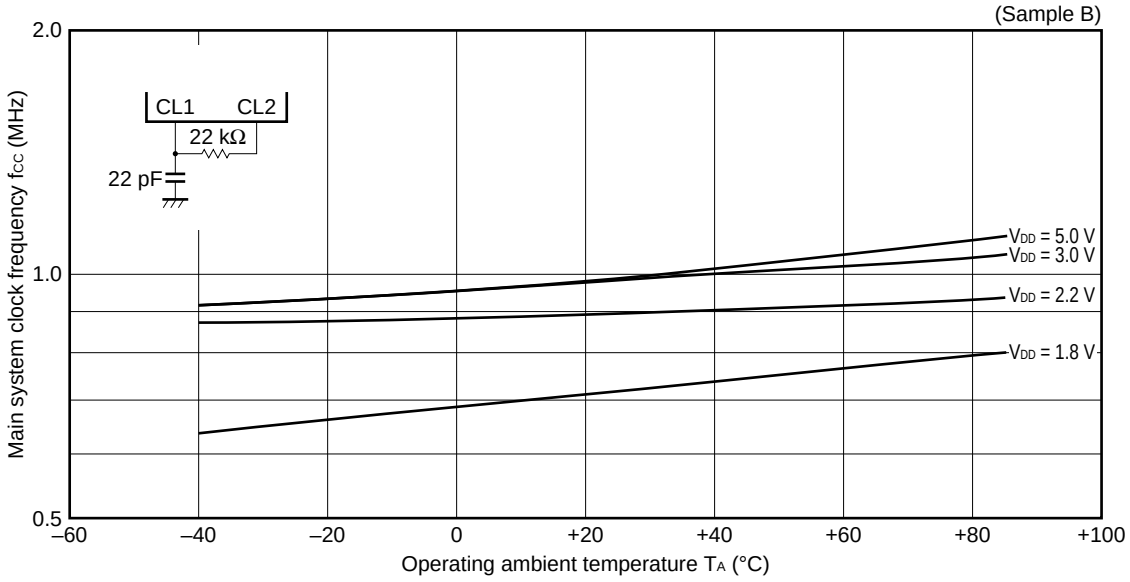


f_{CC} vs T_A (RC oscillation, R = 22kΩ, C = 22 pF)

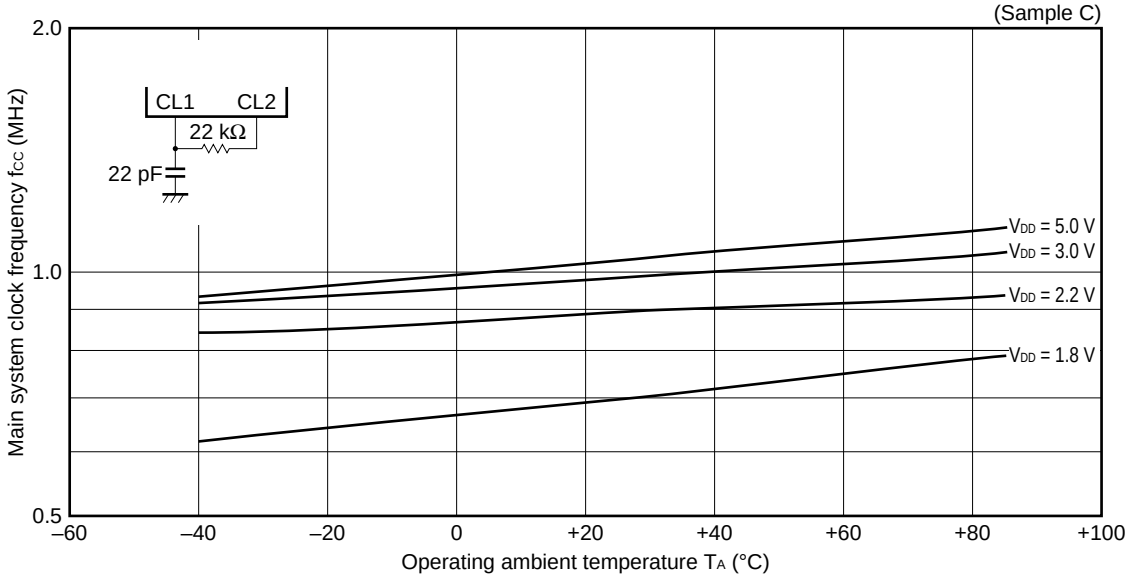
(Sample A)



(Sample B)

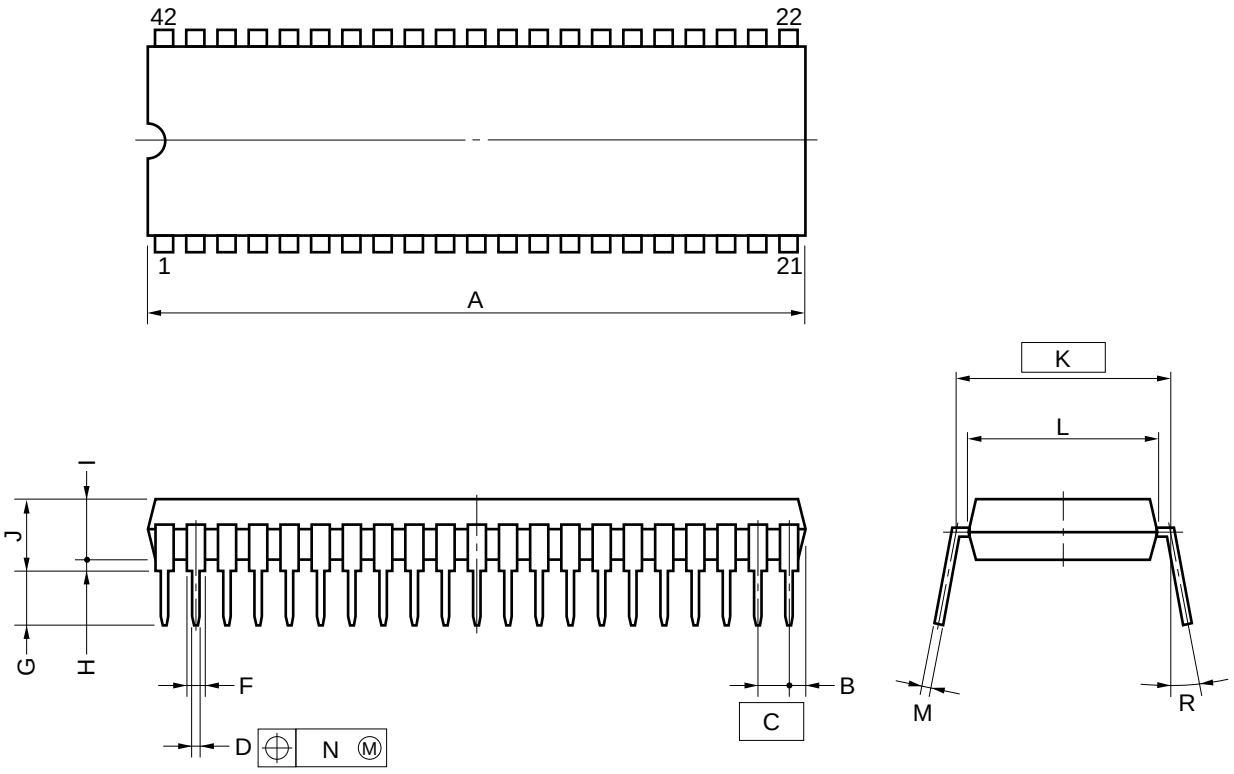


(Sample C)



12. PACKAGE DRAWINGS

42PIN PLASTIC SHRINK DIP (600 mil)



NOTES

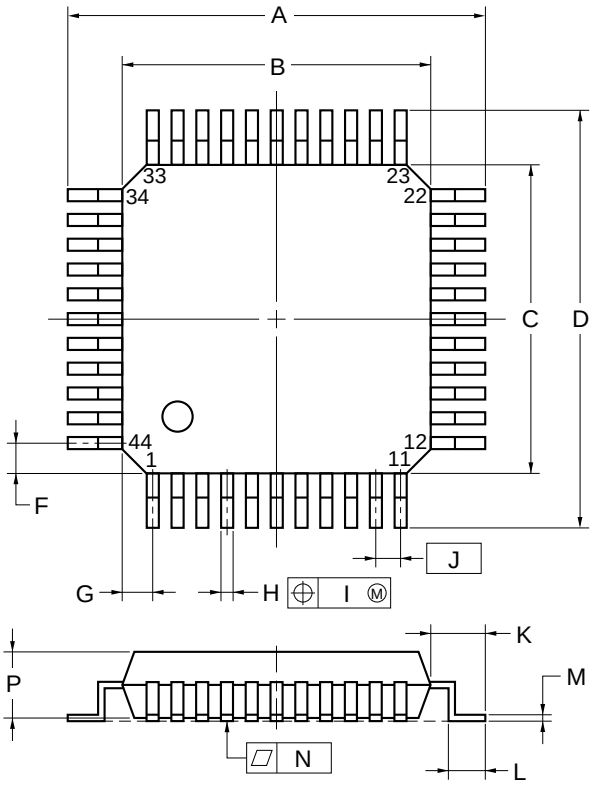
1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

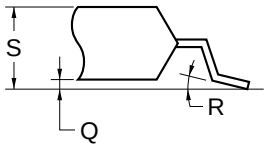
ITEM	MILLIMETERS	INCHES
A	39.13 MAX.	1.541 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

P42C-70-600A-1

44 PIN PLASTIC QFP (□10)



detail of lead end



NOTE

Each lead centerline is located within 0.16 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	13.2±0.2	$0.520^{+0.008}_{-0.009}$
B	10.0±0.2	$0.394^{+0.008}_{-0.009}$
C	10.0±0.2	$0.394^{+0.008}_{-0.009}$
D	13.2±0.2	$0.520^{+0.008}_{-0.009}$
F	1.0	0.039
G	1.0	0.039
H	$0.37^{+0.08}_{-0.07}$	$0.015^{+0.003}_{-0.004}$
I	0.16	0.007
J	0.8 (T.P.)	0.031 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.17^{+0.06}_{-0.05}$	$0.007^{+0.002}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.125±0.075	0.005±0.003
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	3.0 MAX.	0.119 MAX.

S44GB-80-3BS

13. RECOMMENDED SOLDERING CONDITIONS

Solder the μPD75P0116 under the following recommended conditions.

For the details on the recommended soldering conditions, refer to Information Document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For the soldering methods and conditions other than those recommended, consult NEC.

Table 13-1. Soldering Conditions of Surface Mount Type

μPD75P0116GB-3BS-MTX: 44-pin plastic QFP (10 × 10 mm, 0.8-mm pitch)

Soldering method	Soldering conditions	Symbol of recommended condition
Infrared reflow	Package peak temperature: 235 °C, Time: 30 seconds max. (210 °C min.), Number of times: 3 max.	IR35-00-3
VPS	Package peak temperature: 215 °C, Time: 40 seconds max. (200 °C min.), Number of times: 3 max.	VP15-00-3
Wave soldering	Soldering bath temperature: 260 °C max., Time: 10 seconds max., Number of times: 1 Preheating temperature: 120 °C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300 °C max., Time: 3 seconds max. (per side of device)	–

Caution Do not use two or more soldering methods in combination (except the partial heating method).

Table 13-2. Soldering Conditions of Insertion Type

μPD75P0116CU: 42-pin plastic Shrink DIP (600 mil, 1.778-mm pitch)

Soldering method	Soldering conditions
Wave soldering (pin only)	Soldering bath temperature: 260 °C max., Time: 10 seconds max.
Partial heating	Pin temperature: 300 °C max., Time: 3 seconds max. (per pin)

Caution Apply wave soldering to the pins only. Be careful not to allow solder jet to come into direct contact with the body of the chip.

APPENDIX A. FUNCTION LIST OF μPD750008, 750108, AND 75P0116

(1/2)

Parameter		μPD750008	μPD750108	μPD75P0116
Program memory		Mask ROM 0000H-1FFFH (8192 × 8 bits)		One-time PROM 0000H-3FFFH (16384 × 8 bits)
Data memory		000H-1FFH (512 × 4 bits)		
CPU		75XL CPU		
General register		(4 bits × 8 or 8 bits × 4) × 4 banks		
Main system clock oscillation circuit		Crystal/ceramic oscillation circuit	RC oscillation circuit (external resistor and capacitor)	
Start-up time after reset		$2^{17}/f_X$, $2^{15}/f_X$ (Selected by mask option)	56/f_{CC} fixed	
Wait time after releasing STOP mode due to interrupt occurrence		$2^{20}/f_X$, $2^{17}/f_X$, $2^{15}/f_X$, $2^{13}/f_X$ (Selected by setting BTM)	$2^9/f_{CC}$, no wait (Selected by mask option)	$2^9/f_{CC}$ fixed
Subsystem clock oscillation circuit		Crystal oscillation circuit		
Instruction execution time	When main system clock is selected	• 0.95, 1.91, 3.81, 15.3 μs (at f_X = 4.19-MHz operation) • 0.67, 1.33, 2.67, 10.7 μs (at f_X = 6.0-MHz operation)	• 4, 8, 16, 64 μs (at f_{CC} = 1.0 MHz operation) • 2, 4, 8, 32 μs (at f_{CC} = 2.0 MHz operation)	
	When subsystem clock is selected	122 μs (at 32.768 kHz operation)		
I/O port	CMOS input	8 (on-chip pull-up resistors can be specified in software: 7)		
	CMOS input/output	18 (on-chip pull-up resistors can be specified in software)		
	N-ch open drain input/output	8 (on-chip pull-up resistors can be specified in software), Withstand voltage is 13 V		8 (no mask option) Withstand voltage is 13 V.
	Total	34		
Timer		4 channels • 8-bit timer counter: 1 channel • 8-bit timer/event counter: 1 channel • Basic interval timer/ watchdog timer: 1 channel • Watch timer: 1 channel	4 channels • 8-bit timer counter (with watch timer output function): 1 channel • 8-bit timer/event counter: 1 channel • Basic interval timer/watchdog timer: 1 channel • Watch timer: 1 channel	
Serial interface		3 modes are available • 3-wire serial I/O mode ... MSB/LSB can be selected for transfer top bit • 2-wire serial I/O mode • SBI mode		
Clock output (PCL)		• Φ, 524, 262, 65.5 kHz (Main system clock: at 4.19-MHz operation) • Φ, 750, 375, 93.8 kHz (Main system clock: at 6.0-MHz operation)	• Φ, 125, 62.5, 15.6 kHz (main system clock: at 1.0-MHz operation) • Φ, 250, 125, 31.3 kHz (main system clock: at 2.0-MHz operation)	
Buzzer output (BUZ)		• 2, 4, 32 kHz (Main system clock: at 4.19-MHz operation or subsystem clock: at 32.768-kHz operation) • 2.93, 5.86, 46.9 kHz (Main system clock: at 6.0-MHz operation)	• 2, 4, 32 kHz (Subsystem clock: at 32.768-kHz operation) • 0.488, 0.977, 7.813 kHz (Main system clock: at 1.0-MHz operation) • 0.977, 1.953, 15.625 kHz (Main system clock: at 2.0-MHz operation)	

(2/2)

Parameter	μPD750008	μPD750108	μPD75P0116
Vectored interrupt	External: 3, internal: 4		
Test input	External: 1, internal: 1		
Operation supply voltage	V_{DD} = 2.2 to 5.5 V	V_{DD} = 1.8 to 5.5 V	
Operating ambient temperature	T_A = –40 to +85 ˚C		
Package	• 42-pin plastic shrink DIP (600 mil, 1.778-mm pitch) • 44-pin plastic shrink QFP (10 × 10 mm, 0.8-mm pitch)		

APPENDIX B. DEVELOPMENT TOOLS

The following development tools are provided for system development using the μPD75P0116. The 75XL series uses a common relocatable assembler, in combination with a device file matching each machine.

RA75X relocatable assembler	Host machine			Part number (product name)
		OS	Supply medium	
	PC-9800 series	MS-DOS™ (Ver.3.30 to Ver.6.2 **Note**)	3.5" 2HD	μS5A13RA75X
			5" 2HD	μS5A10RA75X
	IBM PC/AT™ or compatible	Refer to **OS for IBM PCs**	3.5" 2HC	μS7B13RA75X
			5" 2HC	μS7B10RA75X

Device file	Host machine			Part number (product name)
		OS	Supply medium	
	PC-9800 series	MS-DOS (Ver.3.30 to Ver.6.2 **Note**)	3.5" 2HD	μS5A13DF750008
			5" 2HD	μS5A10DF750008
	IBM PC/AT or compatible	Refer to **OS for IBM PCs**	3.5" 2HC	μS7B13DF750008
			5" 2HC	μS7B10DF750008

Note Ver. 5.00 and the upper versions of Ver. 5.00 are provided with a task swap function, but it does not work with this software.

Remark The operation of the assembler and device file is guaranteed only on the above host machines and OSs.

PROM Write Tools

<table>
<tr><td rowspan="2">Hardware</td><td>PG-1500</td><td colspan="4">A stand-alone system can be configured of a single-chip microcomputer with on-chip PROM when connected to an auxiliary board (companion product) and a programmer adapter (separately sold). Alternatively, a PROM programmer can be operated on a host machine for programming.
In addition, typical PROMs in capacities ranging from 256 K to 4 M bits can be programmed.</td></tr>
<tr><td>PA-75P008CU</td><td colspan="4">This is a PROM programmer adapter for the μPD75P0116CU/GB. It can be used when connected to a PG-1500.</td></tr>
<tr><td rowspan="6">Software</td><td rowspan="6">PG-1500 controller</td><td colspan="4">Establishes serial and parallel connections between the PG-1500 and a host machine for host-machine control of the PG-1500.</td></tr>
<tr><td rowspan="2">Host machine</td><td colspan="2" rowspan="2">OS</td><td rowspan="2">Supply medium</td><td>Part number</td></tr>
<tr><td>(product name)</td></tr>
<tr><td>PC-9800 Series</td><td colspan="2">MS-DOS
(Ver.3.30 to Ver.6.2 Note)</td><td>3.5" 2HD</td><td>μS5A13PG1500</td></tr>
<tr><td>PC-9800 Series</td><td colspan="2">MS-DOS
(Ver.3.30 to Ver.6.2 Note)</td><td>5" 2HD</td><td>μS5A10PG1500</td></tr>
<tr><td>IBM PC/AT or compatible</td><td colspan="2">Refer to OS for IBM PCs</td><td>3.5" 2HD</td><td>μS7B13PG1500</td></tr>
<tr><td>IBM PC/AT or compatible</td><td colspan="2">Refer to OS for IBM PCs</td><td>5" 2HC</td><td>μS7B10PG1500</td></tr>
</table>

Note Ver. 5.00 and the upper versions of Ver. 5.00 are provided with a task swapping function, but it does not work with this software.

Remark Operation of the PG-1500 controller is guaranteed only on the above host machine and OSs.

Debugging Tools

In-circuit emulators (IE-75000-R and IE-75001-R) are provided as program debugging tools for the μPD75P0116. Various system configurations using these in-circuit emulators are listed below.

<table>
<tr><td rowspan="6">Hardware</td><td>IE-75000-R^{Note 1}</td><td colspan="3">The IE-75000-R is an in-circuit emulator to be used for hardware and software debugging during development of application systems that use 75X or 75XL Series products. For development of the μPD750108 subseries, the IE-75000-R is used with a separately sold emulation board IE-75300-R-EM and emulation probe EP-75008CU-R or EP-75008GB-R.
These products can be applied for highly efficient debugging when connected to a host machine and PROM programmer.
The IE-75000-R can include a connected emulation board (IE-75000-R-EM).</td></tr>
<tr><td>IE-75001-R</td><td colspan="3">The IE-75001-R is an in-circuit emulator to be used for hardware and software debugging during development of application systems that use 75X or 75XL Series products. The IE-75001-R is used with a separately sold emulation board IE-75300-R-EM and emulation probe EP-75008CU-R or EP-75008GB-R.
These products can be applied for highly efficient debugging when connected to a host machine and PROM programmer.</td></tr>
<tr><td>IE-75300-R-EM</td><td colspan="3">This is an emulation board for evaluating application systems that use the μPD750108 subseries. It is used in combination with the IE-75000-R or IE-75001-R in-circuit emulator.</td></tr>
<tr><td>EP-75008CU-R</td><td colspan="3">This is an emulation probe for the μPD75P0116CU.
When being used, it is connected with the IE-75000-R or IE-75001-R and the IE-75300-R-EM.</td></tr>
<tr><td>EP-75008GB-R
EV-9200G-44</td><td colspan="3">This is an emulation probe for the μPD75P0116GB.
When being used, it is connected with the IE-75000-R or IE-75001-R and the IE-75300-R-EM.
It includes a 44-pin conversion socket EV-9200G-44 to facilitate connections with various target systems.</td></tr>
<tr><td rowspan="4">Software</td><td rowspan="4">IE control program</td><td colspan="3">This program can control the IE-75000-R or IE-75001-R on a host machine when connected to the IE-75000-R or IE-75001-R via an RS-232-C or Centronics I/F.</td></tr>
<tr><td rowspan="2">Host machine</td><td rowspan="2">OS</td><td rowspan="2">Supply medium</td><td>Part number</td></tr>
<tr><td>(product name)</td></tr>
<tr><td>PC-9800 series</td><td>MS-DOS
(Ver.3.30 to Ver.6.2 ^{Note 2})</td><td>3.5" 2HD</td><td>μS5A13IE75X</td></tr>
<tr><td>IBM PC/AT or compatible</td><td>Refer to OS for IBM PCs</td><td>5" 2HD</td><td>μS5A10IE75X</td></tr>
<tr><td></td><td></td><td>3.5" 2HC</td><td>μS7B13IE75X</td></tr>
<tr><td></td><td></td><td>5" 2HC</td><td>μS7B10IE75X</td></tr>
</table>

Notes 1. This is a service part provided for maintenance purpose only.

2. Ver. 5.00 and the upper versions of Ver. 5.00 are provided with a task swapping function, but it does not work with this software.

Remarks 1. Operation of the IE control program is guaranteed only on the above host machine and OSs.

2. The μPD750108 subseries consists of the μPD750104, 750106, 750108 and 75P0116.

OS for IBM PCs

The following operating systems for the IBM PC are supported.

OS	Version
PC DOS™	Ver.3.1 to Ver.6.3 J6.1/V[Note] to J6.3/V[Note]
MS-DOS	Ver.5.0 to Ver.6.22 5.0/V[Note] to J6.2/V[Note]
IBM DOS™	J5.02/V[Note]

Note Supports English version only.

Caution Ver 5.0 and above include a task swapping function, but this software is not able to use that function.

APPENDIX C. RELATED DOCUMENTS

Some of the following related documents are preliminary. This document, however, is not indicated as preliminary.

Device Related Documents

Document name	Document No.	
	Japanese	English
μPD750104, 750106, 750108, 750104(A), 750106(A), 750108(A) Data Sheet	U12301J	Planned
μPD75P0116 Data Sheet	U12603J	This document
μPD750108 User's Manual	U11330J	U11330E
μPD750008, 750108 Instruction List	U11456J	–
75XL Series Selection Guide	U10453J	U10453E

Development Tool Related Documents

Document name			Document No.	
			Japanese	English
Hardware	IE-75000 R/IE-75001-R User's Manual		EEU-846	EEU-1416
	IE-75300-R-EM User's Manual		U11354J	U11354E
	EP-750008CU-R User's Manual		EEU-699	EEU-1317
	EP-750008GB-R User's Manual		EEU-698	EEU-1305
	PG-1500 User's Manual		U11940J	EEU-1335
Software	RA75X Assembler Package User's Manual	Operation	EEU-731	EEU-1346
		Language	EEU-730	EEU-1363
	PG-1500 Controller User's Manual	PC-9800 Series (MS-DOS) Base	EEU-704	EEU-1291
		IBM PC Series (PC DOS) Base	EEU-5008	U10540E

Other Documents

Document name	Document No.	
	Japanese	English
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Devices	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Static Electricity Discharge (ESD) Test	MEM-539	–
Semiconductor Devices Quality Guarantee Guide	C11893J	MEI-1202
Guide for Products Related to Microcomputer : Other Companies	C11416J	–

Caution The above related documents are subject to change without notice. For design purpose, etc., be sure to use the latest documents.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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