NEC

MOS INTEGRATED CIRCUIT

μPD75P068

4 BIT SINGLE-CHIP MICROCOMPUTER

The μPD75P068 is produced by replacing the internal mask ROM of the μPD75068 with a one-time PROM in which data can be written once.

The following user's manual describes the details of the functions of the μPD75P068. Be sure to read it before designing an application system.

μPD75068 User's Manual: IEU-1366

FEATURES

- Compatible with the μPD75068
  - Can be replaced with the μPD75068 containing mask ROM on a full-production basis.
- Internal one-time PROM: 8064 words × 8 bits
- Internal RAM: 512 words × 4 bits
- Internal pull-up resistors can be specified with software: Ports 0 to 3 and 6
- N-ch open-drain input-output: Ports 4 and 5
- Can operate at low voltage: V_{DD} = 2.7 to 6.0 V

ORDERING INFORMATION

Part number	Package	Quality grade
μPD75P068CU	42-pin plastic shrink DIP (600 mil)	Standard
μPD75P068GB-3B4	44-pin plastic QFP (Square 10 mm)	Standard

Caution The μPD75P068 is not provided with mask-selected pull-up resistors.

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

The information in this document is subject to change without notice.

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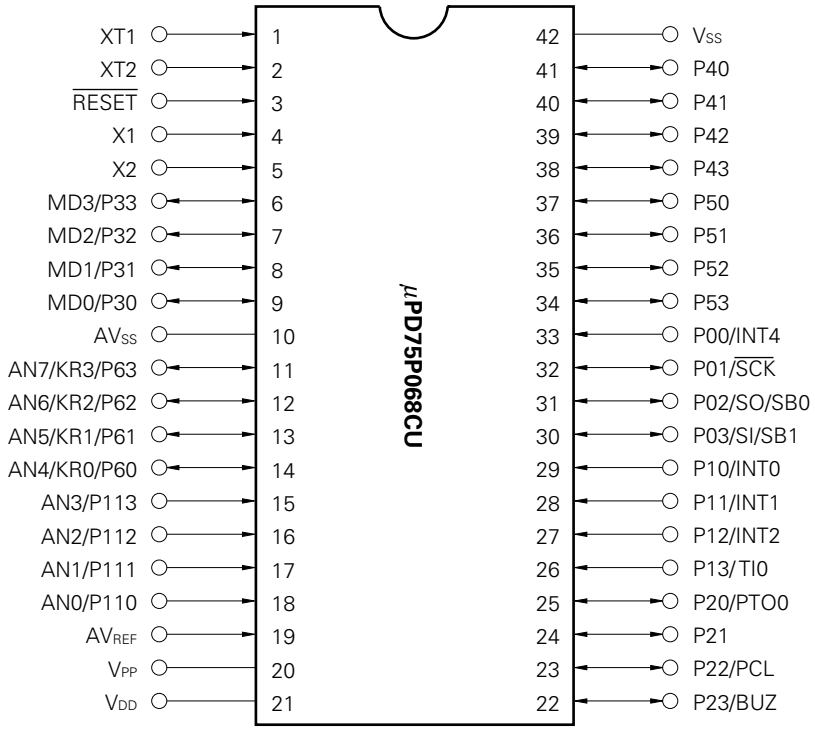
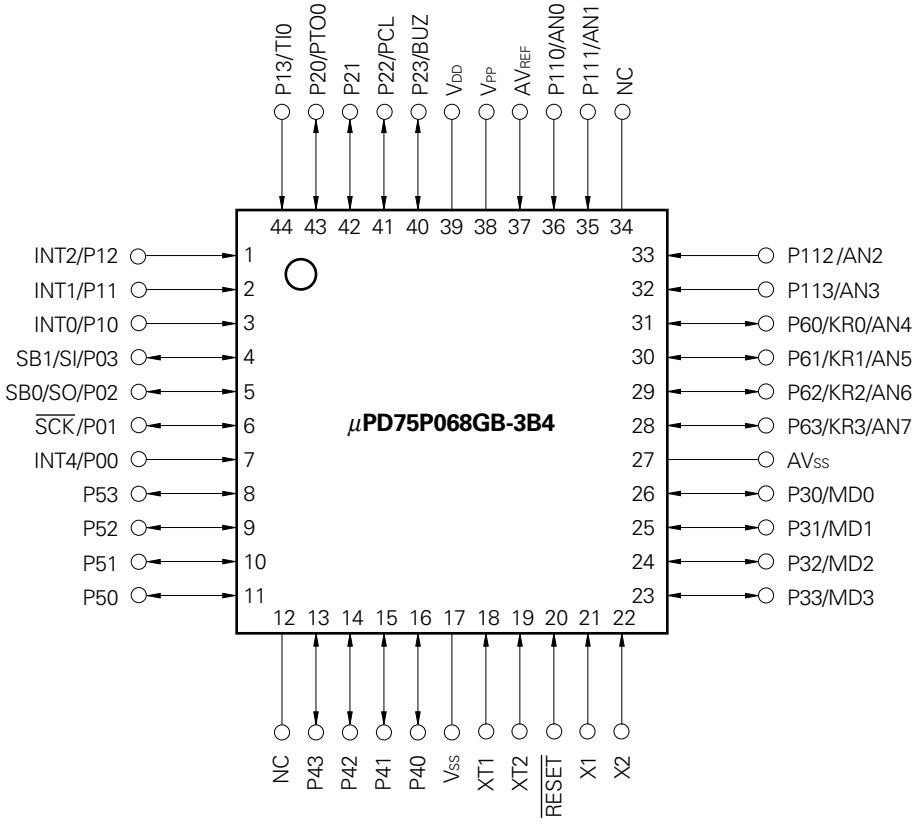
Major changes in this revision are indicated by stars (★) in the margins.

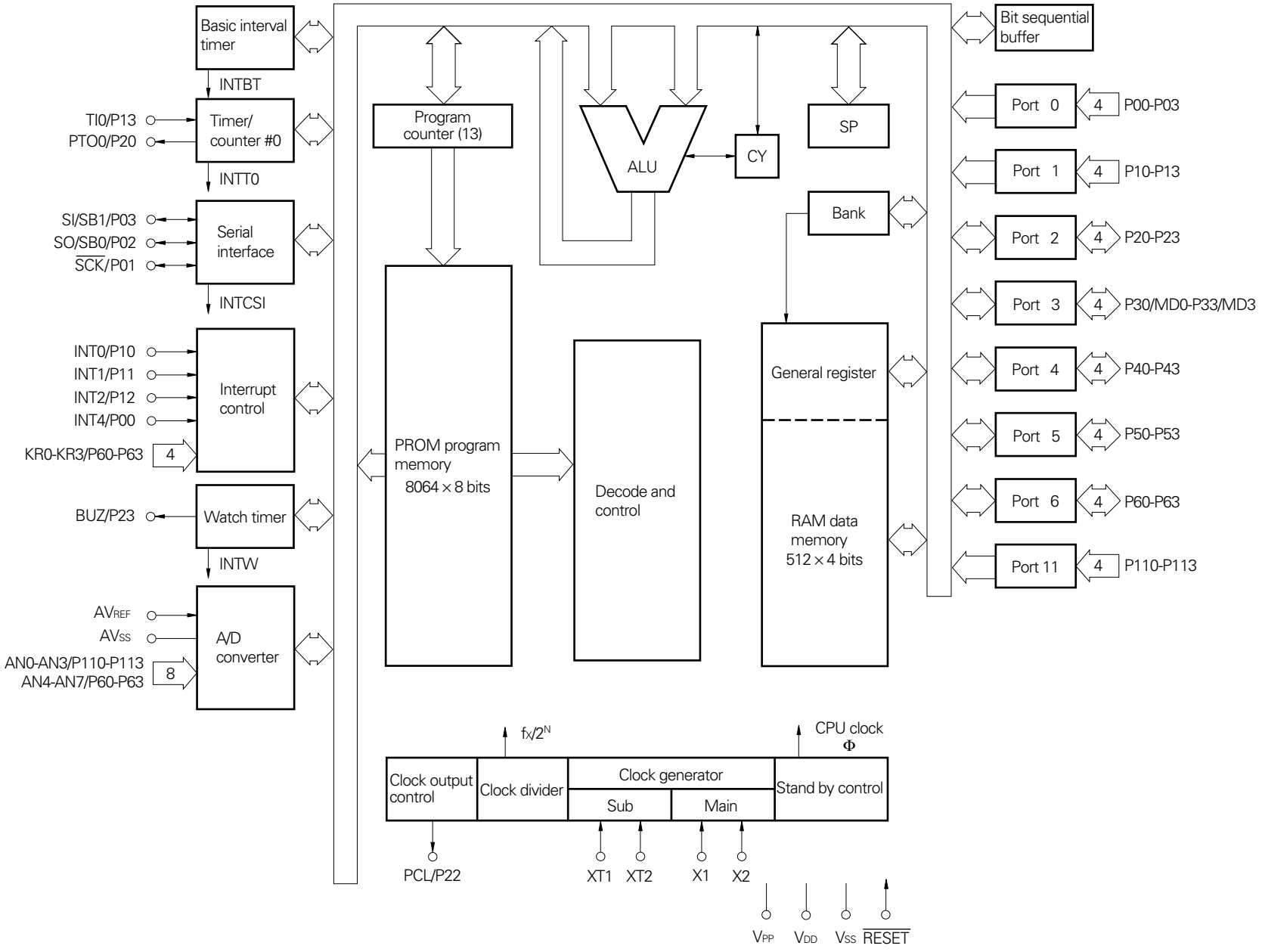
PIN CONFIGURATION (TOP VIEW)

- **42-pin plastic shrink DIP**



- **44-pin plastic QFP**




Basic interval timer
INTBT
TI0/P13
PTO0/P20
Timer/ counter #0
INTT0
SI/SB1/P03
SO/SB0/P02
SCK/P01
Serial interface
INTCSI
INT0/P10
INT1/P11
INT2/P12
INT4/P00
KR0-KR3/P60-P63
4
Interrupt control
BUZ/P23
Watch timer
INTW
AVREF
AVSS
AN0-AN3/P110-P113
AN4-AN7/P60-P63
8
A/D converter
Program counter (13)
ALU
CY
SP
Bank
PROM program memory
8064 × 8 bits
Decode and control
General register
RAM data memory
512 × 4 bits
Bit sequential buffer
Port 0
4
P00-P03
Port 1
P10-P13
Port 2
P20-P23
Port 3
P30/MD0-P33/MD3
Port 4
P40-P43
Port 5
P50-P53
Port 6
P60-P63
Port 11
P110-P113
fX/2N
CPU clock
Φ
Clock output control
Clock divider
Clock generator
Sub
Main
Stand by control
PCL/P22
XT1
XT2
X1
X2
VPP
VDD
VSS
RESET

CONTENTS

1. PIN FUNCTIONS

1.1 PORT PINS

Pin	Input/ output	Shared pin	Function	8 bit I/O	When reset	I/O circuit type[Note 1]
P00	Input	INT4	4-bit input port (PORT0). For P01-P03, pull-up resistors can be provided by software in units of 3 bits.	×	Input	Ⓑ
P01	I/O	$\overline{SCK}$				Ⓕ-A
P02	I/O	SO/SB0				Ⓕ-B
P03	I/O	SI/SB1				Ⓜ-C
P10	Input	INT0	With noise elimination function	×	Input	Ⓑ-C
P11		INT1	4-bit input port (PORT1). Pull-up resistors can be provided by software in units of 4 bits.			
P12		INT2				
P13		TI0				
P20	I/O	PTO0	4-bit I/O port (PORT2). Pull-up resistors can be provided by software in units of 4 bits.	×	Input	E-B
P21		—				
P22		PCL				
P23		BUZ				
P30[Note 2]	I/O	MD0	Programmable 4-bit I/O port (PORT3). I/O can be specified bit by bit. Pull-up resistors can be provided by software in units of 4 bits.	×	Input	E-B
P31[Note 2]		MD1				
P32[Note 2]		MD2				
P33[Note 2]		MD3				
P40-P43[Note 2]	I/O	—	N-ch open-drain 4-bit I/O port (PORT4). Withstand voltage of 10 V Data input-output (low-order 4 bits) when writing to and verifying program memory (PROM)	○	High Impedance	M-A
P50-P53[Note 2]	I/O	—	N-ch open-drain 4-bit I/O port (PORT5). Withstand voltage of 10 V Data input-output (high-order 4 bits) when writing to and verifying program memory (PROM)		High Impedance	M-A
P60	I/O	KR0/AN4	Programmable 4-bit I/O port (PORT6). Pull-up resistors can be provided by software in units of 4 bits.	×	Input	Ⓨ-D
P61		KR1/AN5				
P62		KR2/AN6				
P63		KR3/AN7				
P110	Input	AN0	4-bit input port (PORT11)	×	Input	Y-A
P111		AN1				
P112		AN2				
P113		AN3				

Notes 1. The circle (○) indicates the Schmitt trigger input.

2. Can directly drive the LED.

1.2 NON-PORT PINS

Pin	Input/ output	Shared pin	Function		When reset	I/O circuit type[Note 1]
TI0	Input	P13	Input for receiving external event pulse signal for timer/event counter		Input	Ⓑ-C
PTO0	I/O	P20	Timer/event counter output		Input	E-B
PCL	I/O	P22	Clock output		Input	E-B
BUZ	I/O	P23	Output for arbitrary frequency output (for buzzer output or system clock trimming)		Input	E-B
$\overline{SCK}$	I/O	P01	Serial clock I/O		Input	Ⓕ-A
SO/SB0	I/O	P02	Serial data output Serial bus I/O		Input	Ⓕ-B
SI/SB1	I/O	P03	Serial data input Serial bus I/O		Input	Ⓜ-C
INT4	Input	P00	Edge detection vectored interrupt input (either rising edge or falling edge detection)		Input	Ⓑ
INT0	Input	P10	Edge detection vectored interrupt input (detection edge selectable)		Input	Ⓑ-C
INT1		P11				
INT2	Input	P12	Edge detection testable input (rising edge detection)		Input	Ⓑ-C
KR0-KR3	I/O	P60-P63/ AN4-AN7	Parallel falling edge detection testable input		Input	Ⓨ-D
AN0-AN3	Input	P110-P113	For A/D converter only	8-bit analog input	—	Y-A
AN4-AN7	I/O	P60-P63/ KR0-KR3				Ⓨ-D
AV_{REF}	Input	—		Reference voltage input	—	Z
AV_{SS}	—	—		GND potential	—	Z
X1, X2	Input	—	Crystal/ceramic connection for main system clock generation. When external clock signal is used, it is applied to X1, and its reverse phase signal is applied to X2.		—	—
XT1, XT2	Input	—	Crystal connection for subsystem clock generation. When external clock signal is used, it is applied to XT1, and its reverse phase signal is applied to XT2. XT1 can be used as a 1-bit input (test).		—	—
$\overline{RESET}$	Input	—	System reset input		—	Ⓑ
MD0-MD3	I/O	P30-P33	Mode selection when writing to or verifying program memory (PROM)		Input	E-B
V_{PP}[Note 2]	—	—	Programming voltage application when writing to or verifying program memory (PROM) Directly connected to V_{DD} during normal operation. +12.5 V is applied when data is written in PROM or when the PROM is verified.		—	—
V_{DD}	—	—	Main power supply		—	—
V_{SS}	—	—	GND potential		—	—

Notes 1. The circle (○) indicates the Schmitt trigger input.

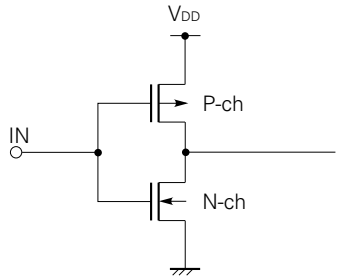
2. Unless the V_{PP} pin is directly connected to the V_{DD} pin during normal operation, the μPD75P068 does not operate normally.

1.3 PIN INPUT/OUTPUT CIRCUITS

The input/output circuit of each μPD75P068 pin is shown below in a simplified manner.

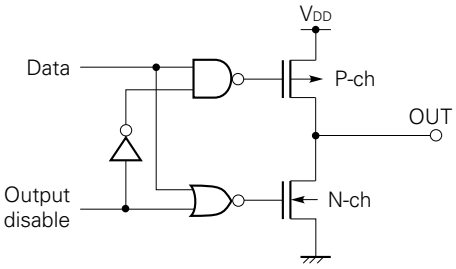
(1/3)

Type A (For type E-B)



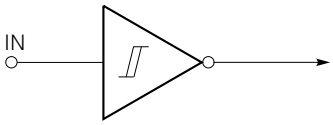
CMOS input buffer

Type D (For type E-B,F-A)



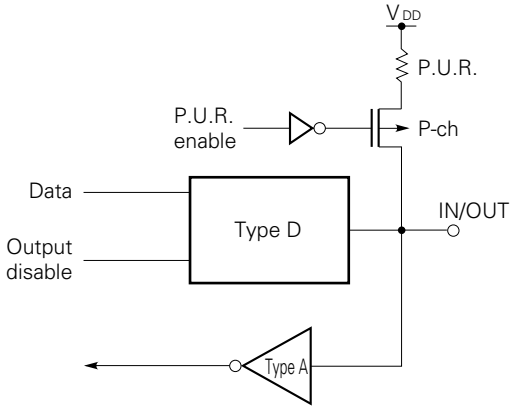
Push-pull output which can be set to high-impedance output (off for both P-ch and N-ch)

Type B



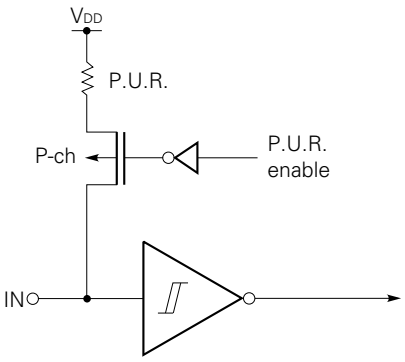
Schmitt trigger input with hysteresis

Type E-B



P.U.R.: Pull-up resistor

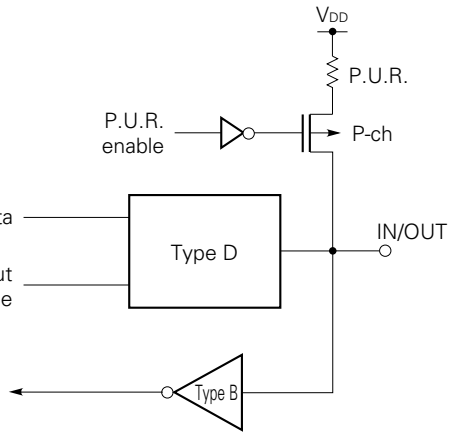
Type B-C



P.U.R.: Pull-up resistor

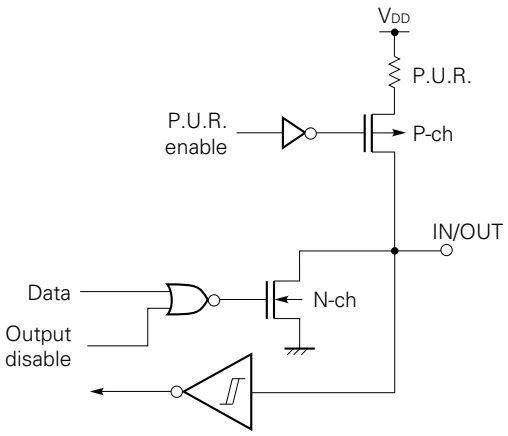
(2/3)

Type F-A



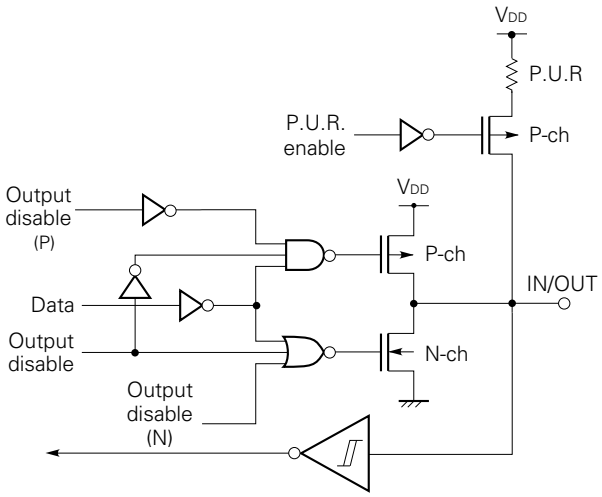
P.U.R.: Pull-up resistor

Type M-C



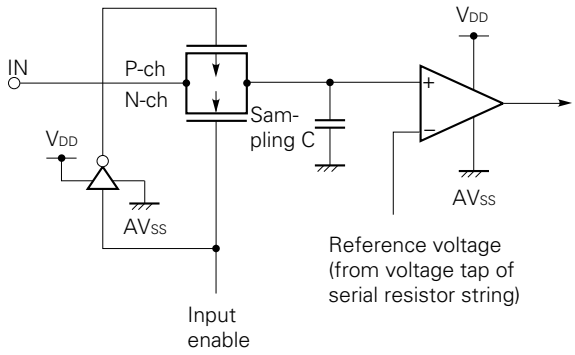
P.U.R.: Pull-up resistor

Type F-B

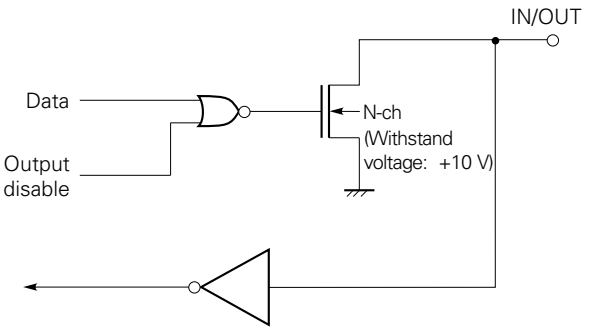


P.U.R.: Pull-up resistor

Type Y (For type Y-A , Y-D)



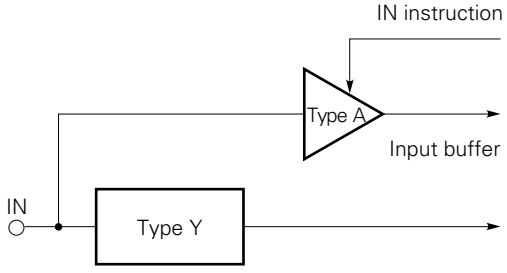
Type M-A



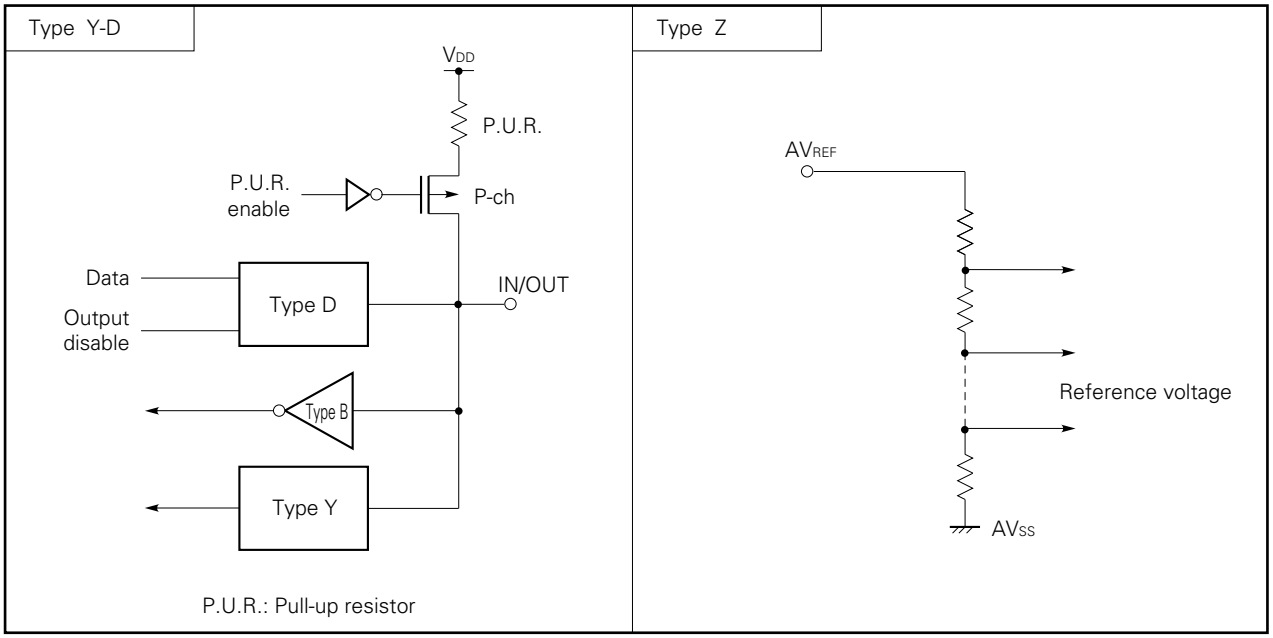
Input buffer with an intermediate withstand voltage of +10 V

P.U.R.: Pull-up resistor

Type Y-A ★



(3/3)



2. DIFFERENCE BETWEEN THE μPD75P068 AND μPD75068

The μPD75P068 is produced by replacing the internal mask ROM (program memory) of the μPD75068 with a one-time PROM in which data can be written once. Both have the same CPU function and internal hardware. Table 2-1 shows the difference between the μPD75P068 and μPD75068.

For details of the CPU function and internal hardware, refer to the individual references for the μPD75068.

Table 2-1 Difference between the μPD75P068 and μPD75068

Item		μPD75P068 (One-time PROM product)	μPD75P068 (Mask ROM product)
Program memory		• 0000H to 1F7FH • 8064 words × 8 bits	
Pull-up resistor	Ports 0 to 3 and 6	Can be specified with software.	
	Ports 4 and 5	None	Mask option
XT1 feedback resistor		Contained	Mask option
Operating supply voltage range		2.7 to 6.0 V	
Pin function	Pins 6 to 9 of SDIP Pins 23 to 26 of QFP	P30/MD0 to P33/MD3	P30 to P33
	Pin 20 of SDIP Pin 38 of QFP	V_{PP}	IC
Electrical characteristics		They differ in consumption current. For details, refer to the corresponding items in each data sheet.	
Others		Since they differ in circuit scale and mask layout, they differ in noise immunity and noise radiation.	

Caution The PROM and mask ROM products differ in noise immunity and noise radiation. Use not ES products but CS products (mask ROM products) to evaluate them thoroughly when considering the change from the PROM products to the mask ROM products during processes from preproduction to volume production.

3. WRITING TO AND VERIFYING PROM (PROGRAM MEMORY)

The program memory in the μPD75P068 is a one-time PROM which consists of 8064 words × 8 bits. Writing to and verifying the contents of the one-time PROM is accomplished using the pins shown in the table below. Note that address inputs are not used; instead, the address is updated using the clock input from the X1 pin.

Pin name	Function
V_{PP}	Voltage is applied to this pin when writing to the program memory or verifying its contents (normally V_{DD} electric potential).
X1, X2	Address update clock inputs used when writing to the program memory or verifying its contents. The X2 pin is used to input the inverted signal of the X1 pin input.
MD0 to MD3 (P30 to P33)	Operation mode selection pins used when writing to the program memory or verifying its contents.
P40 to P43 (low-order four bits) P50 to P53 (high-order four bits)	I/O pins for 8-bit data used when writing to the program memory or verifying its contents.
V_{DD}	Power voltage is applied to this pin. During normal operation, 2.7 to 6.0 V should be applied; 6 V should be applied when writing to the program memory or verifying its contents.

Caution Since the μPD75P068CU/GB does not have an erasure window, the contents of the memory can not be erased with ultraviolet radiation.

3.1 OPERATING MODES WHEN WRITING TO AND VERIFYING THE PROGRAM MEMORY

If +6 V is applied to the V_{DD} pin and +12.5 V is applied to the V_{PP} pin, the μPD75P068 enters program memory write/verify mode. The specific operating mode is then selected by setting the MD0 through MD3 pins as listed below. The remaining pins are all connected to V_{SS} via pull-down resistors.

Operating mode specification						Operating mode
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
+12.5 V	+6 V	H	L	H	L	Program memory address clear mode
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	×	H	H	Program inhibit mode

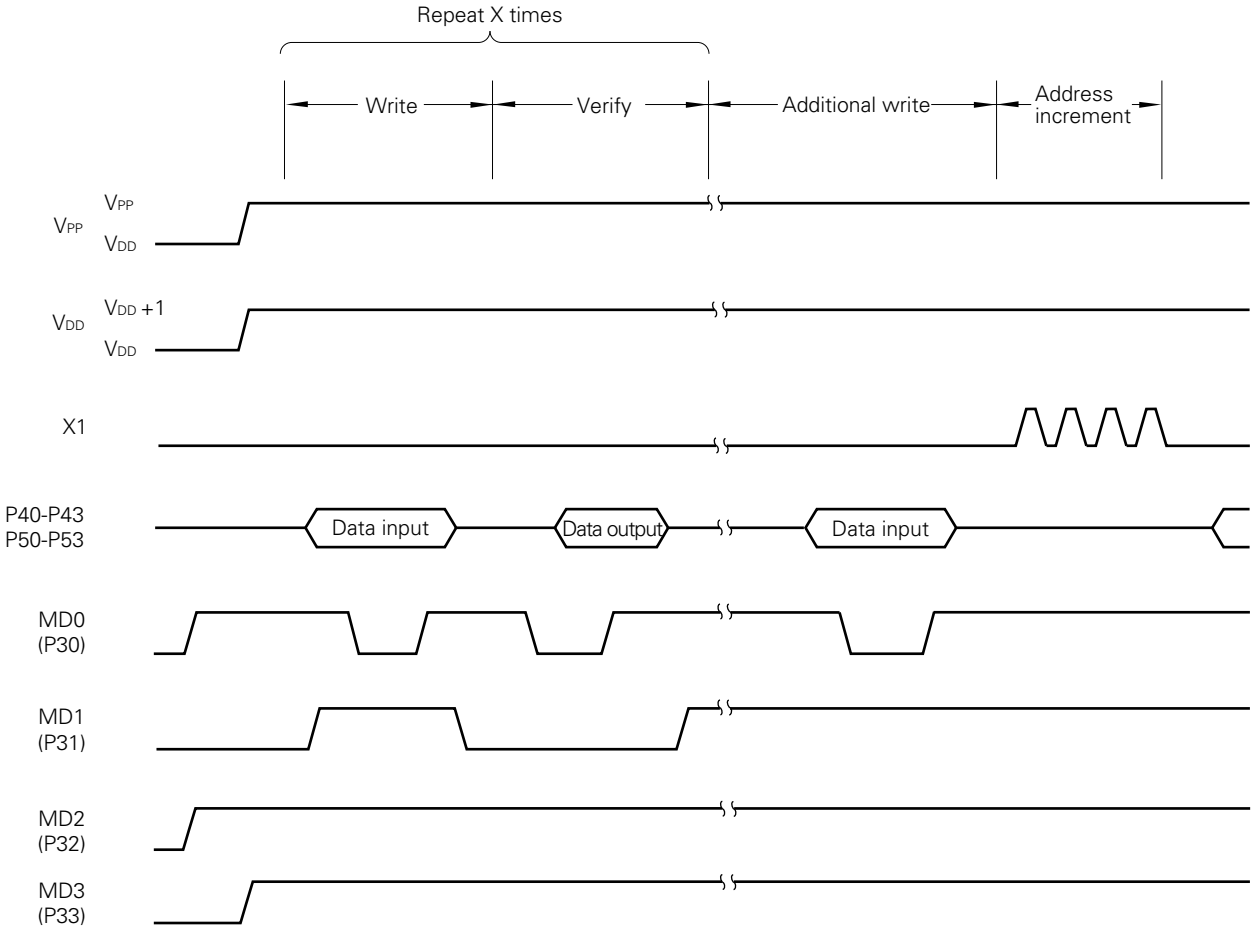
× indicates L or H.

3.2 WRITING TO THE PROGRAM MEMORY

The procedure for writing to program memory is described below; high-speed write is possible.

(1) Connect all unused pins to V_{SS} through resistors. Apply a low-level signal to the X1 pin.
(2) Apply 5 V to V_{DD} and V_{PP} pins.
(3) Wait 10 μs.
(4) Select program memory address clear mode.
(5) Apply +6 V to V_{DD} and +12.5 V to V_{PP}.
(6) Select program inhibit mode.
(7) Select write mode for 1 ms duration and write data.
(8) Select program inhibit mode.
(9) Select verify mode. If write is successful, proceed to step (10). If write fails, repeat steps (7) to (9).
(10) Perform additional write for (Number (X) of repetitions of steps (7) to (9)) × 1 ms duration.
(11) Select program inhibit mode.
(12) Increment the program memory address by inputting four pulses on the X1 pin.
(13) Repeat steps (7) to (12) until the last address is reached.
(14) Select program memory address clear mode.
(15) Apply 5 V to V_{DD} and V_{PP} pins.
(16) Turn the power off.

The timing for steps (2) to (12) is shown below.

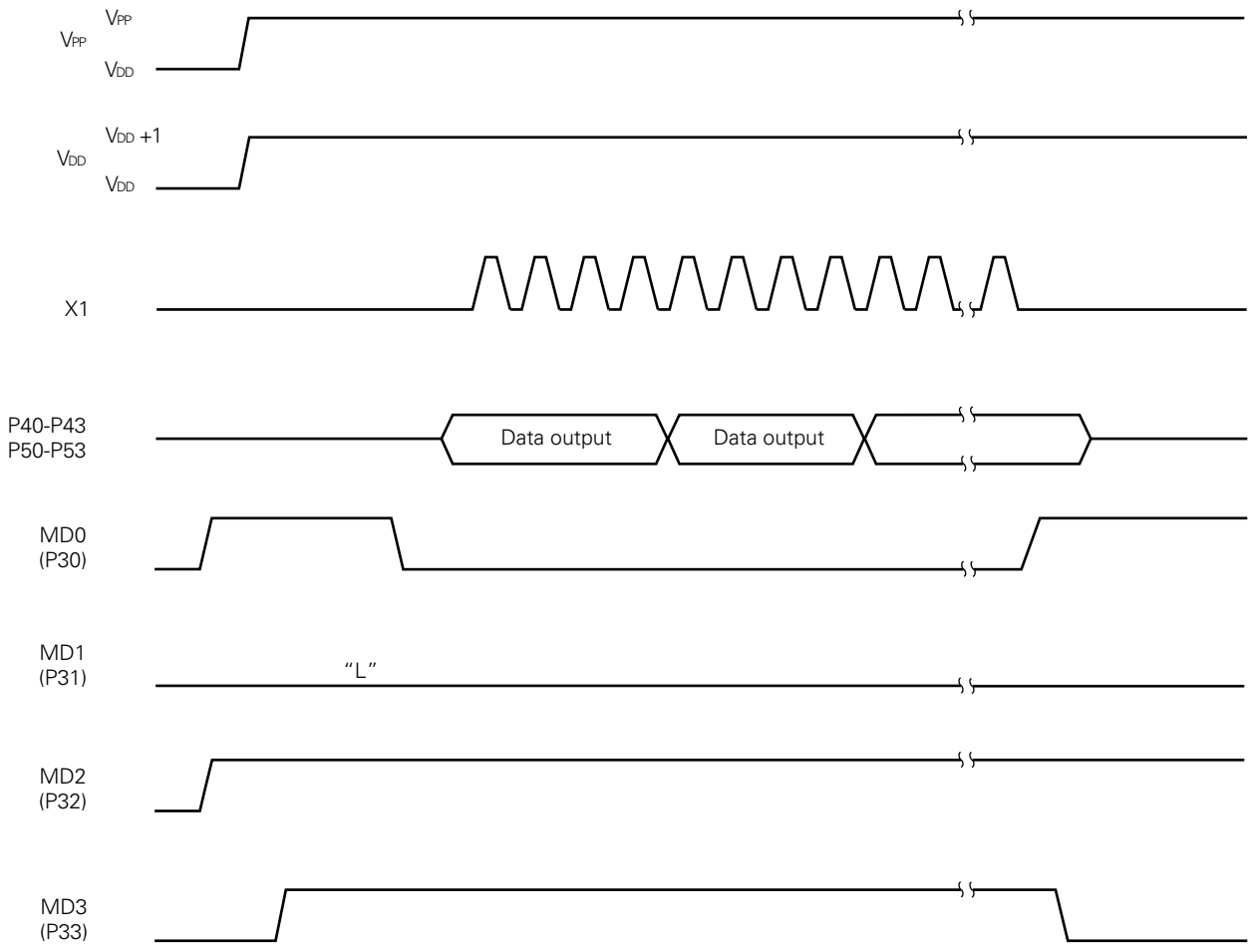


3.3 READING THE PROGRAM MEMORY

The procedure for reading the contents of program memory is described below. The read is performed in the verify mode.

(1) Connect all unused pins to V_{SS} through resistors. Apply a low-level signal to the X1 pin.
(2) Apply 5 V to V_{DD} and V_{PP} pins.
(3) Wait 10 μs.
(4) Select program memory address clear mode.
(5) Apply +6 V to V_{DD} and +12.5 V to V_{PP}.
(6) Select program inhibit mode.
(7) Select verify mode. Data is output sequentially one address at a time for each cycle of four clock pulses appearing on the X1 pin.
(8) Select program inhibit mode.
(9) Select program memory address clear mode.
(10) Apply 5 V to V_{DD} and V_{PP} pins.
(11) Turn the power off.

The timing for steps (2) to (9) is shown below.



4. SCREENING ONE-TIME PROM PRODUCTS ★

NEC cannot execute a complete test of one-time PROM products (μPD75P068CU and μPD75P068GB-3B4) due to their structure before shipment. It is recommended that you screen (verify) PROM products after writing necessary data into them and storing them at 125 °C for 24 hours.

NEC offers a charged service called QTOP microcomputer service. This service includes writing to one-time PROM, marking, screening, and verification.

Ask your sales representative for details.

5. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Parameter	Symbol	Conditions		Rated value	Unit
Supply voltage	V_{DD}			–0.3 to +7.0	V
Supply voltage	V_{PP}			–0.3 to +13.5	V
Input voltage	V_{I1}	Ports other than ports 4 and 5		–0.3 to V_{DD} + 0.3	V
	V_{I2}	Ports 4 and 5	N-ch open drain	–0.3 to +11	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
High-level output current	I_{OH}	1 pin		–10	mA
		All pins		–30	mA
Low-level output current	I_{OL} **Note**	1 pin of ports 0, 3, 4, and 5	Peak value	30	mA
			rms	15	mA
		1 pin of ports 2 and 6	Peak value	20	mA
			rms	5	mA
		Total of all pins of ports 0, 3, 4, and 5	Peak value	160	mA
			rms	120	mA
		Total of all pins of ports 2, and 6	Peak value	30	mA
			rms	20	mA
Operating temperature	T_{opt}			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

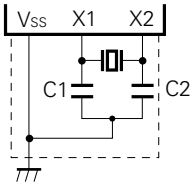
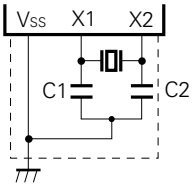
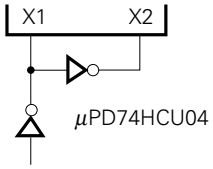
Note Calculate rms with [rms] = [peak value] × $\sqrt{\text{duty}}$.

Caution Absolute maximum ratings are rated values beyond which some physical damages may be caused to the product; if any of the parameters in the table above exceeds its rated value even for a moment, the quality of the product may deteriorate. Be sure to use the product within the rated values.

CAPACITANCE (T_a = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_I	f = 1 MHz 0 V for pins other than pins to be measured			15	pF
Output capacitance	C_O				15	pF
I/O capacitance	C_{IO}				15	pF

CHARACTERISTICS OF THE MAIN SYSTEM CLOCK OSCILLATOR (T_a = -40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

Resonator	Recommended constant	Parameter	Conditions	Min.	Typ.	Max.	Unit
Ceramic resonator		Oscillator frequency (f_X) **Note 1**		1.0		5.0**Note 3**	MHz
		Oscillation settling time **Note 2**				4	ms
Crystal		Oscillator frequency (f_X) **Note 1**		1.0	4.19	5.0**Note 3**	MHz
		Oscillation settling time **Note 2**	V_{DD} = 4.5 to 6.0 V			10	ms
						30	ms
External clock		X1 input frequency (f_X) **Note 1**		1.0		5.0**Note 3**	MHz
		X1 input high/low level width (t_{XH}, t_{XL})		100		500	ns

Notes 1. The oscillator frequency and input frequency indicate only the oscillator characteristics. See the item of AC characteristics for the instruction execution time.

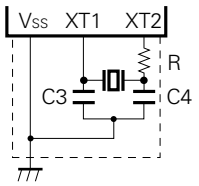
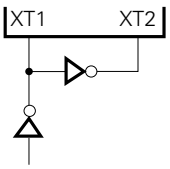
2. The oscillation settling time means the time required for the oscillation to settle after V_{DD} is reaches the minimum voltage in the oscillation voltage range.

3. When 4.19 MHz < $f_X \leq$ 5.0 MHz, do not select PCC = 0011 as the instruction execution time. When PCC = 0011, one machine cycle falls short of 0.95 μs, the minimum value for the standard.

Caution When the main system clock oscillator is used, conform to the following guidelines when wiring at the portions surrounded by dotted lines in the figures above to eliminate the influence of the wiring capacity.

- **The wiring must be as short as possible.**
- **Other signal lines must not run in these areas.**
- **Any line carrying a high fluctuating current must be kept away as far as possible.**
- **The grounding point of the capacitor of the oscillator must have the same potential as that of V_{DD}. It must not be grounded to ground patterns carrying a large current.**
- **No signal must be taken from the oscillator.**

CHARACTERISTICS OF THE SUBSYSTEM CLOCK OSCILLATOR (T_a = -40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

Resonator	Recommended constant	Parameter	Conditions	Min.	Typ.	Max.	Unit
Crystal		Oscillator frequency (f_{XT}) **Note 1**		32	32.768	35	kHz
		Oscillation settling time **Note 2**	V_{DD} = 4.5 to 6.0 V		1.0	2	s
						10	s
External clock		XT1 input frequency (f_{XT}) **Note 1**		32		100	kHz
		XT1 input high/low level width (t_{XTH}, t_{XTL})		5		15	μs

Notes 1. The oscillator frequency and input frequency indicate only the oscillator characteristics. See the item of AC characteristics for the instruction execution time.

2. The oscillation settling time means the time required for the oscillation to settle after V_{DD} reaches the minimum voltage in the oscillation voltage range.

Caution When the subsystem clock oscillator is used, conform to the following guidelines when wiring at the portions surrounded by dotted lines in the figures above to eliminate the influence of the wiring capacity.

- **The wiring must be as short as possible.**
- **Other signal lines must not run in these areas.**
- **Any line carrying a high fluctuating current must be kept away as far as possible.**
- **The grounding point of the capacitor of the oscillator must have the same potential as that of V_{SS}. It must not be grounded to ground patterns carrying a large current.**
- **No signal must be taken from the oscillator.**

When the subsystem clock is used, pay special attention to its wiring; the subsystem clock oscillator has low amplification to minimize current consumption and is more likely to malfunction due to noise than the main system clock oscillator.

RECOMMENDED CAPACITORS IN THE OSCILLATION CIRCUIT ★

Main system clock: Ceramic resonator (T_a = –20 to +80°C)

Manufacturer	Part number	Frequency (MHz)	Recommended constant		Oscillation voltage range	
			C1 (pF)	C2 (pF)	Min. (V)	Max. (V)
Kyocera	KBR-1000F/Y	1.00	150	150	2.7	6.0
	KBR-2.0MS	2.00	47	47		
	PBRC 2.00A					
	KBR-3.0MS	3.00	33	33		
	KBR-3.58MSA	3.58				
	PBRC 3.58A					
	KBR-3.58MKS		Contained	Contained		
	KBR-3.58MWS					
	KBR-4.00MSA	4.00	33	33		
	PBRC 4.00A					
	KBR-4.00MKS		Contained	Contained		
	KBR-4.00MWS					
	KBR-5.0MSA	5.00	33	33		
	PBRC 5.00A					
	KBR-5.0MKS		Contained	Contained		
	KBR-5.0MWS					
Toko	CRHF2.50	2.50	30	30	2.7	6.0
	CRHF4.19	4.19				
	CRHT4.19		Contained	Contained		
	CRHF5.00	5.00	30	30		

Main system clock: Crystal (T_a = –40 to +85°C)

Manufacturer	Part number	Frequency (MHz)	Recommended constant		Oscillation voltage range	
			C1 (pF)	C2 (pF)	Min. (V)	Max. (V)
Kinseki	HC-49/U	2.00	22	22	3.5	6.0
		4.19				
		6.00				

Subsystem clock: Crystal (T_a = –15 to +60°C)

Manufacturer	Part number	Frequency (kHz)	Recommended constant			Oscillation voltage range	
			C3 (pF)	C4 (pF)	R (kΩ)	Min. (V)	Max. (V)
Kyocera	KF-38G	32.768	15	27	220	2.7	6.0

DC CHARACTERISTICS (T_a = -40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
High-level input voltage	V_{IH1}	Ports 2, 3, and 11		0.7V_{DD}		V_{DD}	V
	V_{IH2}	Ports 0, 1, and 6, and $\overline{\text{RESET}}$		0.8V_{DD}		V_{DD}	V
	V_{IH3}	Ports 4 and 5		0.7V_{DD}		10	V
	V_{IH4}	X1, X2, XT1, and XT2		V_{DD} – 0.5		V_{DD}	V
Low-level input voltage	V_{IL1}	Ports 2 to 5 and 11		0		0.3V_{DD}	V
	V_{IL2}	Ports 0, 1, and 6, and $\overline{\text{RESET}}$		0		0.2V_{DD}	V
	V_{IL3}	X1, X2, XT1, and XT2		0		0.4	V
High-level output voltage	V_{OH}	V_{DD} = 4.5 to 6.0 V, I_{OH} = –1 mA		V_{DD} – 1.0			V
		I_{OH} = –100 μA		V_{DD} – 0.5			V
Low-level output voltage	V_{OL}	Ports 4 and 5	V_{DD} = 4.5 to 6.0 V, I_{OL} = 15 mA		0.7	2.0	V
		Port 3	V_{DD} = 4.5 to 6.0 V, I_{OL} = 15 mA		0.8	2.0	V
		V_{DD} = 4.5 to 6.0 V, I_{OL} = 1.6 mA				0.4	V
		I_{OL} = 400 μA				0.5	V
		SB0 and SB1	Pull-up resistor: 1 kΩ or more			0.2V_{DD}	V
High-level input leakage current	I_{LIH1}	V_I = V_{DD}	Other than X1, X2, XT1, and XT2			3	μA
	I_{LIH2}		X1, X2, XT1, and XT2			20	μA
	I_{LIH3}	V_I = 10 V	Ports 4 and 5			20	μA
Low-level input leakage current	I_{LIL1}	V_I = 0 V	Other than X1, X2, XT1, and XT2			–3	μA
	I_{LIL2}		X1, X2, XT1, and XT2			–20	μA
High-level output leakage current	I_{LOH1}	V_O = V_{DD}				3	μA
	I_{LOH2}	V_O = 10 V	Ports 4 and 5			20	μA
Low-level out-put leakage current	I_{LOL}	V_O = 0 V				–3	μA
Built-in pull-up resistor	R_U	P01, P02, P03, and ports 1 to 3, and 6 V_I = 0 V	V_{DD} = 5.0 V ±10 %	15	40	80	kΩ
			V_{DD} = 3.0 V ±10 %	30		300	kΩ
Power supply current[Note 1]	I_{DD1}	4.19 MHz[Note 2] crystal resonance C1 = C2 = 22 pF	V_{DD} = 5.0 V ±10 %[Note 3]		3.3	10	mA
			V_{DD} = 3.0 V ±10 %[Note 4]		0.45	1.4	mA
	I_{DD2}		HALT mode, V_{DD} = 5.0 V ±10 %		600	1800	μA
			HALT mode, V_{DD} = 3.0 V ±10 %		220	700	μA
	I_{DD3}	32.768 kHz[Note 5] crystal resonance	V_{DD} = 3.0 V ±10 %		35	120	μA
	I_{DD4}		HALT mode, V_{DD} = 3.0 V ±10 %		5	15	μA
	I_{DD5}	XT1 = 0 V	V_{DD} = 5.0 V ±10 %		0.5	20	μA
			V_{DD} = 3.0 V ±10 %		0.1	10	μA
			3.0 V ±10 %, T_a = 25 °C		0.1	5	μA

Notes 1. This current excludes the current which flows through the built-in pull-up resistors.

2. This value applies also when the subsystem clock oscillates.

3. Value when the processor clock control register (PCC) is set to 0011 and the μPD75036 is operated in the high-speed mode

4. Value when the PCC is set to 0000 and the μPD75036 is operated in the low-speed mode

5. This value applies when the system clock control register (SCC) is set to 1001 to stop the main system clock pulse and to start the subsystem clock pulse.

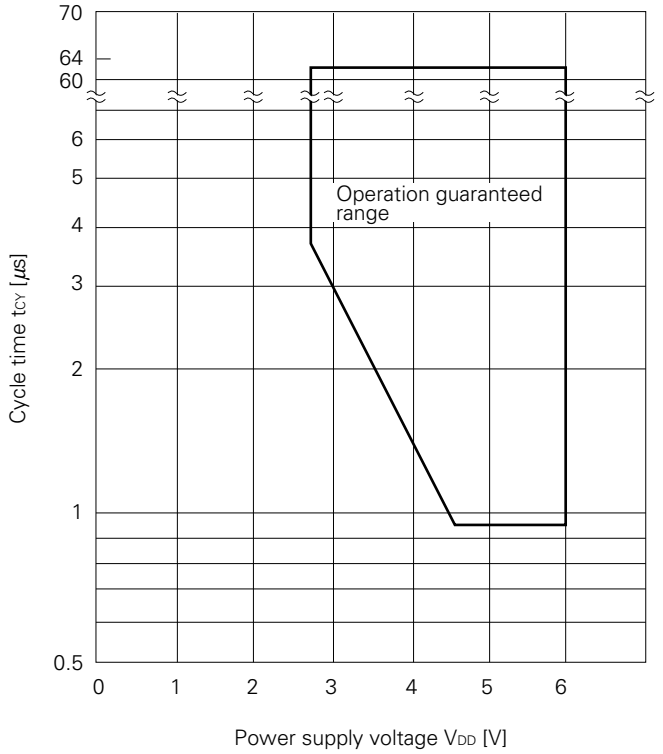
AC CHARACTERISTICS (T_a = -40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
CPU clock cycle time (minimum instruction execution time = 1 machine cycle)**Note 1**	t_{CY}	Operated by main system clock pulse	V_{DD} = 4.5 to 6.0 V	0.95		64	μs
				3.8		64	μs
		Operated by subsystem clock pulse		114	122	125	μs
TI0 input frequency	f_{TI}	V_{DD} = 4.5 to 6.0 V		0		1	MHz
				0		275	kHz
TI0 input high/low level width	t_{TIH}, t_{TIL}	V_{DD} = 4.5 to 6.0 V		0.48			μs
				1.8			μs
Interrupt input high/low level width	t_{INTH}, t_{INTL}	INT0		**Note 2**			μs
		INT1, INT2, and INT4		10			μs
		KR0 to KR3		10			μs
$\overline{\text{RESET}}$ low level width	t_{RSL}			10			μs

Notes 1. The cycle time of the CPU clock (Φ) depends on the connected resonator frequency, the system clock control register (SCC), and the processor clock control register (PCC).
The figure on the right side shows the cycle time t_{CY} characteristics for the supply voltage V_{DD} during main system clock operation.

2. This value becomes $2t_{CY}$ or 128/fx according to the setting of the interrupt mode register (IM0).

t_{CY} vs V_{DD}
(Main system clock in operation)



SERIAL TRANSFER OPERATION

Two-wire and three-wire serial I/O modes ($\overline{SCK}$ ... Internal clock output):

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
$\overline{SCK}$ cycle time	t_{KCY1}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ high/low level width	t_{KL1}	V_{DD} = 4.5 to 6.0 V		$t_{KCY1}/2 - 50$			ns
	t_{KH1}			$t_{KCY1}/2 - 150$			ns
SI setup time (referred to $\overline{SCK}\uparrow$)	t_{SIK1}			150			ns
SI hold time (referred to $\overline{SCK}\uparrow$)	t_{KSI1}			400			ns
Delay time from $\overline{SCK}\downarrow$ to SO output	t_{KSO1}	R_L = 1 kΩ, C_L = 100 pF**Note**	V_{DD} = 4.5 to 6.0 V	0		250	ns
				0		1000	ns

Two-wire and three-wire serial I/O modes ($\overline{SCK}$ ... External clock input):

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
$\overline{SCK}$ cycle time	t_{KCY2}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high/low level width	t_{KL2}	V_{DD} = 4.5 to 6.0 V		400			ns
	t_{KH2}			1600			ns
SI setup time (referred to $\overline{SCK}\uparrow$)	t_{SIK2}			100			ns
SI hold time (referred to $\overline{SCK}\uparrow$)	t_{KSI2}			400			ns
Delay time from $\overline{SCK}\downarrow$ to SO output	t_{KSO2}	R_L = 1 kΩ, C_L = 100 pF**Note**	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns

Note R_L and C_L are the resistance and capacitance of the SO output line load respectively.

SBI mode ($\overline{SCK}$ ... Internal clock output (master)):

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
$\overline{SCK}$ cycle time	t_{KCY3}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ high/low level width	t_{KL3}	V_{DD} = 4.5 to 6.0 V		$t_{KCY3}/2$ - 50			ns
	t_{KH3}			$t_{KCY3}/2$ - 150			ns
SB0/SB1 setup time (referred to $\overline{SCK}\uparrow$)	t_{SIK3}			150			ns
SB0/SB1 hold time (referred to $\overline{SCK}\uparrow$)	t_{KSI3}			$t_{KCY3}/2$			ns
Delay time from $\overline{SCK}\downarrow$ to SB0/SB1 output	t_{KSO3}	R_L = 1 kΩ, C_L = 100 pF**Note**	V_{DD} = 4.5 to 6.0 V	0		250	ns
				0		1000	ns
From $\overline{SCK}\uparrow$ to SB0/SB1$\downarrow$	t_{KSB}			t_{KCY3}			ns
From SB0/SB1$\downarrow$ to $\overline{SCK}$	t_{SBK}			t_{KCY3}			ns
SB0/SB1 low level width	t_{SBL}			t_{KCY3}			ns
SB0/SB1 high level width	t_{SBH}			t_{KCY3}			ns

SBI mode ($\overline{SCK}$ ... External clock input (slave)):

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
$\overline{SCK}$ cycle time	t_{KCY4}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high/low level width	t_{KL4}	V_{DD} = 4.5 to 6.0 V		400			ns
	t_{KH4}			1600			ns
SB0/SB1 setup time (referred to $\overline{SCK}\uparrow$)	t_{SIK4}			100			ns
SB0/SB1 hold time (referred to $\overline{SCK}\uparrow$)	t_{KSI4}			$t_{KCY4}/2$			ns
Delay time from $\overline{SCK}\downarrow$ to SB0/SB1 output	t_{KSO4}	R_L = 1 kΩ, C_L = 100 pF**Note**	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns
From $\overline{SCK}\uparrow$ to SB0/SB1$\downarrow$	t_{KSB}			t_{KCY4}			ns
From SB0/SB1$\downarrow$ to $\overline{SCK}\downarrow$	t_{SBK}			t_{KCY4}			ns
SB0/SB1 low level width	t_{SBL}			t_{KCY4}			ns
SB0/SB1 high level width	t_{SBH}			t_{KCY4}			ns

Note R_L and C_L are the resistance and capacitance of the SB0/SB1 output line load respectively.

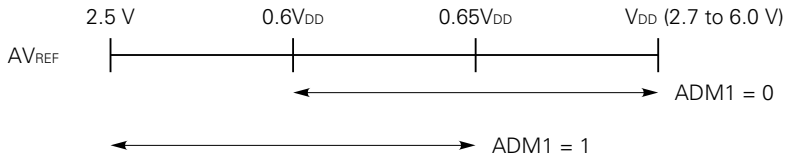
A/D CONVERTER (T_a = -40 to +85 °C, V_{DD} = 2.7 to 6.0 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Resolution				8	8	8	bit
Absolute accuracy[Note 1]		2.5 V ≤ AV_{REF} ≤ V_{DD}[Note 2]	-10 ≤ Ta ≤ +85°C			±1.5	LSB
			-40 ≤ Ta < -10°C			±2.0	LSB
Conversion time[Note 3]	t_{CONV}					168/f_X	μs
Sampling time[Note 4]	t_{SAMP}					44/f_X	μs
Reference input voltage	AV_{REF}			2.5		V_{DD}	V
Analog input voltage	V_{IAN}			AV_{SS}		AV_{REF}	V
Analog input impedance	R_{AN}				1000		MΩ
AV_{REF} current	AI_{REF}				0.7	2.0	mA

Notes 1. Absolute accuracy excluding quantization error (±1/2 LSB)

2. 2.5 V ≤ AV_{REF} ≤ V_{DD}

ADM1 is set to 0 or 1 depending on the A/D converter reference voltage (AV_{REF}) as follows:

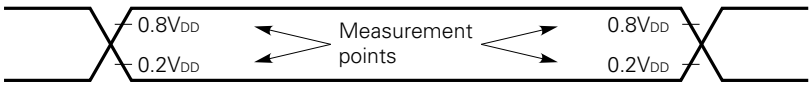


When 0.6V_{DD} ≤ AV_{REF} ≤ 0.65V_{DD}, ADM1 can be set to either 0 or 1.

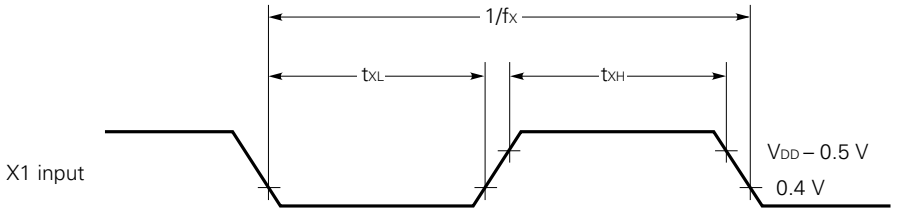
3. Time from the execution of a conversion start instruction till the end of conversion (EOC = 1) (40.1 μs: f_X = 4.19 MHz)

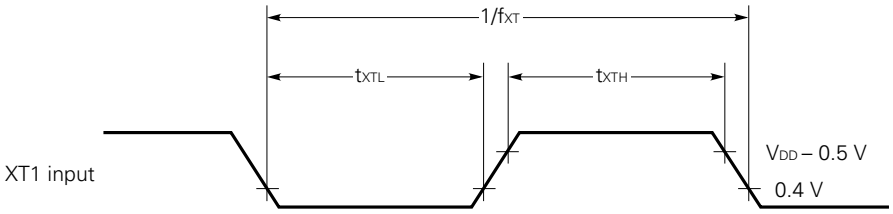
4. Time from the execution of a conversion start instruction till the end of sampling (10.5 μs: f_X = 4.19 MHz)

AC Timing Measurement Points (Excluding X1 and XT1 Inputs)

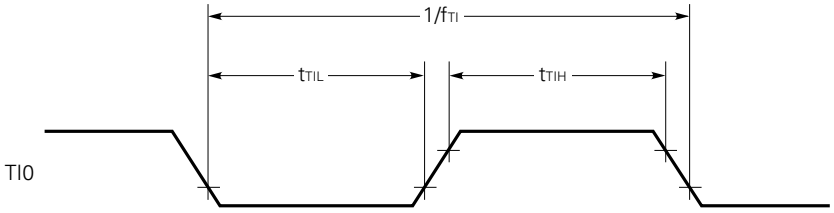


Clock Timing



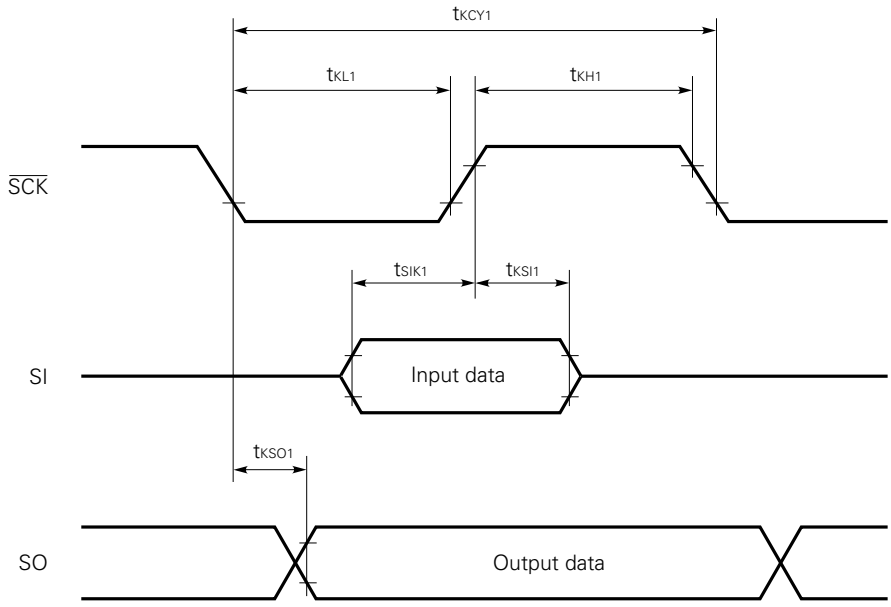


TI0 Timing

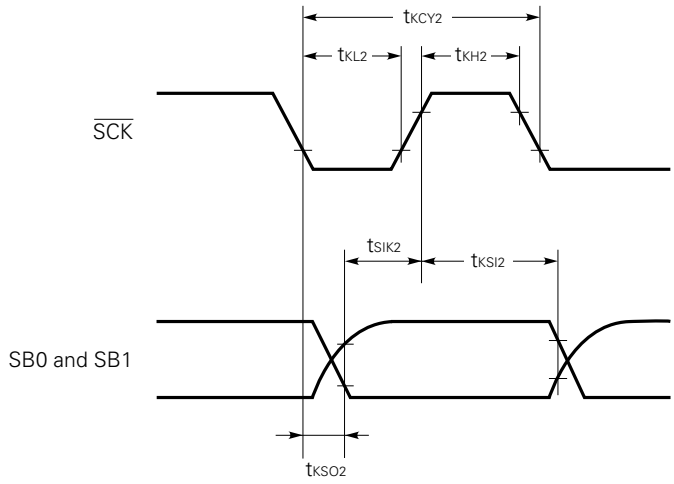


Serial Transfer Timing

Three-wire serial I/O mode:

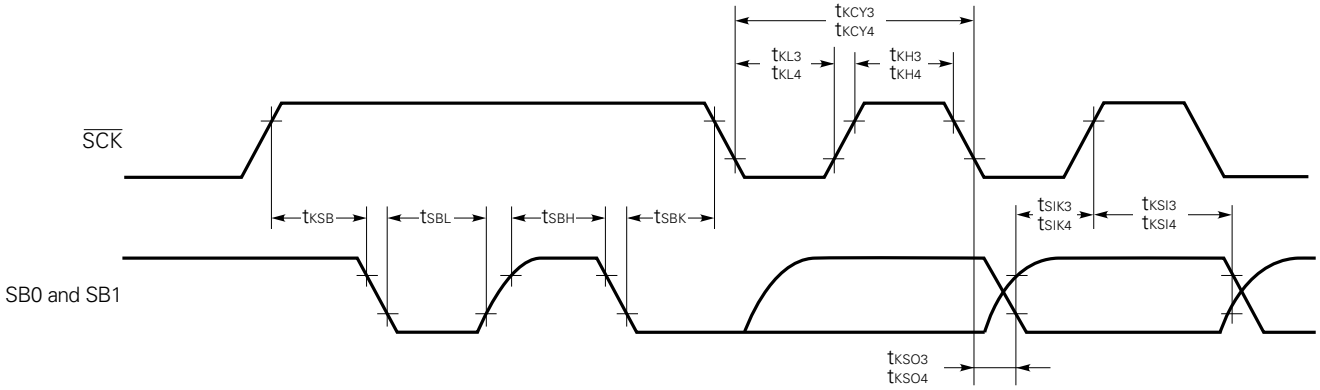


Two-wire serial I/O mode:

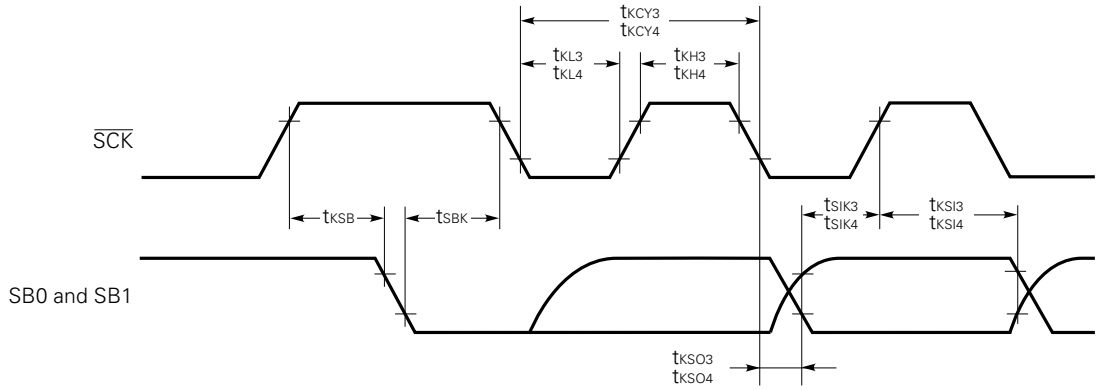


Serial Transfer Timing

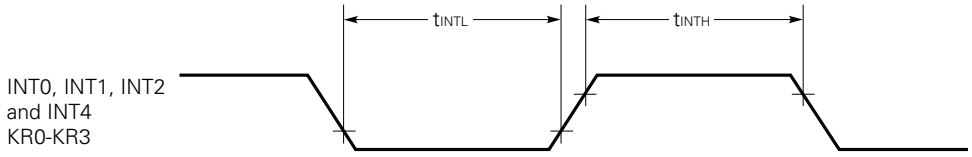
Bus release signal transfer:



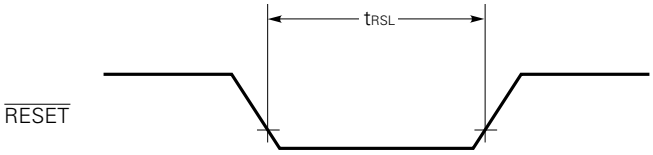
Command signal transfer:



Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



DATA HOLD CHARACTERISTICS BY LOW SUPPLY VOLTAGE IN DATA MEMORY STOP MODE

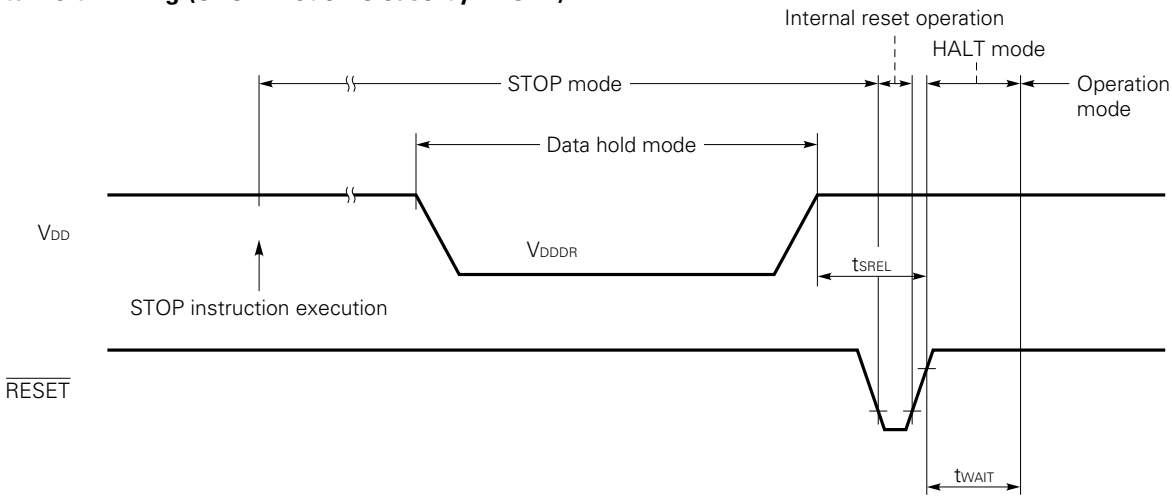
(T_a = -40 to +85 °C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data hold supply voltage	V_{DDDR}		2.0		6.0	V
Data hold supply current **Note 1**	I_{DDDR}	V_{DDDR} = 2.0 V		0.1	10	μA
Release signal setting time	t_{SREL}		0			μs
Oscillation settling time **Note 2**	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/f_X$		ms
		Release by interrupt request		**Note 3**		ms

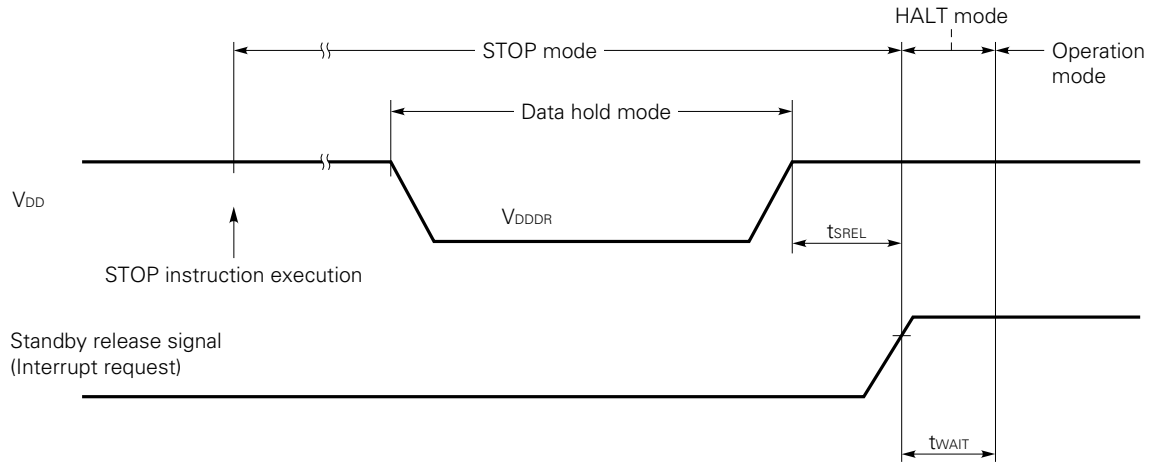
Notes 1. Excluding the current which flows through the built-in pull-up resistors
2. CPU operation stop time for preventing unstable operation at the beginning of oscillation
3. This value depends on the settings of the basic interval timer mode register (BTM) shown below.

BTM3	BTM2	BTM1	BTM0	Wait time (Values at f_X = 4.19 MHz in parentheses)
—	0	0	0	$2^{20}/f_X$ (approx. 250 ms)
—	0	1	1	$2^{17}/f_X$ (approx. 31.3 ms)
—	1	0	1	$2^{15}/f_X$ (approx. 7.82 ms)
—	1	1	1	$2^{13}/f_X$ (approx. 1.95 ms)

Data Hold Timing (STOP Mode Release by $\overline{RESET}$)

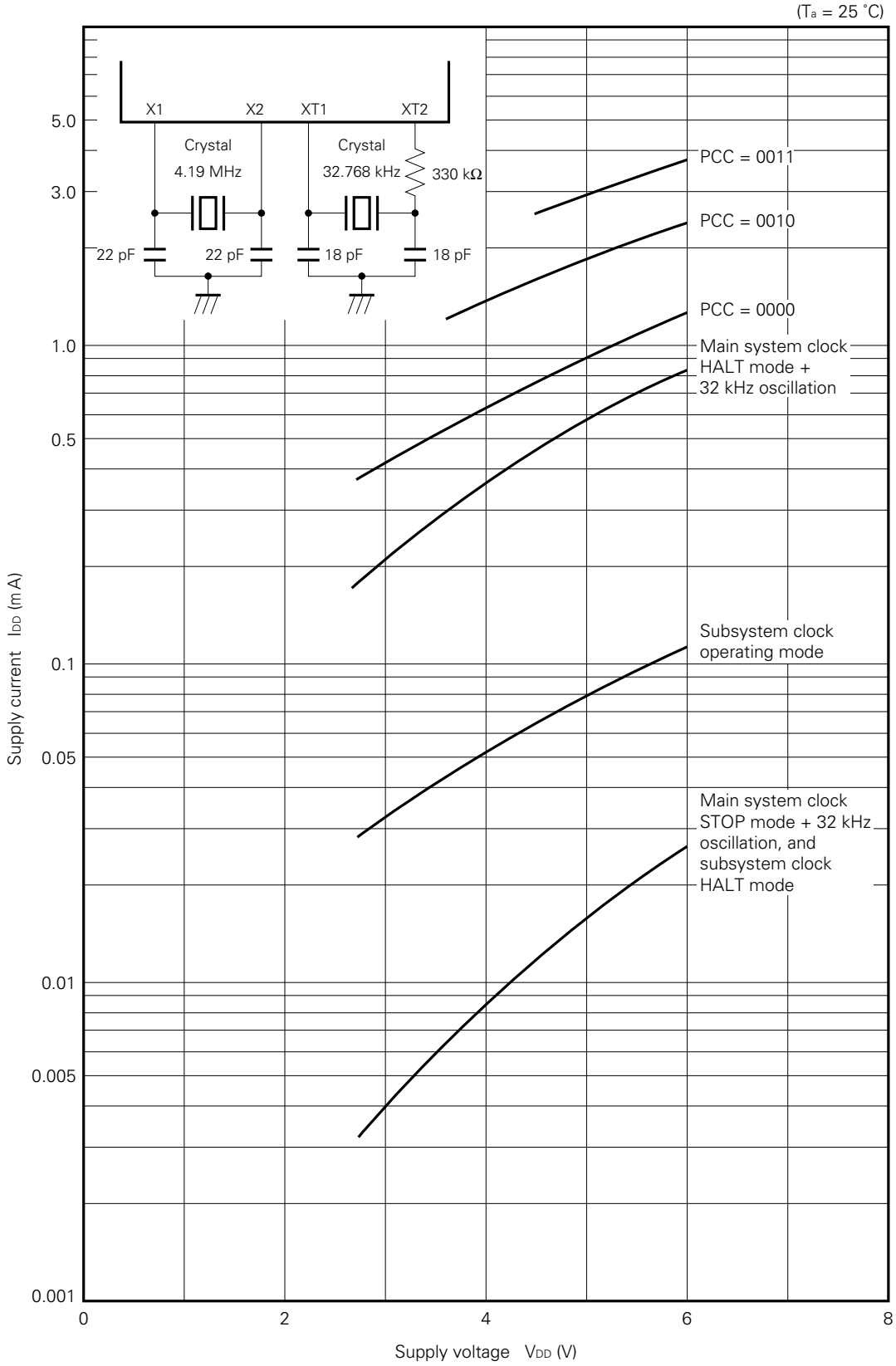


Data Hold Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)

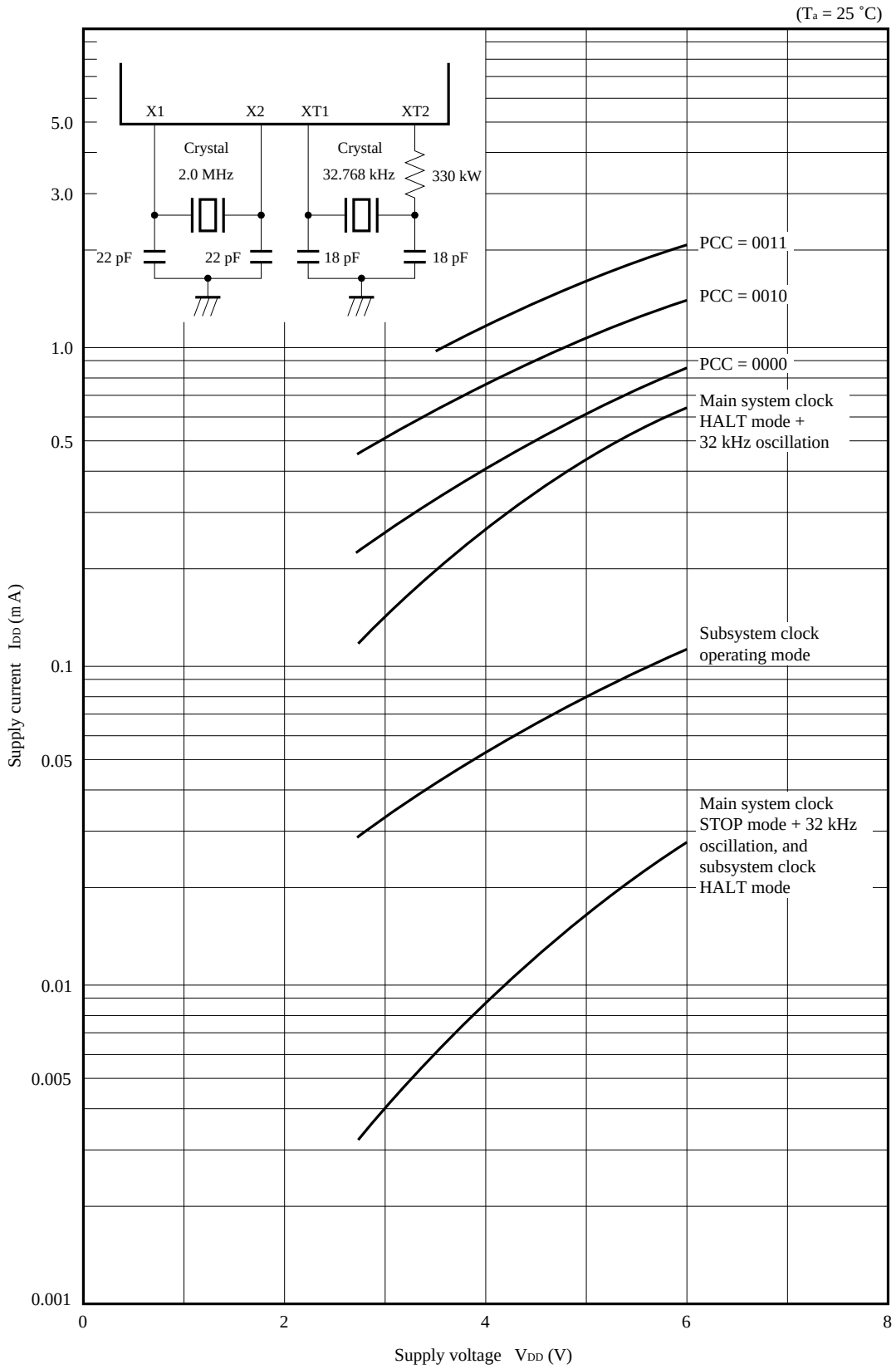


6. CHARACTERISTIC CURVES (FOR REFERENCE) ★

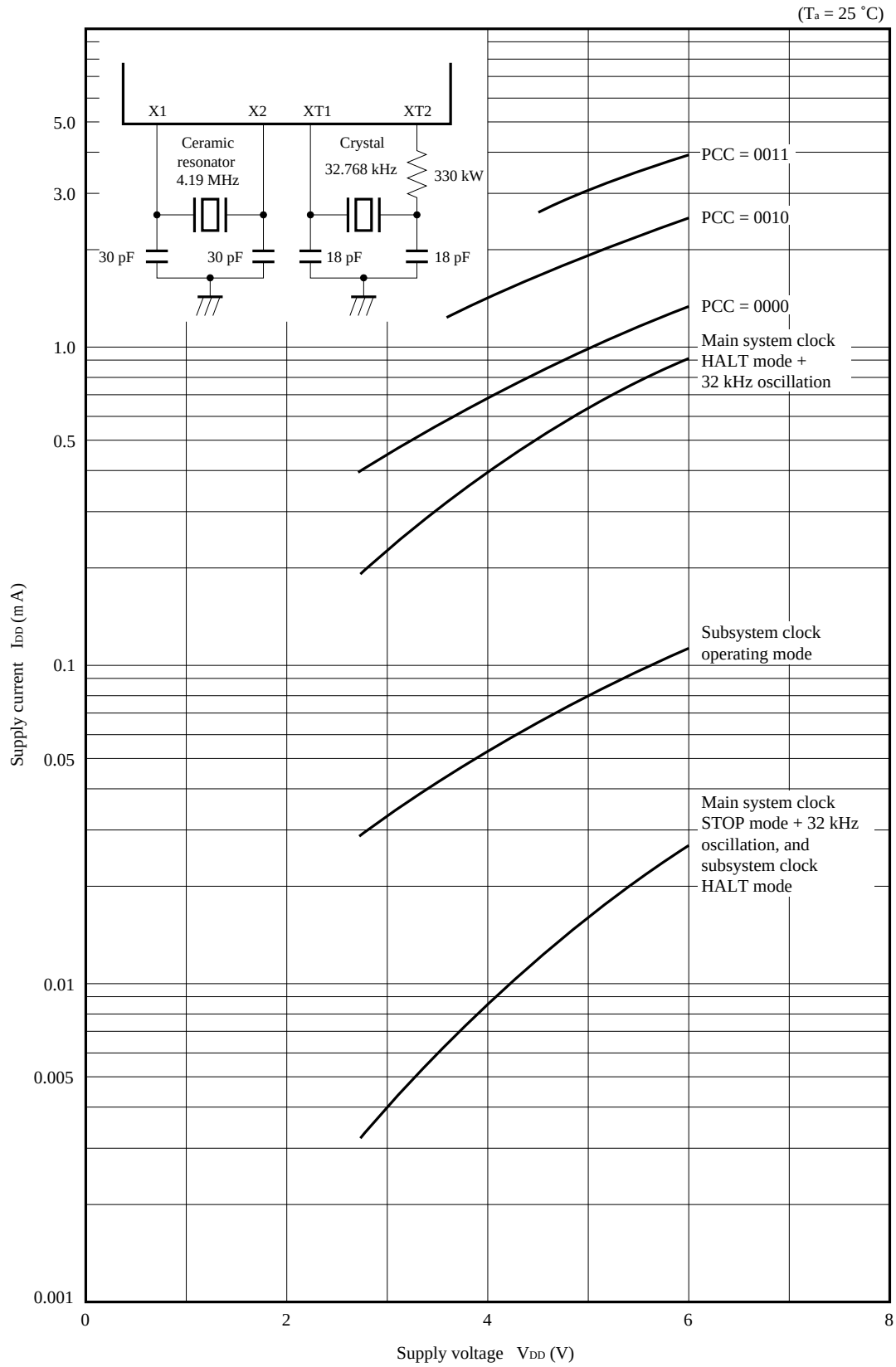
I_{DD} vs V_{DD} (When the main system clock operates at 4.19 MHz with a crystal)



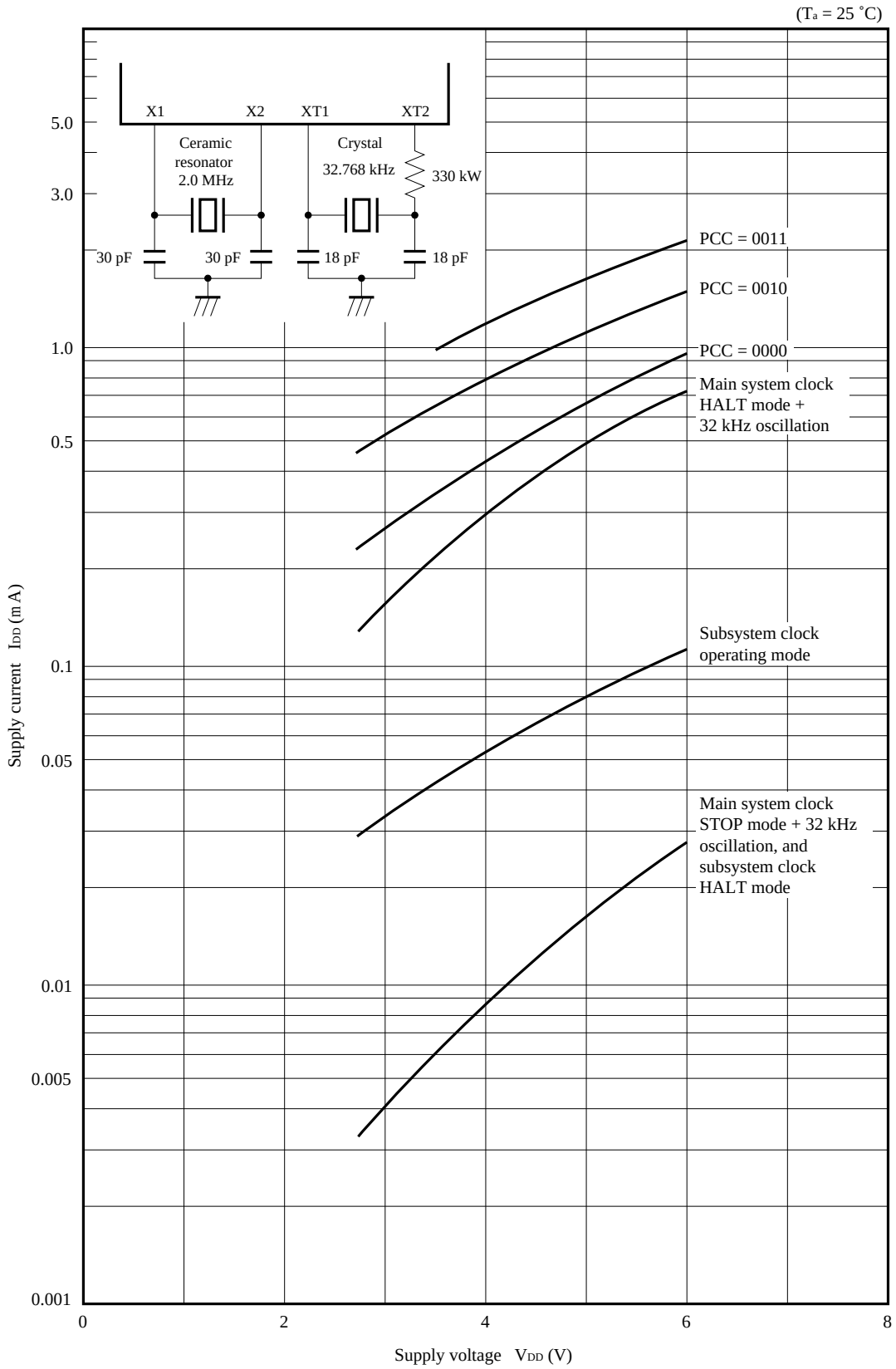
I_{DD} vs V_{DD} (When the main system clock operates at 2.0 MHz with a crystal)



I_{DD} vs V_{DD} (When the main system clock operates at 4.19 MHz with a ceramic resonator)

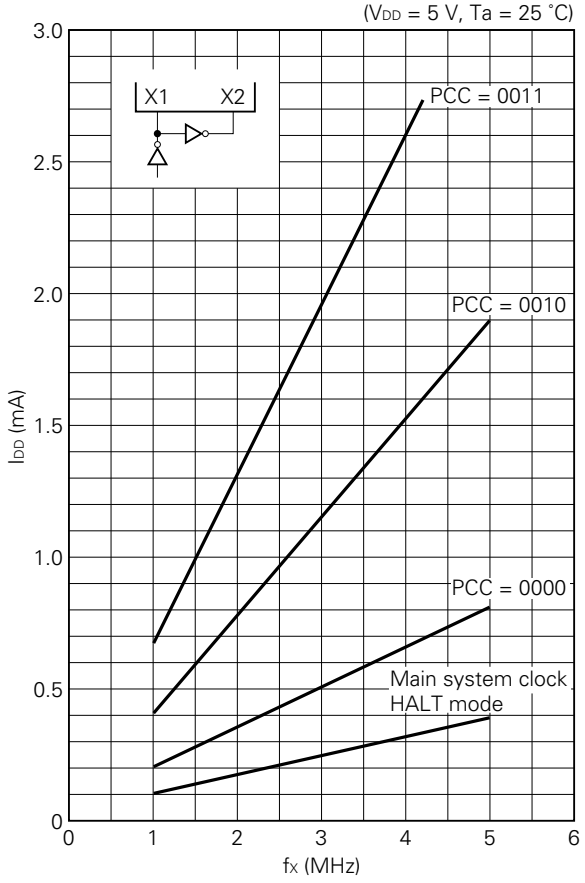


I_{DD} vs V_{DD} (When the main system clock operates at 2.0 MHz with a ceramic resonator)



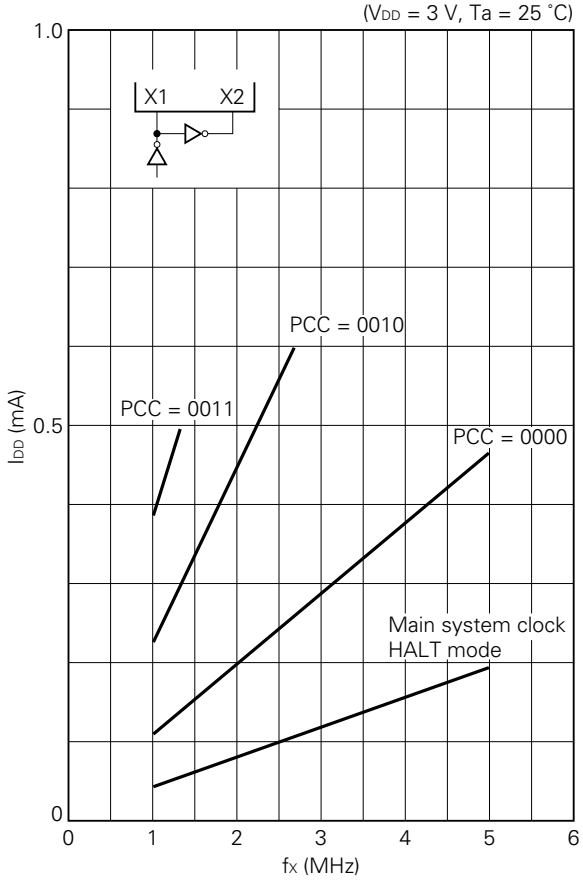
I_{DD} vs f_x

(V_{DD} = 5 V, Ta = 25 °C)



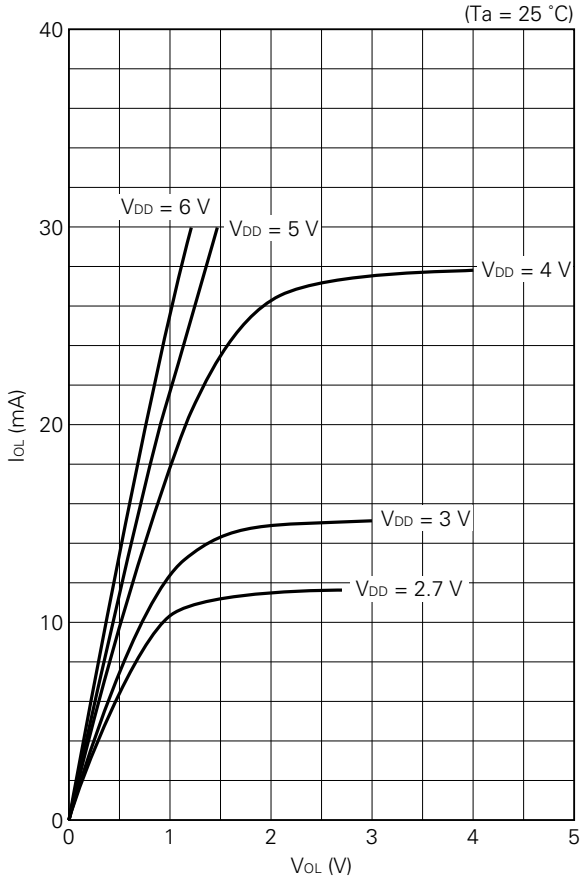
I_{DD} vs f_x

(V_{DD} = 3 V, Ta = 25 °C)



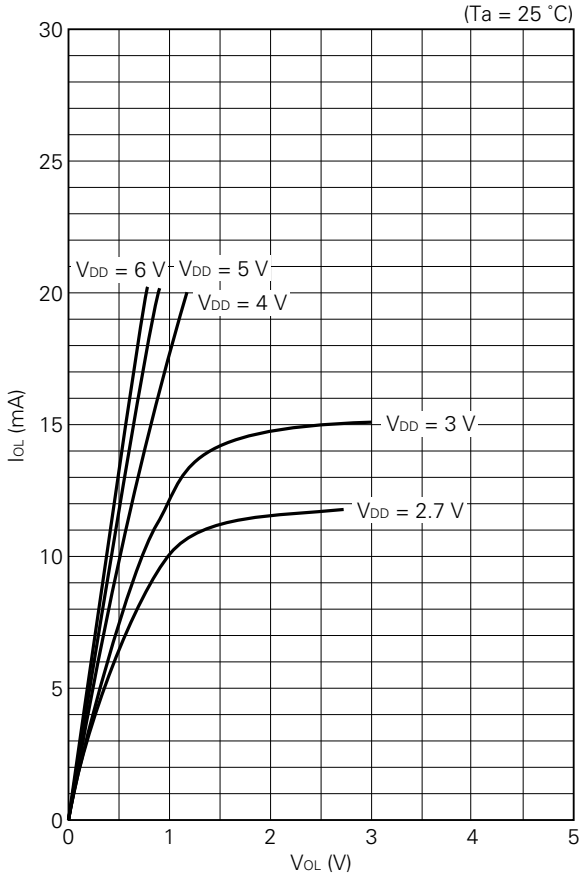
I_{OL} vs V_{OL} (Port 0)

(Ta = 25 °C)

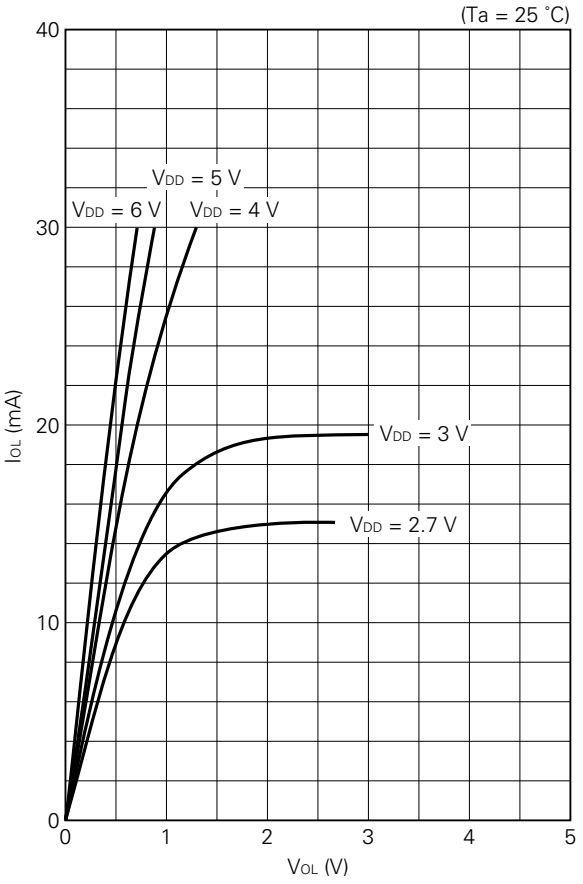


I_{OL} vs V_{OL} (Ports 2 and 6)

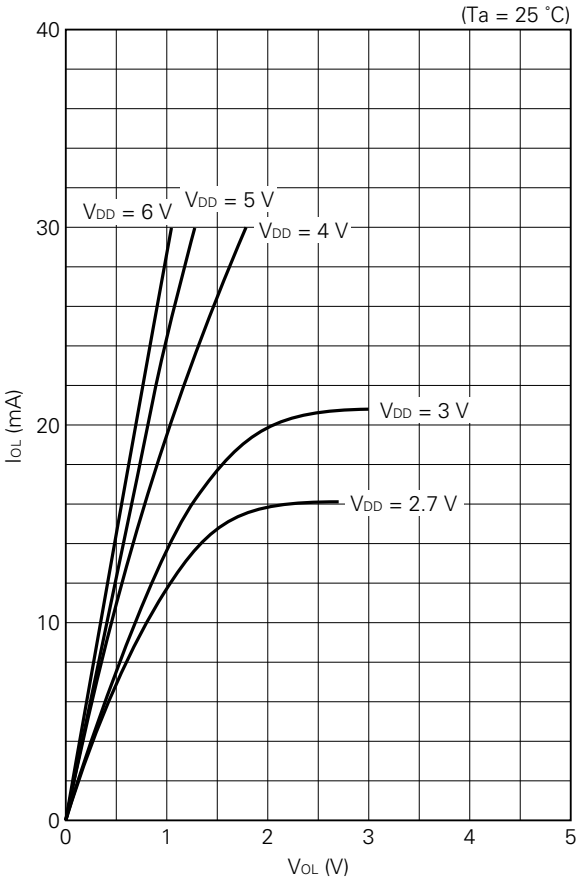
(Ta = 25 °C)



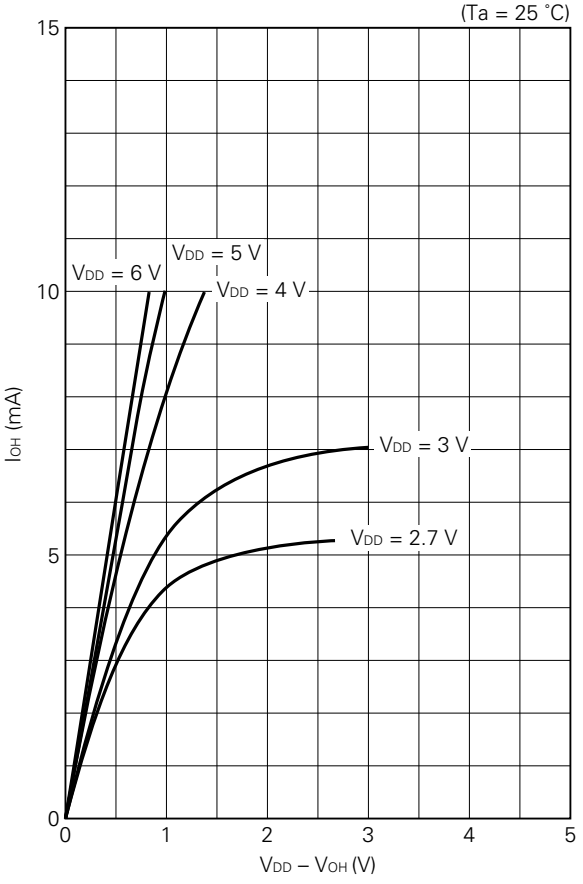
I_{OL} vs V_{OL} (Port 3)



I_{OL} vs V_{OL} (Ports 4 and 5)

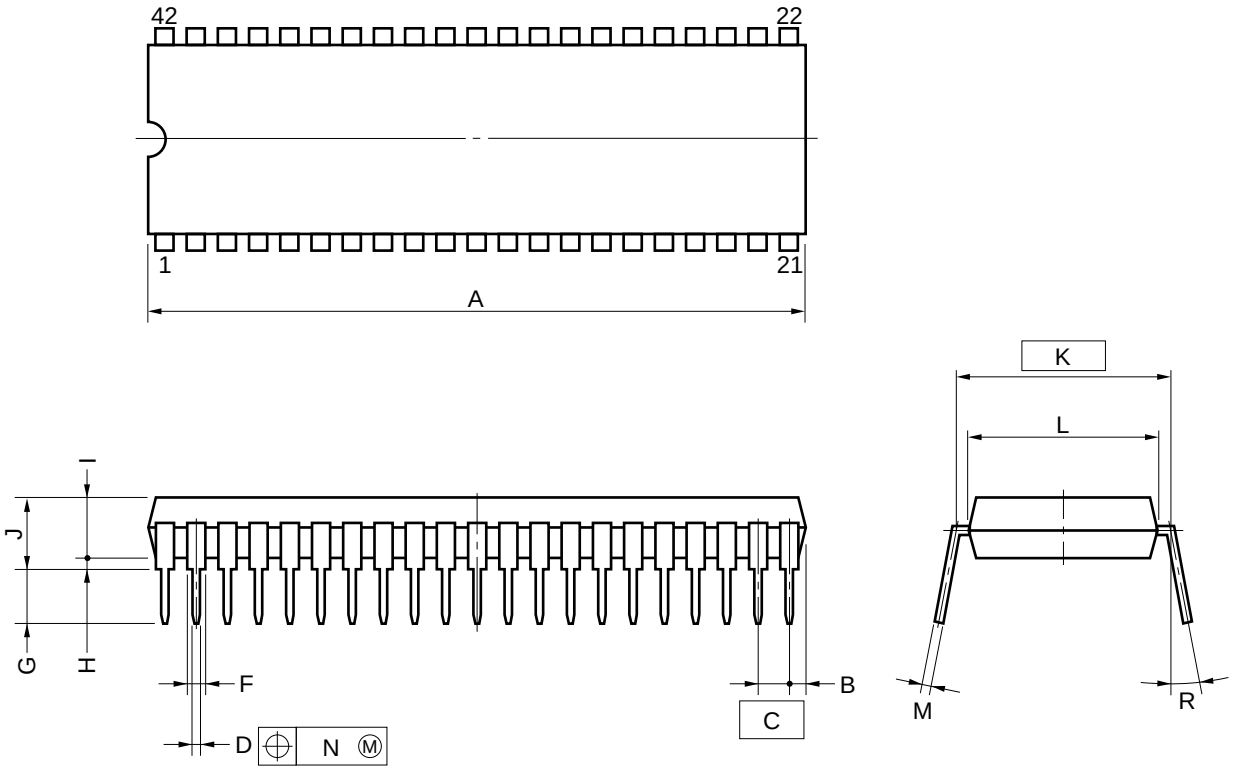


I_{OH} vs V_{OH}



7. PACKAGE DRAWINGS

42PIN PLASTIC SHRINK DIP (600 mil)



NOTES

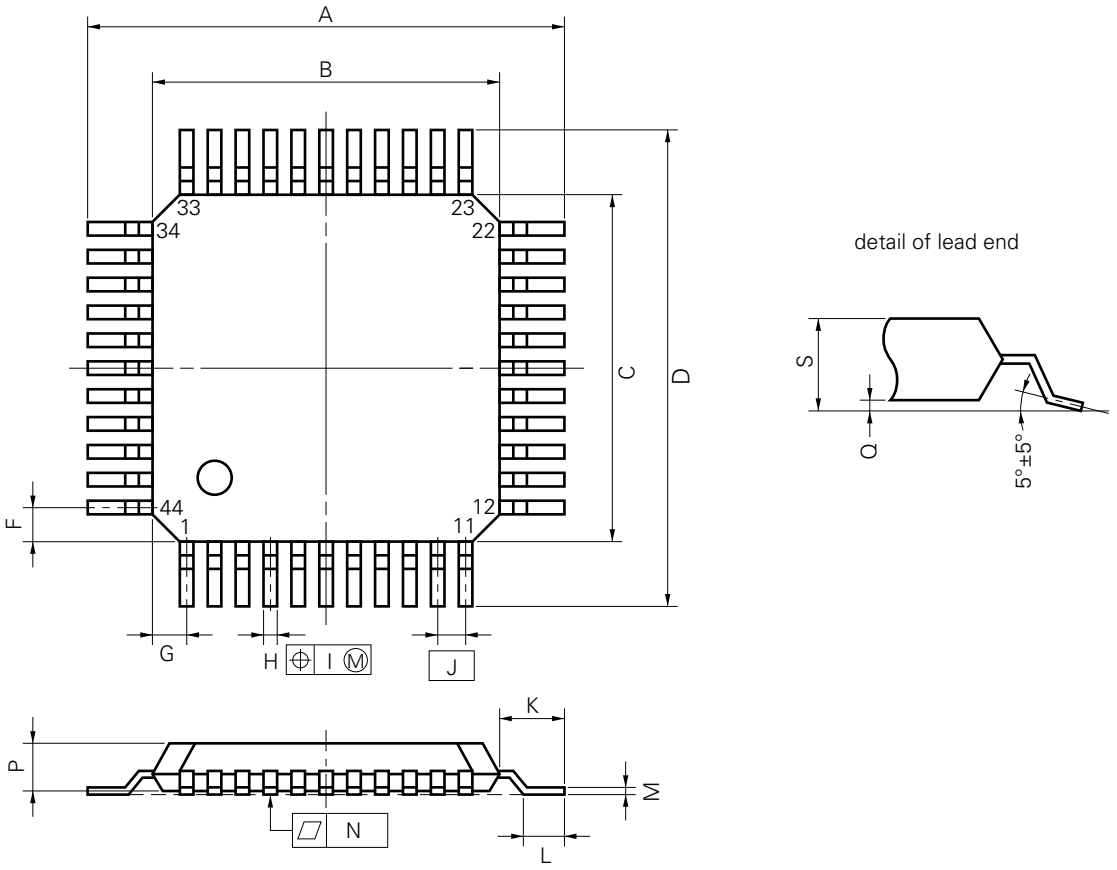
1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	39.13 MAX.	1.541 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2 ± 0.3	0.126 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

P42C-70-600A-1

44 PIN PLASTIC QFP (□10)



P44GB-80-3B4-2

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	13.6±0.4	$0.535^{+0.017}_{-0.016}$
B	10.0±0.2	$0.394^{+0.008}_{-0.009}$
C	10.0±0.2	$0.394^{+0.008}_{-0.009}$
D	13.6±0.4	$0.535^{+0.017}_{-0.016}$
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.12	0.005
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

8. RECOMMENDED SOLDERING CONDITIONS ★

The conditions listed below shall be met when soldering the μPD75P068.

For details of the recommended soldering conditions, refer to our document "SMD Surface Mount Technology Manual" (IEI-1207).

Please consult with our sales offices in case any other soldering process is used, or in case soldering is done under different conditions.

Table 8-1 Soldering Conditions for Surface-Mount Devices

μPD75P068GB-3B4: 44-pin plastic QFP (10 × 10 mm)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 235 °C Reflow time: 30 seconds or less (at 210 °C or more) Maximum allowable number of reflow processes: 2 <Cautions> (1) Do not start reflow-soldering the device if its temperature is higher than the room temperature because of a previous reflow soldering. (2) Do not use water for flux cleaning before a second reflow soldering.	IR35-00-2
VPS	Peak package's surface temperature: 215 °C Reflow time: 40 seconds or less (at 200 °C or more) Maximum allowable number of reflow processes: 2 <Cautions> (1) Do not start reflow-soldering the device if its temperature is higher than the room temperature because of a previous reflow soldering. (2) Do not use water for flux cleaning before a second reflow soldering.	VP15-00-2
Wave soldering	Solder temperature: 260°C or less Flow time: 10 seconds or less Number of flow processes: 1 Preheating temperature: 120 max. (measured on the package surface)	WS60-00-1
Partial heating method	Terminal temperature: 300 °C or less Flow time: 3 seconds or less (for each side of device)	–

Caution Do not apply more than a single process at once, except for "Partial heating method."

Table 8-2 Soldering Conditions for Through Hole Mount Devices

μPD75P068CU: 42-pin plastic shrink DIP (600 mil)

Soldering process	Soldering conditions
Wave soldering (only for leads)	Solder temperature: 260 °C or less Flow time: 10 seconds or less
Partial heating method	Terminal temperature: 260 °C or less Flow time: 10 seconds or less

Caution In wave soldering, apply solder only to the lead section. Care must be taken that jet solder does not come in contact with the main body of the package.

Notice

Other versions of the products are available. For these versions, the recommended reflow soldering conditions have been mitigated as follows:
Higher peak temperature (235 °C), two-stage, and longer exposure limit.
Contact an NEC representative for details.

APPENDIX A DEVELOPMENT TOOLS

The following development tools are provided for developing systems including the μPD75P068:

Hardware	IE-75000-R[Note 1] IE-75001-R	In-circuit emulator for the 75X series
	IE-75000-R-EM[Note 2]	Emulation board for the IE-75000-R and IE-75001-R
	EP-75068CU-R	Emulation probe for the μPD75P068CU
	EP-75068GB-R EV-9200G-44	Emulation probe for the μPD75P068GB. A 44-pin conversion socket, the EV-9200G-64, is attached to the probe.
	PG-1500	PROM programmer
	PA-75P008CU	PROM programmer adapter for the μPD75P068CU/GB. Connected to the PG-1500.
Software	IE control program	Host machine • PC-9800 series (MS-DOS™ Ver. 3.30 to Ver. 5.00A[Note 3]) • PC/AT™ series (PC DOS™ Ver. 3.10)
	PG-1500 controller	
	RA75X relocatable assembler	

Notes 1. Maintenance service only

2. Not contained in the IE-75001-R

3. MS-DOS versions 5.00 and 5.00A are provided with a task swap function. This function, however, cannot be used in these software.

Remark Refer to *75X Series Selection Guide* (IF-1027) for development tools manufactured by third parties.

APPENDIX B RELATED DOCUMENTS

Documents related to the device

Document Name	Document No.
User's Manual	IEU-1366
Application Note (Preliminary)	IEA-1296
75X Series Selection Guide	IF-1027

Documents related to development tools

	Document Name		Document No.
Hardware	IE-75000-R/IE-75001-R User's Manual		EEU-1455
	IE-75000-R-EM User's Manual		EEU-1294
	EP-75068CU-R User's Manual		EEU-1317
	EP-75068GB-R User's Manual		EEU-1428
	PG-1500 User's Manual		EEU-1335
Software	RA75X Assembler Package User's Manual	Operation	EEU-1346
		Language	EEU-1363
	PG-1500 Controller User's Manual		EEU-1291

Other documents

Document Name	Document No.
Package Manual	IEI-1213
SMD Surface Mount Technology Manual	IEI-1207
Quality Grades on NEC Semiconductor Devices	IEI-1209
NEC Semiconductor Device Reliability/Quality Control System	IEI-1203
Electrostatic Discharge (ESD) Test	IEI-1201
Guide to Quality Assurance for Semiconductor Devices	MEI-1202

Caution The above documents may be revised without notice. Use the latest versions when you design an application system.

[MEMO]

Cautions on CMOS Devices

① **Countermeasures against static electricity for all MOSs**

Caution When handling MOS devices, take care so that they are not electrostatically charged.

Strong static electricity may cause dielectric breakdown in gates. When transporting or storing MOS devices, use conductive trays, magazine cases, shock absorbers, or metal cases that NEC uses for packaging and shipping. Be sure to ground MOS devices during assembling. Do not allow MOS devices to stand on plastic plates or do not touch pins. Also handle boards on which MOS devices are mounted in the same way.

② **CMOS-specific handling of unused input pins**

Caution Hold CMOS devices at a fixed input level.

Unlike bipolar or NMOS devices, if a CMOS device is operated with no input, an intermediate-level input may be caused by noise. This allows current to flow in the CMOS device, resulting in a malfunction. Use a pull-up or pull-down resistor to hold a fixed input level. Since unused pins may function as output pins at unexpected times, each unused pin should be separately connected to the V_{DD} or GND pin through a resistor.

If handling of unused pins is documented, follow the instructions in the document.

③ **Statuses of all MOS devices at initialization**

Caution The initial status of a MOS device is unpredictable when power is turned on.

Since characteristics of a MOS device are determined by the amount of ions implanted in molecules, the initial status cannot be determined in the manufacture process. NEC has no responsibility for the output statuses of pins, input and output settings, and the contents of registers at power on. However, NEC assures operation after reset and items for mode setting if they are defined.

When you turn on a device having a reset function, be sure to reset the device first.

[MEMO]

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