

## 8-BIT SINGLE-CHIP MICROCONTROLLER

## DESCRIPTION

The  $\mu$ PD78F0034Y is a product of the  $\mu$ PD780034Y Subseries in the 78K/0 Series and equivalent to the  $\mu$ PD780034Y with a flash memory in place of internal ROM.

The  $\mu$ PD78F0034Y incorporates a flash memory, which can be programmed and erased without being removed from the substrate.

Functions are described in detail in the following user's manuals. Be sure to read them before designing.

$\mu$ PD780024, 780024Y, 780034, 780034Y Subseries User's Manual : U12022E  
78K/0 Series User's Manual — Instructions : U12326E

## FEATURES

- I<sup>2</sup>C bus serial interface supporting multimaster
- Pin-compatible with mask ROM versions (except V<sub>PP</sub> pin)
- Flash memory : 32 Kbytes
- Internal high-speed RAM : 1024 bytes<sup>Note</sup>
- ★ • Power supply voltage : V<sub>DD</sub> = 2.7 to 5.5 V

**Note** The flash memory and internal high-speed RAM capacities can be changed with the memory size switching register (IMS).

**Remark** For the differences between the flash memory versions and the mask ROM versions, refer to 1.  
**DIFFERENCES BETWEEN  $\mu$ PD78F0034Y AND MASK ROM VERSIONS.**

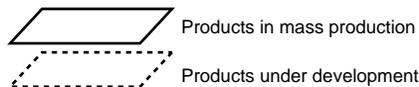
## ORDERING INFORMATION

Part Number	Package	Internal ROM
$\mu$ PD78F0034YCW	64-pin plastic shrink DIP (750 mils)	Flash memory
$\mu$ PD78F0034YGC-AB8	64-pin plastic QFP (14 × 14 mm)	Flash memory
$\mu$ PD78F0034YGK-8A8	64-pin plastic LQFP (12 × 12 mm)	Flash memory

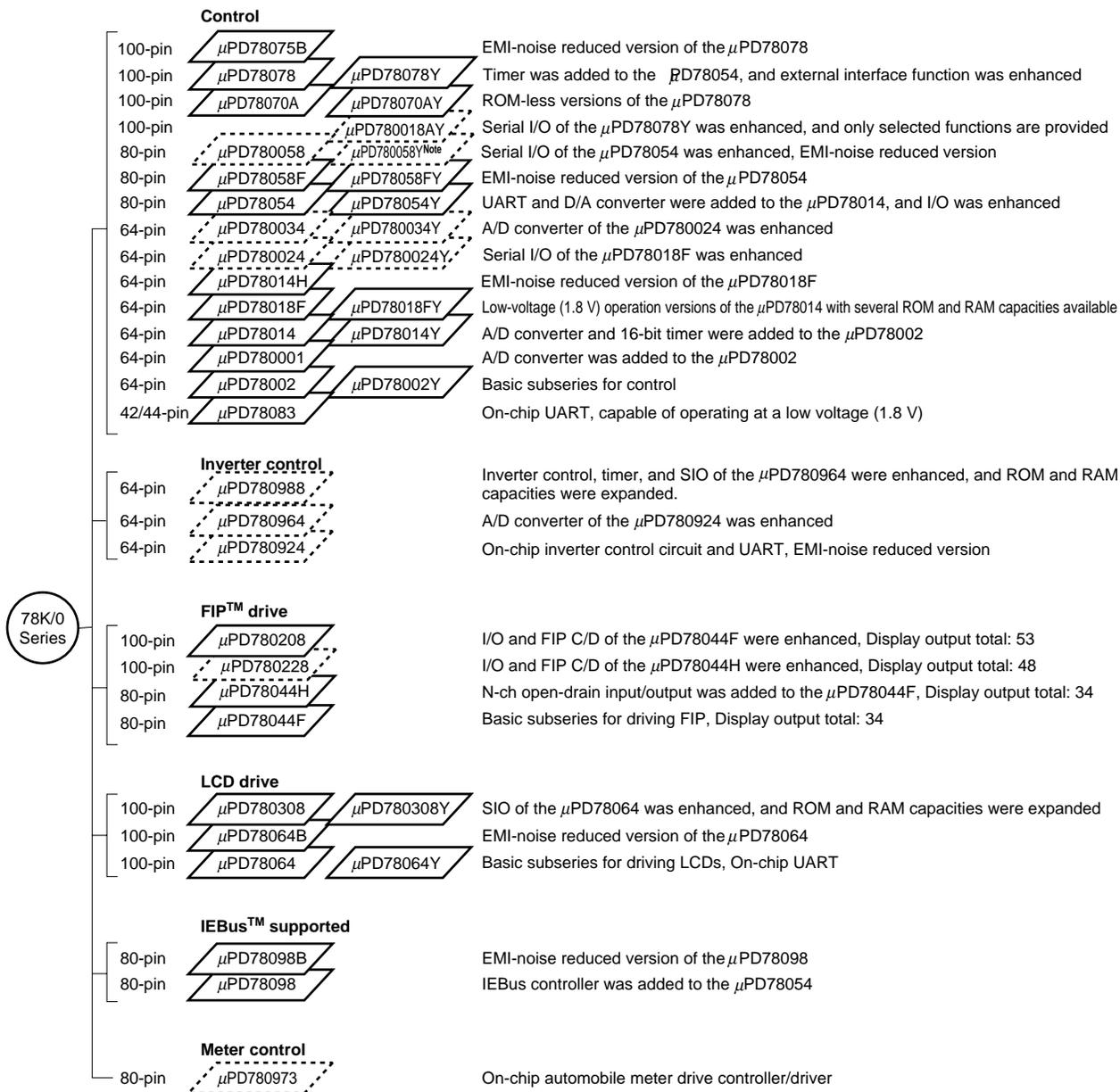
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★ 78K/0 SERIES DEVELOPMENT

The products in the 78K/0 Series are listed below. The names enclosed in boxes are subseries names.



Y subseries products are compatible with I<sup>2</sup>C bus.



**Note** Under planning

The major functional differences among the Y subseries are shown below.

Function		ROM Capacity	Configuration of Serial Interface	I/O	V <sub>DD</sub> MIN. Value
Subseries Name					
Control	μPD78078Y	48 K to 60 K	3-wire/2-wire/I <sup>2</sup> C : 1 ch 3-wire with automatic transmit/receive function : 1 ch	88	1.8 V
	μPD78070AY	–	3-wire/UART : 1 ch	61	2.7 V
	μPD780018AY	48 K to 60 K	3-wire with automatic transmit/receive function : 1 ch Time-division 3-wire : 1 ch I <sup>2</sup> C bus (multimaster supported) : 1 ch	88	
	μPD780058Y	24 K to 60 K	3-wire/2-wire/I <sup>2</sup> C : 1 ch 3-wire with automatic transmit/receive function : 1 ch 3-wire/time-division UART : 1 ch	68	1.8 V
	μPD78058FY	48 K to 60 K	3-wire/2-wire/I <sup>2</sup> C : 1 ch 3-wire with automatic transmit/receive function : 1 ch	69	2.7 V
	μPD78054Y	16 K to 60 K	3-wire/UART : 1 ch		2.0 V
	μPD780034Y	8 K to 32 K	UART : 1 ch 3-wire : 1 ch	51	1.8 V
	μPD780024Y		I <sup>2</sup> C bus (multimaster supported) : 1 ch		
	μPD78018FY	8 K to 60 K	3-wire/2-wire/I <sup>2</sup> C : 1 ch 3-wire with automatic transmit/receive function : 1 ch	53	
	μPD78014Y	8 K to 32 K	3-wire/2-wire/SBI/I <sup>2</sup> C : 1 ch 3-wire with automatic transmit/receive function : 1 ch		2.7 V
μPD78002Y	8 K to 16 K	3-wire/2-wire/SBI/I <sup>2</sup> C : 1 ch			
LCD drive	μPD780308Y	48 K to 60 K	3-wire/2-wire/I <sup>2</sup> C : 1 ch 3-wire/time-division UART : 1 ch 3-wire : 1 ch	57	2.0 V
	μPD78064Y	16 K to 32 K	3-wire/2-wire/I <sup>2</sup> C : 1 ch 3-wire/UART : 1 ch		

**Remark** The functions other than the serial interface are common to the subseries without Y.

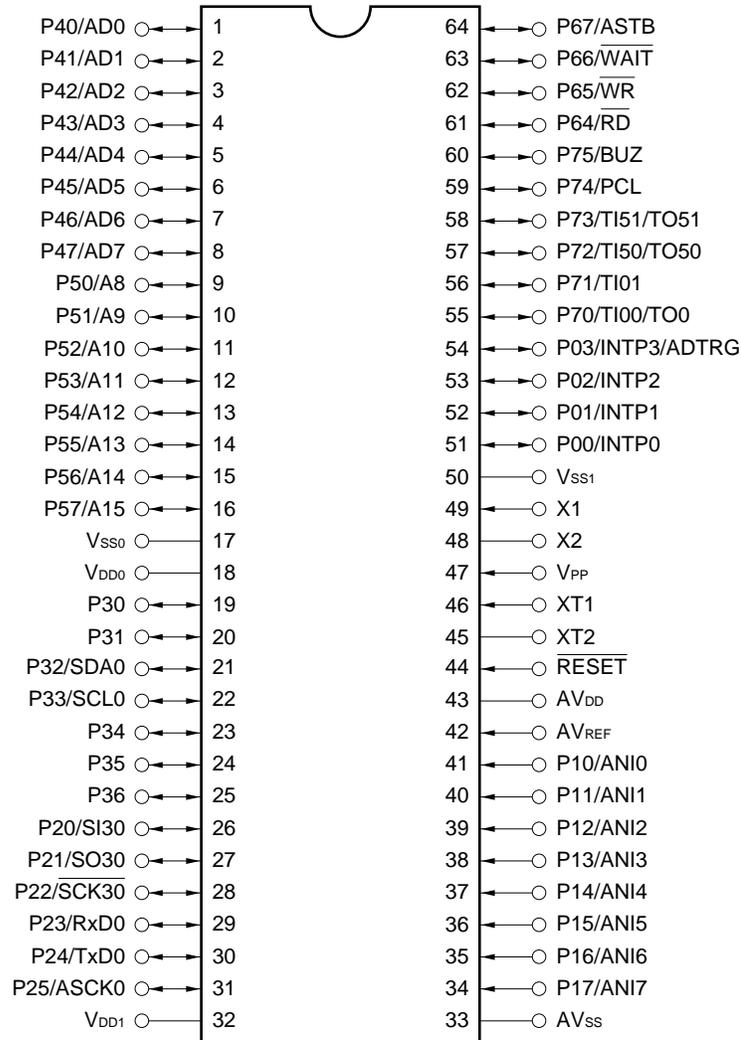
OVERVIEW OF FUNCTION

Item		Function
Internal memory	Flash memory	32 Kbytes <sup>Note</sup>
	High-speed RAM	1024 bytes <sup>Note</sup>
Memory space		64 Kbytes
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Minimum instruction execution time		On-chip minimum instruction execution time cycle modification function
	When main system clock selected	0.24 μs/0.48 μs/0.95 μs/1.91 μs/3.81 μs (at 8.38-MHz operation)
	When subsystem clock selected	122 μs (at 32.768-kHz operation)
Instruction set		<ul style="list-style-type: none"> <li>• 16-bit operate • multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits)</li> <li>• Bit manipulate (set, reset, test, Boolean operation)</li> <li>• BCD adjust, etc.</li> </ul>
I/O ports		Total : 51 <ul style="list-style-type: none"> <li>• CMOS input : 8</li> <li>• CMOS I/O : 39</li> <li>• N-ch open-drain I/O (5-V withstand voltage) : 4</li> </ul>
A/D converter		• 10-bit resolution × 8 channels
Serial interface		<ul style="list-style-type: none"> <li>• 3-wire serial I/O mode : 1 channel</li> <li>• UART mode : 1 channel</li> <li>• I<sup>2</sup>C bus mode (multimaster supported) : 1 channel</li> </ul>
Timer		<ul style="list-style-type: none"> <li>• 16-bit timer/event counter : 1 channel</li> <li>• 8-bit timer/event counter : 2 channels</li> <li>• Watch timer : 1 channel</li> <li>• Watchdog timer : 1 channel</li> </ul>
Timer output		3 (8-bit PWM output capable: 2)
Clock output		131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.10 MHz, 4.19 MHz, 8.38 MHz (at 8.38-MHz operation with main system clock) 32.768 kHz (at 32.768-kHz operation with subsystem clock)
Buzzer output		1.02 kHz, 2.05 kHz, 4.10 kHz, 8.19 kHz (at 8.38-MHz operation with main system clock)
★ Vectored interrupt source	Maskable	Internal : 13, External : 5
	Non-maskable	Internal : 1
	Software	1
Test input		Internal : 1, External : 1
★ Power supply voltage		V <sub>DD</sub> = 2.7 to 5.5 V
Operating ambient temperature		T <sub>A</sub> = -40 to +85°C
Package		<ul style="list-style-type: none"> <li>• 64-pin plastic shrink DIP (750 mils)</li> <li>• 64-pin plastic QFP (14 × 14 mm)</li> <li>• 64-pin plastic LQFP (12 × 12 mm)</li> </ul>

**Note** The capacities of the flash memory and the internal high-speed RAM can be changed with the memory size switching register (IMS).

**PIN CONFIGURATION (TOP VIEW)**

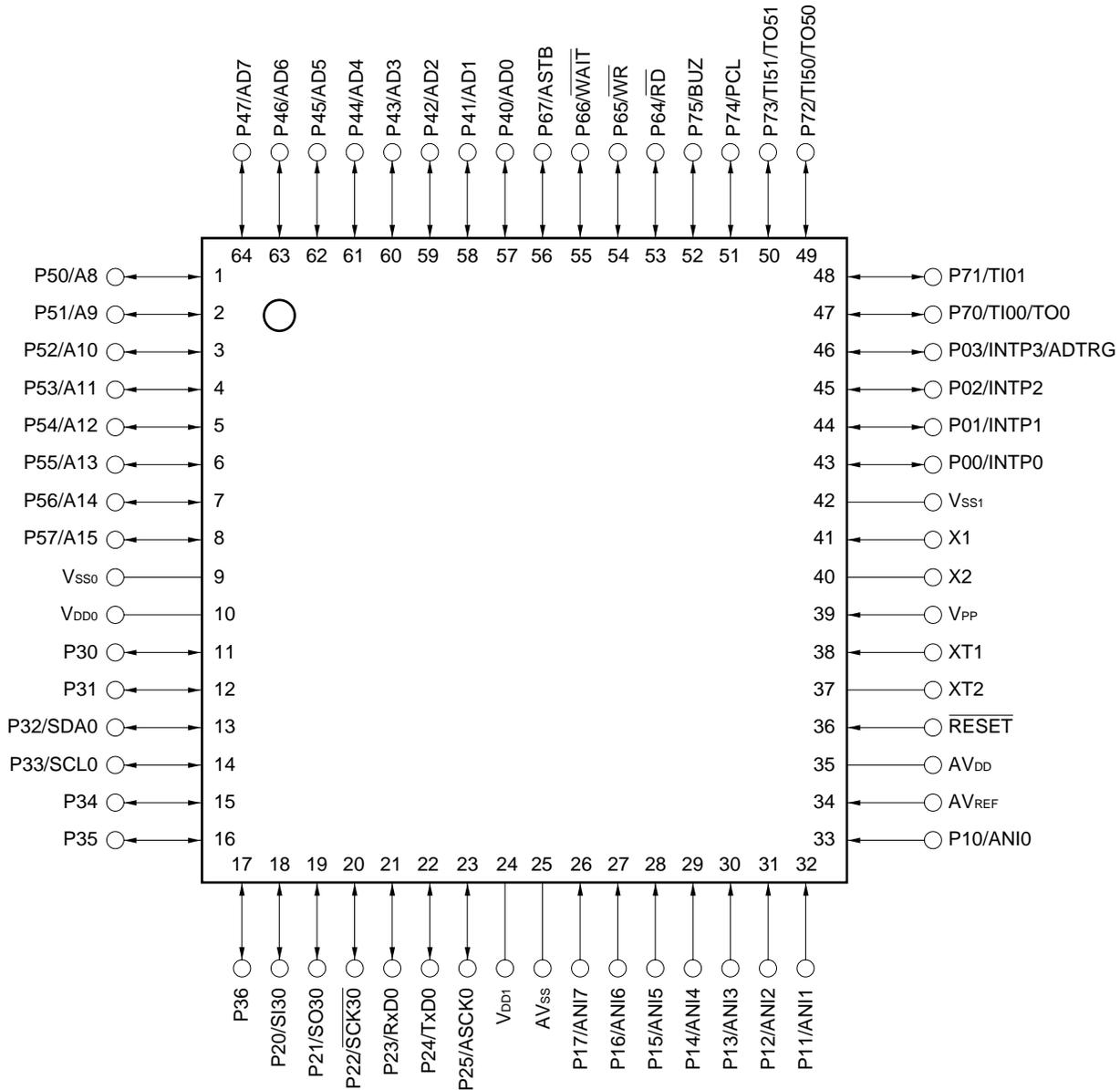
- 64-pin Plastic Shrink DIP (750 mils)  
μPD78F0034YCW



- ★ **Cautions**
  1. Connect the V<sub>PP</sub> pin directly to V<sub>SS0</sub> or V<sub>SS1</sub> in normal operation mode.
  2. Connect the AV<sub>SS</sub> pin to V<sub>SS0</sub>.

**Remark** When the μPD78F0034Y is used in application fields that require reduction of the noise generated from inside the microcontroller, the implementation of noise reduction measures, such as supplying voltage to V<sub>DD0</sub> and V<sub>DD1</sub> independently and connecting V<sub>SS0</sub> and V<sub>SS1</sub> to different ground lines, is recommended.

- 64-pin Plastic QFP (14 × 14 mm)  
μPD78F0034YGC-AB8
- 64-pin Plastic LQFP (12 × 12 mm)  
μPD78F0034YGK-8A8

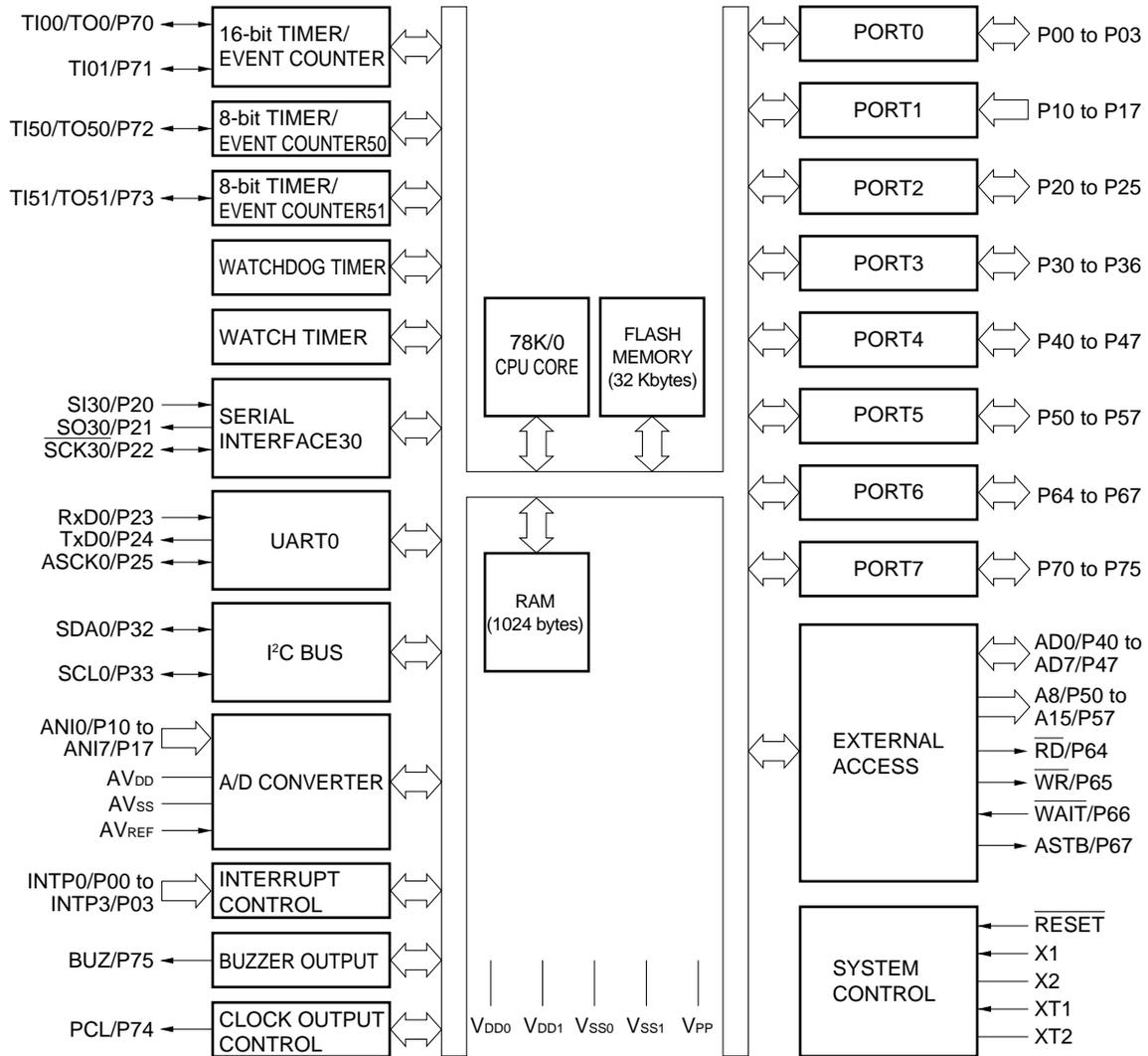


- ★ **Cautions**
  1. Connect the V<sub>PP</sub> pin directly to V<sub>SS0</sub> or V<sub>SS1</sub> in normal operation mode.
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A8 to A15	: Address Bus	PCL	: Programmable Clock
AD0 to AD7	: Address/Data Bus	$\overline{RD}$	: Read Strobe
ADTRG	: AD Trigger Input	$\overline{RESET}$	: Reset
ANI0 to ANI7	: Analog Input	RxD0	: Receive Data
ASCK0	: Asynchronous Serial Clock	$\overline{SCK30}$	: Serial Clock
ASTB	: Address Strobe	SCL0	: Serial Clock
AV <sub>DD</sub>	: Analog Power Supply	SDA0	: Serial Data
AV <sub>REF</sub>	: Analog Reference Voltage	SI30	: Serial Input
AV <sub>SS</sub>	: Analog Ground	SO30	: Serial Output
BUZ	: Buzzer Clock	TI00, TI01, TI50, TI51	: Timer Input
INTP0 to INTP3	: Interrupt from Peripherals	TO0, TO50, TO51	: Timer Output
P00 to P03	: Port 0	TxD0	: Transmit Data
P10 to P17	: Port 1	V <sub>DD0</sub> , V <sub>DD1</sub>	: Power Supply
P20 to P25	: Port 2	V <sub>PP</sub>	: Programming Power Supply
P30 to P36	: Port 3	V <sub>SS0</sub> , V <sub>SS1</sub>	: Ground
P40 to P47	: Port 4	$\overline{WAIT}$	: Wait
P50 to P57	: Port 5	$\overline{WR}$	: Write Strobe
P64 to P67	: Port 6	X1, X2	: Crystal (Main System Clock)
P70 to P75	: Port 7	XT1, XT2	: Crystal (Subsystem Clock)

BLOCK DIAGRAM



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1. DIFFERENCES BETWEEN μPD78F0034Y AND MASK ROM VERSIONS

The μPD78F0034Y is a product provided with a flash memory that enables on-board writing, erasing, and rewriting of programs with the device mounted on the target system.

The functions of the μPD78F0034Y (except the functions specified for flash memory) can be made the same as those of the mask ROM versions by setting the memory size switching register (IMS).

Table 1-1 shows the differences between the flash memory version (μPD78F0034Y) and the mask ROM versions (μPD780031Y, 780032Y, 780033Y, and 780034Y).

Table 1-1. Differences between μPD78F0034Y and Mask ROM Versions

Item	μPD78F0034	Mask ROM Versions
Internal ROM type	Flash memory	Mask ROM
Internal ROM capacity	32 Kbytes	μPD780031Y : 8 Kbytes μPD780032Y : 16 Kbytes μPD780033Y : 24 Kbytes μPD780034Y : 32 Kbytes
Internal high-speed RAM capacity	1024 bytes	μPD780031Y : 512 bytes μPD780032Y : 512 bytes μPD780033Y : 1024 bytes μPD780034Y : 1024 bytes
Internal ROM and internal high-speed RAM capacity changeable/not changeable with memory size switching register (IMS)	Changeable <sup>Note</sup>	Not changeable
IC pin	Not provided	Provided
V <sub>PP</sub> pin	Provided	Not provided
★ Power supply voltage	V <sub>DD</sub> = 2.7 to 5.5 V	V <sub>DD</sub> = 1.8 to 5.5 V
Electrical specifications, recommended soldering conditions	Refer to the data sheet of individual products.	

**Note** Flash memory is set to 32 Kbytes and internal high-speed RAM is set to 1024 bytes by  $\overline{\text{RESET}}$  input.

★ **Caution** There are differences in noise immunity and noise radiation between the flash memory versions and mask ROM versions. When pre-producing an application set with the flash memory version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluation for commercial samples (not engineering samples) of the mask ROM version.

2. PIN FUNCTIONS

2.1 Port Pins (1/2)

Pin Name	I/O	Function		After Reset	Alternate Function
P00	I/O	Port 0 4-bit input/output port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be used by software.		Input	INTP0
P01					INTP1
P02					INTP2
P03					INTP3/ADTRG
P10 to P17	Input	Port 1 8-bit input only port.		Input	ANI0 to ANI7
P20	I/O	Port 2 6-bit input/output port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be used by software.		Input	SI30
P21					SO30
P22					SCK30
P23					RxD0
P24					TxD0
P25					ASCK0
P30	I/O	Port 3 7-bit input/output port. Input/output can be specified bit-wise.	N-ch open-drain input/output port. LEDs can be driven directly.	Input	—
P31					SDA0
P32					
P33			When used as an input port, an on-chip pull-up resistor can be used by software.		—
P34					
P35					
P36					
P40 to P47	I/O	Port 4 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be used by software. Test input flag (KRIF) is set to 1 by the falling-edge detection.		Input	AD0 to AD7
P50 to P57	I/O	Port 5 8-bit input/output port. LEDs can be driven directly. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be used by software.		Input	A8 to A15
P64	I/O	Port 6 4-bit input/output port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be used by software.		Input	RD
P65					WR
P66					WAIT
P67					ASTB

2.1 Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
P70	I/O	Port 7 6-bit input/output port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be used by software.	Input	T100/TO0
P71				T101
P72				T150/TO50
P73				T151/TO51
P74				PCL
P75				BUZ

2.2 Non-Port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt request input for which the effective edge (rising edge, falling edge, or both rising edge and falling edge) can be specified.	Input	P00
INTP1				P01
INTP2				P02
INTP3				P03/ADTRG
SI30	Input	Serial interface serial data input.	Input	P20
SO30	Output	Serial interface serial data output.	Input	P21
SDA0	I/O	Serial interface serial data input/output.	Input	P32
SCK30	I/O	Serial interface serial clock input/output.	Input	P22
SCL0				P33
RxD0	Input	Serial data input for asynchronous serial interface.	Input	P23
TxD0	Output	Serial data output for asynchronous serial interface.	Input	P24
ASCK0	Input	Serial clock input for asynchronous serial interface.	Input	P25
★ T100	Input	External count clock input to 16-bit timer (TM0). Capture trigger signal input to TM0 capture register (CR01).	Input	P70/TO0
★ T101		Capture trigger signal input to TM0 capture register (CR00).		P71
T150		External count clock input to 8-bit timer (TM50).		P72/TO50
T151		External count clock input to 8-bit timer (TM51).		P73/TO51
TO0	Output	16-bit timer (TM0) output.	Input	P70/T100
TO50		8-bit timer (TM50) output (alternate function is 8-bit PWM output).	Input	P72/T150
TO51		8-bit timer (TM51) output (alternate function is 8-bit PWM output).		P73/T151
PCL	Output	Clock output (for trimming of main system clock and subsystem clock).	Input	P74
BUZ	Output	Buzzer output.	Input	P75
AD0 to AD7	I/O	Lower address/data bus for extending memory externally.	Input	P40 to P47
A8 to A15	Output	Higher address bus for extending memory externally.	Input	P50 to P57
RD	Output	Strobe signal output for read operation of external memory.	Input	P64
WR		Strobe signal output for write operation of external memory.		P65
WAIT	Input	Inserting wait for accessing external memory.	Input	P66
ASTB	Output	Strobe output that externally latches address information output to port 4 and port 5 to access external memory.	Input	P67

2.2 Non-Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
ANI0 to ANI7	Input	A/D converter analog input.	Input	P10 to P17
ADTRG	Input	A/D converter trigger signal input.	Input	P03/INTP3
AVREF	Input	A/D converter reference voltage input.	—	—
AVDD	—	A/D converter analog power supply. Set the voltage equal to VDD0 or VDD1.	—	—
AVSS	—	A/D converter ground potential. Set the voltage equal to VSS0 or VSS1.	—	—
RESET	Input	System reset input.	—	—
X1	Input	Connecting crystal resonator for main system clock oscillation.	—	—
X2	—		—	—
XT1	Input	Connecting crystal resonator for subsystem clock oscillation.	—	—
XT2	—		—	—
VDD0	—	Positive power supply for ports.	—	—
VSS0	—	Ground potential of ports.	—	—
VDD1	—	Positive power supply (except ports).	—	—
VSS1	—	Ground potential (except ports).	—	—
VPP	—	Applying high voltage for program write/verify. Connect directly to VSS0 or VSS1 in normal operation mode.	—	—

★

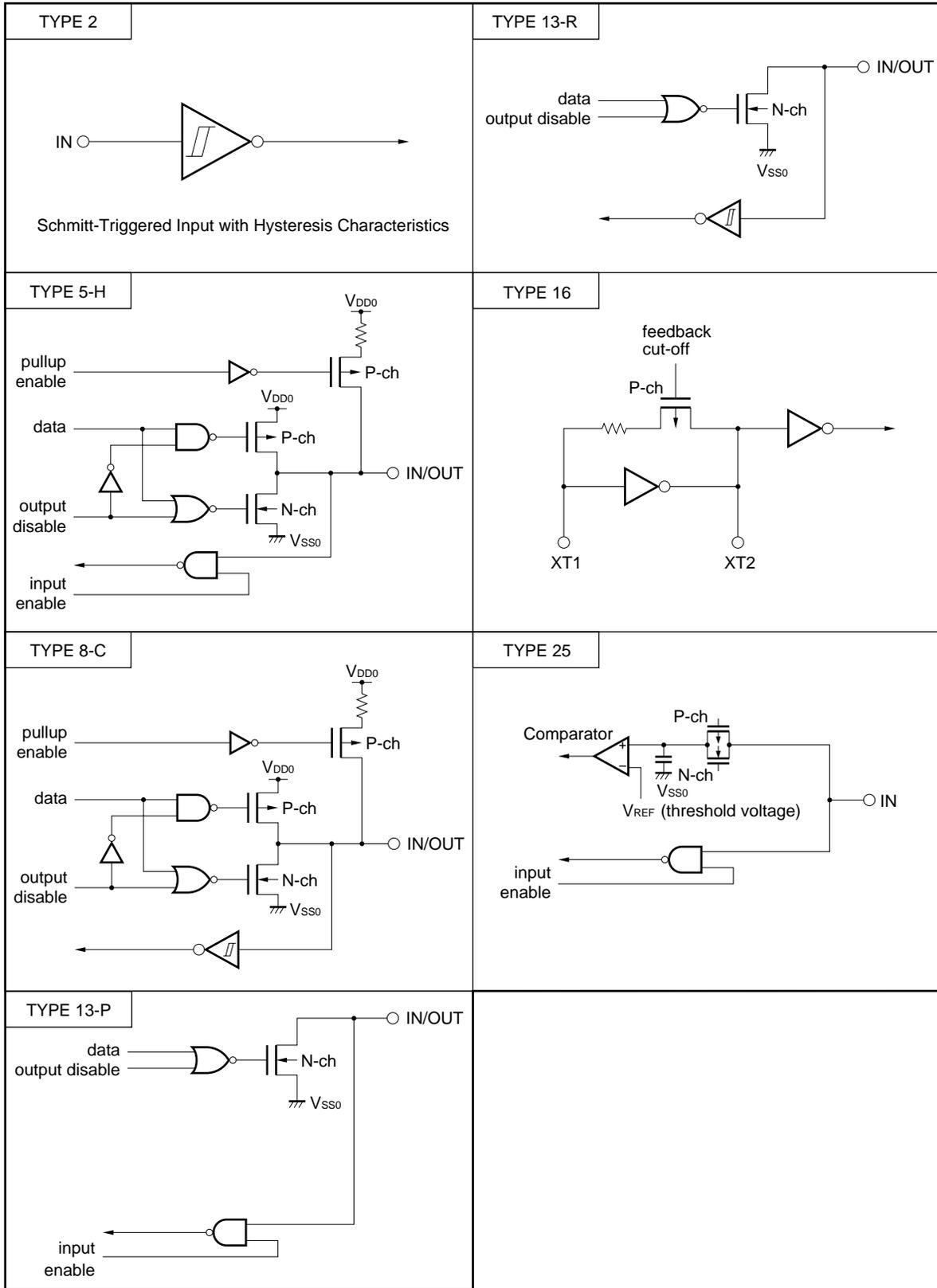
★ 2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

Table 2-1 shows the types of pin I/O circuits and recommended connection of unused pins.  
Refer to Figure 2-1 about the configuration of each type of I/O circuit.

**Table 2-1. Pin I/O Circuit Type**

Pin Name	Input/output Circuit Type	Input/Output	Recommended Connection of Unused Pins		
P00/INTP0	8-C	Input	Independently connect to V <sub>SS0</sub> via a resistor.		
P01/INTP1					
P02/INTP2					
P03/INTP3					
P10/ANI0 to P17/ANI7	25	Input	Independently connect to V <sub>DD0</sub> or V <sub>SS0</sub> via a resistor.		
P20/SI30	8-C	Input/output			
P21/SO30	5-H				
P22/SCK30	8-C				
P23/RxD0	5-H				
P24/TxD0					
P25/ASCK0				8-C	
P30, P31	13-P			Input/output	Independently connect to V <sub>DD0</sub> via a resistor.
P32/SDA0	13-R				
P33/SCL0					
P34	8-C	Independently connect to V <sub>DD0</sub> or V <sub>SS0</sub> via a resistor.			
P35	5-H				
P36	8-C				
P40/AD0 to P47/AD7	5-H	Input/output	Independently connect to V <sub>DD0</sub> via a resistor.		
P50/A8 to P57/A15	5-H	Input/output	Independently connect to V <sub>DD0</sub> or V <sub>SS0</sub> via a resistor.		
P64/RD		Input/output			
P65/WR					
P66/WAIT					
P67/ASTB					
P70/TI00/TO0				8-C	
P71/TI01					
P72/TI50/TO50					
P73/TI51/TO51					
P74/PCL					5-H
P75/BUZ					
RESET	2	Input	—		
XT1	16		—	Connect to V <sub>DD0</sub> .	
XT2		Leave open.			
AV <sub>DD</sub>	—	—	Connect to V <sub>DD0</sub> .		
AV <sub>REF</sub>			Connect to V <sub>SS0</sub> .		
AV <sub>SS</sub>					
V <sub>PP</sub>			Connect directly to V <sub>SS0</sub> or V <sub>SS1</sub> .		

Figure 2-1 Pin Input/Output Circuit



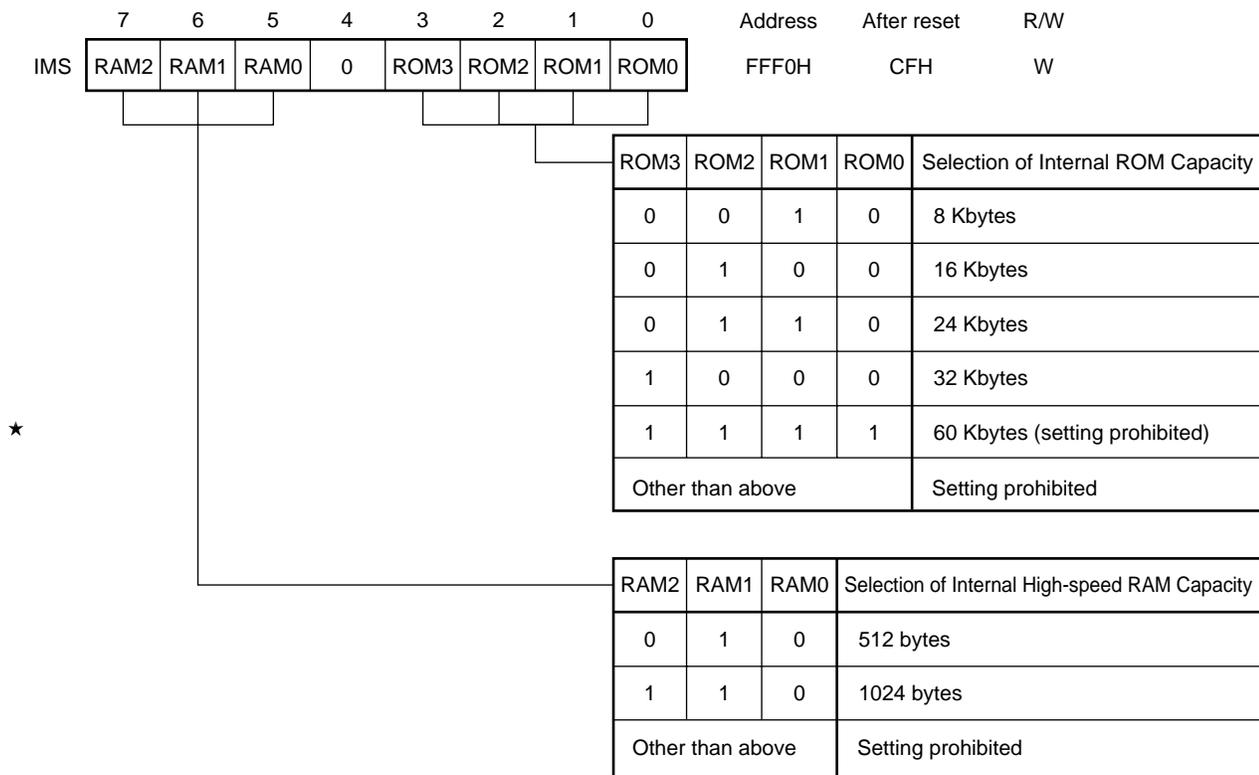
### 3. MEMORY SIZE SWITCHING REGISTER (IMS)

This register sets a part of internal memory not used by software. The memory mapping can be made the same as that of mask ROM versions with different types of internal memory (ROM and RAM).

The IMS is set with an 8-bit memory manipulation instruction.

RESET input sets the IMS to CFH.

Figure 3-1. Format of Memory Size Switching Register



★

Table 3-1 shows the IMS set value to make the memory mapping the same as those of mask ROM versions.

Table 3-1. Set Value of Memory Size Switching Register

Target Mask ROM Versions	IMS Set Value
μPD780031Y	42H
μPD780032Y	44H
μPD780033Y	C6H
μPD780034Y	C8H

★ **Caution** When using mask ROM versions, set values indicated in Table 3-1 to IMS.

#### 4. FLASH MEMORY PROGRAMMING

Writing to a flash memory can be performed without removing the memory from the target system. Writing is performed connecting the dedicated flash memory programmer (Flashpro II) to the host machine and the target system.

Also, it can be performed on an adapter for flash memory writing connected to the Flashpro II.

**Remark** Flashpro II is a product of Naitou Densai Machidaseisakusho Co., Ltd.

##### 4.1 Selection of Transmission Method

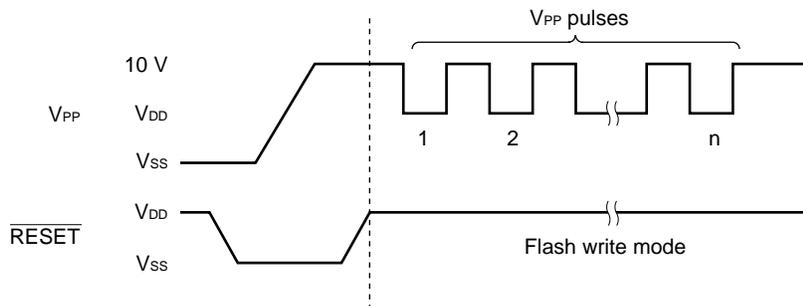
Writing to a flash memory is performed using the Flashpro II with a serial transmission mode. One of the transmission methods in Table 4-1 is selected. The selection of the transmission method is made by using the format shown in Figure 4-1. Each transmission method is selected by the number of  $V_{PP}$  pulses shown in Table 4-1.

**Table 4-1. Transmission Methods**

Transmission Method	Channels	Pin	$V_{PP}$ Pulses
3-wire serial I/O	1	SI30/P20 SO30/P21 $\overline{\text{SCK30/P22}}$	0
UART	1	RxD0/P23 TxD0/P24 ASCK0/P25	8
I <sup>2</sup> C bus	1	SDA0/P32 SCL0/P33	4
Pseudo 3-wire serial I/O	1	P72/TI50/TO50 (serial clock input) P71/TI01 (serial data output) P70/TI00/TO0 (serial data input)	12

**Caution** Be sure to select a communication system using the number of  $V_{PP}$  pulses shown in Table 4-1.

**Figure 4-1. Format of Transmission Method Selection**



### 4.2 Function of Flash Memory Programming

Operations such as writing to a flash memory are performed by various command/data transmission and reception operations according to the selected transmission method. Table 4-2 shows major functions of flash memory programming.

**Table 4-2. Major Functions of Flash Memory Programming**

Functions	Descriptions
Reset	Used to stop write operation and detect transmission cycle.
Batch verify	Compares the entire memory contents with the input data.
Batch delete	Deletes the entire memory contents.
Batch blank check	Checks the deletion status of the entire memory.
High-speed write	Performs write to the flash memory based on the write start address and the number of data to be written (number of bytes).
Continuous write	Performs continuous write based on the information input with high-speed write operation.
Status	Used to confirm the current operating mode and operation end.
Oscillation frequency setting	Sets the frequency of the resonator.
Delete time setting	Sets the memory delete time.
Silicon signature read	Outputs the device name and memory capacity, and device block information.

### 4.3 Connection of Flashpro II

The connection of the Flashpro II and the μPD78F0034Y differs according to the transmission method (3-wire serial I/O, UART, and I<sup>2</sup>C bus). The connection for each transmission method is shown in Figures 4-2, 4-3, and 4-4, respectively.

**Figure 4-2. Connection of Flashpro II for 3-wire Serial I/O System**

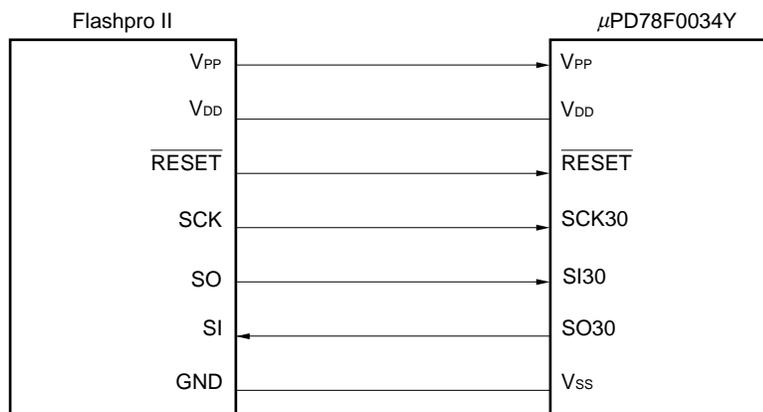


Figure 4-3. Connection of Flashpro II for UART System

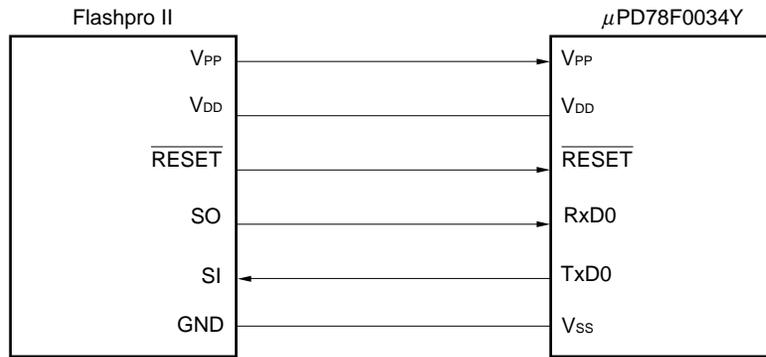
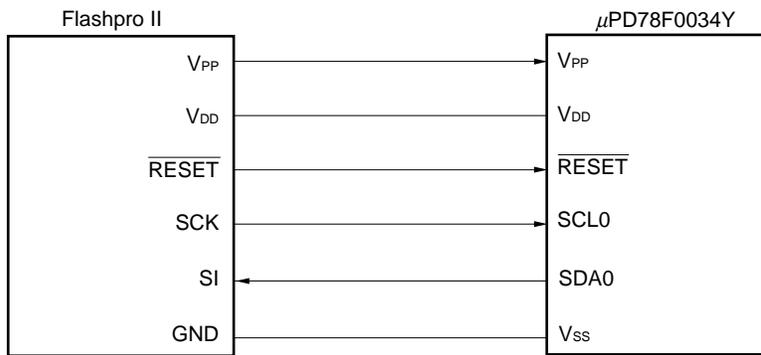


Figure 4-4. Connection of Flashpro II for I<sup>2</sup>C Bus System



★ 5. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T<sub>A</sub> = 25°C)

Parameter	Symbol	Test Conditions		Rating	Unit
Supply voltage	V <sub>DD</sub>			-0.3 to +6.5	V
	V <sub>PP</sub>			-0.3 to +11.0	V
	AV <sub>DD</sub>			-0.3 to V <sub>DD</sub> + 0.3	V
	AV <sub>REF</sub>			-0.3 to V <sub>DD</sub> + 0.3	V
	AV <sub>SS</sub>			-0.3 to +0.3	V
Input voltage	V <sub>I1</sub>	P00 to P03, P10 to P17, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, X1, X2, XT1, XT2, RESET		-0.3 to V <sub>DD</sub> + 0.3	V
	V <sub>I2</sub>	P30 to P33	N-ch Open-drain	-0.3 to V <sub>DD</sub> + 0.3	V
Output voltage	V <sub>O</sub>			-0.3 to V <sub>DD</sub> + 0.3	V
Analog input voltage	V <sub>AN</sub>	P10 to P17	Analog input pin	AV <sub>SS</sub> - 0.3 to AV <sub>REF</sub> + 0.3 and -0.3 to V <sub>DD</sub> + 0.3	V
High-level output current	I <sub>OH</sub>	Per pin		-10	mA
		Total for P00 to P03, P40 to P47, P50 to P57, P64 to P67, P70 to P75		-15	mA
		Total for P20 to P25, P30 to P36		-15	mA
Low-level output current	I <sub>OL</sub> <b>Note</b>	Per pin for P00 to P03, P20 to P25, P34 to P36, P40 to P47, P64 to P67, P70 to P75	Peak value	20	mA
			Effective value	10	mA
		Per pin for P30 to P33, P50 to P57	Peak value	30	mA
			Effective value	15	mA
		Total for P00 to P03, P40 to P47, P64 to P67, P70 to P75	Peak value	50	mA
			Effective value	20	mA
		Total for P20 to P25	Peak value	20	mA
			Effective value	10	mA
		Total for P30 to P36	Peak value	100	mA
			Effective value	70	mA
		Total for P50 to P57	Peak value	100	mA
			Effective value	70	mA
Operating ambient temperature	T <sub>A</sub>			-40 to +85	°C
Storage temperature	T <sub>stg</sub>			-65 to +150	°C

**Note** The effective value should be calculated as follows: [Effective value] = [Peak value] × √duty

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Capacitance (T<sub>A</sub> = 25°C, V<sub>DD</sub> = V<sub>SS</sub> = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C <sub>IN</sub>	f = 1 MHz Unmeasured pins returned to 0 V.				15	pF
I/O capacitance	C <sub>IO</sub>	f = 1 MHz Unmeasured pins returned to 0 V.	P00 to P03, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75,			15	pF
			P30 to P33			20	pF

**Remark** Unless otherwise specified, the characteristics of the alternate function are the same as those of the port-pin function.

Main System Clock Oscillator Characteristics (T<sub>A</sub> = -40 to 85°C, V<sub>DD</sub> = 2.7 to 5.5 V)

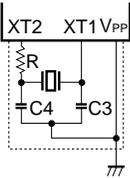
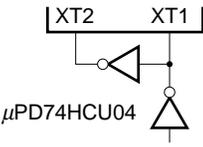
Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f <sub>x</sub> ) <sup>Note 1</sup>	V <sub>DD</sub> = 4.5 to 5.5 V	1.0		8.38	MHz
		Oscillation stabilization time <sup>Note 2</sup>	After V <sub>DD</sub> reaches oscillation voltage range MIN.	1.0		5.0	
Crystal resonator		Oscillation frequency (f <sub>x</sub> ) <sup>Note 1</sup>	V <sub>DD</sub> = 4.5 to 5.5 V	1.0		8.38	MHz
		Oscillation stabilization time <sup>Note 2</sup>	V <sub>DD</sub> = 4.5 to 5.5 V	1.0		5.0	
External clock		X1 input frequency (f <sub>x</sub> ) <sup>Note 1</sup>	V <sub>DD</sub> = 4.5 to 5.5 V	1.0		8.38	MHz
		X1 input high-/low-level width (t <sub>xH</sub> , t <sub>xL</sub> )	V <sub>DD</sub> = 4.5 to 5.5 V	50		500	
				85		500	

- Notes**
1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.
  2. Time required to stabilize oscillation after reset or STOP mode release.

**Cautions** 1. When using the main system clock oscillator, wiring in the area enclosed with the broken line in the above figures should be carried out as follows to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
  - Do not cross the wiring with the other signal lines.
  - Do not route the wiring near a signal line through which a high fluctuating current flows.
  - Always keep the ground point of the oscillator to the same potential as V<sub>SS1</sub>.
  - Do not ground the capacitor to a ground pattern in which a high current flows.
  - Do not fetch signals from the oscillator.
2. When the main system clock is stopped and the system is operated by the subsystem clock, switching back to the main system clock should be done after the oscillation stabilization time has been secured by the program.

**Subsystem Clock Oscillator Characteristics (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 2.7 to 5.5 V)**

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f <sub>XT</sub> ) <sup>Note 1</sup>		32	32.768	35	kHz
		Oscillation stabilization time <sup>Note 2</sup>	V <sub>DD</sub> = 4.5 to 5.5 V		1.2	2	s
External clock		XT1 input frequency (f <sub>XT</sub> ) <sup>Note 1</sup>		32		100	kHz
		XT1 input high-/low-level width (t <sub>XTH</sub> , t <sub>XTL</sub> )		5		15	μs

**Notes** 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after V<sub>DD</sub> reaches oscillation voltage MIN.

**Cautions** 1. When using the subsystem clock oscillator, wiring in the area enclosed with the broken line in the above figures should be carried out as follows to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
  - Do not cross the wiring with the other signal lines.
  - Do not route the wiring near a signal line through which a high fluctuating current flows.
  - Always keep the ground point of the oscillator to the same potential as V<sub>SS1</sub>.
  - Do not ground the capacitor to a ground pattern in which a high current flows.
  - Do not fetch signals from the oscillator.
2. The subsystem clock oscillator is a low-amplitude circuit in order to achieve a low consumption current, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

DC Characteristics (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit	
Input voltage, high	V <sub>IH1</sub>	P10 to P17, P21, P24, P35, P40 to P47, P50 to P57, P64 to P67, P74, P75	0.7V <sub>DD</sub>		V <sub>DD</sub>	V	
	V <sub>IH2</sub>	P00 to P03, P20, P22, P23, P25, P34, P36, P70 to P73, $\overline{\text{RESET}}$	0.8V <sub>DD</sub>		V <sub>DD</sub>	V	
	V <sub>IH3</sub>	P30 to P33 (N-ch open-drain)	0.7V <sub>DD</sub>		5.5	V	
	V <sub>IH4</sub>	X1, X2	V <sub>DD</sub> - 0.5		V <sub>DD</sub>	V	
	V <sub>IH5</sub>	XT1, XT2	V <sub>DD</sub> = 4.5 to 5.5 V	0.8V <sub>DD</sub>		V <sub>DD</sub>	V
			0.9V <sub>DD</sub>		V <sub>DD</sub>	V	
Input voltage, low	V <sub>IL1</sub>	P10 to P17, P21, P24, P35, P40 to P47, P50 to P57, P64 to P67, P74, P75	0		0.3V <sub>DD</sub>	V	
	V <sub>IL2</sub>	P00 to P03, P20, P22, P23, P25, P34, P36, P70 to P73, $\overline{\text{RESET}}$	0		0.2V <sub>DD</sub>	V	
	V <sub>IL3</sub>	P30 to P33	V <sub>DD</sub> = 4.5 to 5.5 V	0		0.3V <sub>DD</sub>	V
				0		0.2V <sub>DD</sub>	V
	V <sub>IL4</sub>	X1, X2	0		0.4	V	
V <sub>IL5</sub>	XT1, XT2	V <sub>DD</sub> = 4.5 to 5.5 V	0		0.2V <sub>DD</sub>	V	
			0		0.1V <sub>DD</sub>	V	
Output voltage, high	V <sub>OH1</sub>	V <sub>DD</sub> = 4.5 to 5.5 V, I <sub>OH</sub> = -1 mA	V <sub>DD</sub> - 1.0		V <sub>DD</sub>	V	
		I <sub>OH</sub> = -100 μA	V <sub>DD</sub> - 0.5		V <sub>DD</sub>	V	
Output voltage, low	V <sub>OL1</sub>	P30 to P33, P50 to P57	V <sub>DD</sub> = 4.5 to 5.5 V, I <sub>OL</sub> = 15 mA	0.4	2.0	V	
		P00 to P03, P20 to P25, P34 to P36, P40 to P47, P64 to P67, P70 to P75	V <sub>DD</sub> = 4.5 to 5.5 V, I <sub>OL</sub> = 1.6 mA		0.4	V	
	V <sub>OL2</sub>	I <sub>OL</sub> = 400 μA			0.5	V	

**Remark** Unless otherwise specified, the characteristics of the alternate function are the same as those of the port-pin function.

**DC Characteristics (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 2.7 to 5.5 V)**

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I <sub>LIH1</sub>	V <sub>IN</sub> = V <sub>DD</sub>	P00 to P03, P10 to P17, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, $\overline{\text{RESET}}$			3	μA
	I <sub>LIH2</sub>		X1, X2, XT1, XT2			20	μA
	I <sub>LIH3</sub>	V <sub>IN</sub> = 5.5 V	P30 to P33			80	μA
Input leakage current, low	I <sub>LIL1</sub>	V <sub>IN</sub> = 0 V	P00 to P03, P10 to P17, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, $\overline{\text{RESET}}$			-3	μA
	I <sub>LIL2</sub>		X1, X2, XT1, XT2			-20	μA
	I <sub>LIL3</sub>		P30 to P33			-3	μA
Output leakage current, low	I <sub>LOH</sub>	V <sub>OUT</sub> = V <sub>DD</sub>				3	μA
Output leakage current, low	I <sub>LOL</sub>	V <sub>OUT</sub> = 0 V				-3	μA
Software pull-up resistance	R	V <sub>IN</sub> = 0 V, P00 to P03, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75		15	30	90	kΩ
Power supply current <sup>Note 1</sup>	I <sub>DD1</sub>	8.38-MHz crystal oscillation operating mode	V <sub>DD</sub> = 5.0 V ±10%		9.5	19.0	mA
	I <sub>DD2</sub>	8.38-MHz crystal oscillation HALT mode	V <sub>DD</sub> = 5.0 V ±10%		1.6	3.2	mA
	I <sub>DD3</sub>	32.768-kHz crystal oscillation operating mode <sup>Note 2</sup>	V <sub>DD</sub> = 5.0 V ±10%		100	200	μA
			V <sub>DD</sub> = 3.0 V ±10%		70	140	μA
	I <sub>DD4</sub>	32.768-kHz crystal oscillation HALT mode <sup>Note 2</sup>	V <sub>DD</sub> = 5.0 V ±10%		25	55	μA
			V <sub>DD</sub> = 3.0 V ±10%		5	15	μA
I <sub>DD5</sub>	XT1 = V <sub>DD1</sub> . STOP mode When feedback resistor is used	V <sub>DD</sub> = 5.0 V ±10%		1	30	μA	
		V <sub>DD</sub> = 3.0 V ±10%		0.5	10	μA	
I <sub>DD6</sub>	XT1 = V <sub>DD1</sub> . STOP mode When feedback resistor is not used	V <sub>DD</sub> = 5.0 V ±10%		0.1	30	μA	
		V <sub>DD</sub> = 3.0 V ±10%		0.05	10	μA	

**Notes** 1. Does not include the current flowing into the on-chip pull-up resistor, the AV<sub>REF</sub> current, and port current.

2. When the main system clock is stopped.

**Remark** Unless otherwise specified, the characteristics of the alternate function are the same as those of the port-pin function.

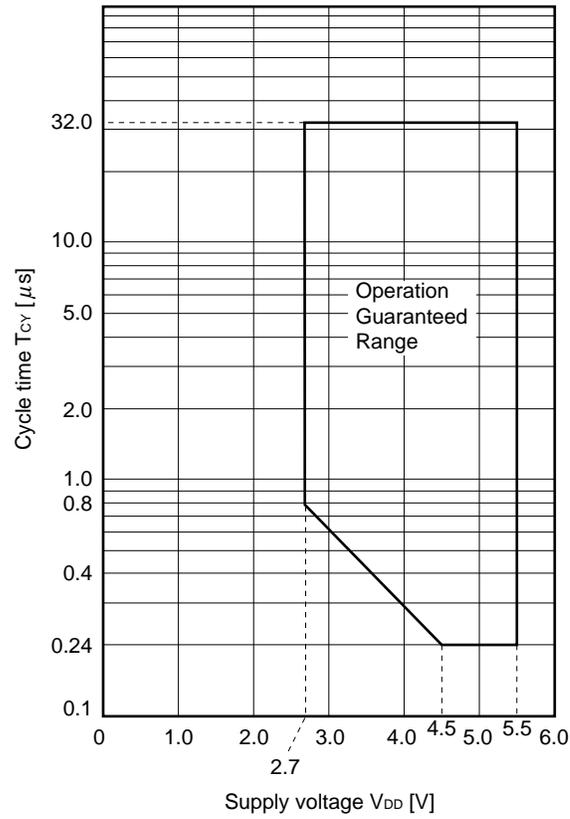
AC Characteristics

(1) Basic Operation (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit	
Cycle time (Min. instruction execution time)	T <sub>CY</sub>	Operating with main system clock	V <sub>DD</sub> = 4.5 to 5.5 V	0.24		32	μs
				0.8		32	μs
		Operating with subsystem clock	40 <sup>Note 1</sup>	122	125	μs	
TI00, TI01 input high-/low-level width	t <sub>TIH0</sub> , t <sub>TILO</sub>	3.5 V ≤ V <sub>DD</sub> ≤ 5.5 V	2/f <sub>sam</sub> + 0.1 <sup>Note 2</sup>			μs	
			2/f <sub>sam</sub> + 0.2 <sup>Note 2</sup>			μs	
TI50, TI51 input frequency	f <sub>TI5</sub>		0		4	MHz	
TI50, TI51 input high-/low-level width	t <sub>TIH5</sub> , t <sub>TI5L</sub>		100			ns	
Interrupt request input high-/low -level width	t <sub>INTH</sub> , t <sub>INTL</sub>	INTP0 to INTP3, P40 to P47	1			μs	
$\overline{\text{RESET}}$ low-level width	t <sub>RSL</sub>		10			μs	

- Notes**
1. Value when using the external clock. When using a crystal resonator, the value becomes 114 μs (MIN.).
  2. Selection of f<sub>sam</sub> = f<sub>x</sub>, f<sub>x</sub>/4, f<sub>x</sub>/64 is possible with bits 0 and 1 (PRM00, PRM01) of prescaler mode register 0 (PRM0). However, if the TI00 valid edge is selected as the count clock, the value becomes f<sub>sam</sub> = f<sub>x</sub>/8.

T<sub>CY</sub> vs V<sub>DD</sub> (at main system clock operation)



(2) Read/Write Operation (T<sub>A</sub> = -40 to + 85°C, V<sub>DD</sub> = 4.5 to 5.5 V) (1/2)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t <sub>ASTH</sub>		0.5t <sub>cy</sub>		ns
Address setup time	t <sub>ADS</sub>		t <sub>cy</sub> - 40		ns
Address hold time	t <sub>ADH</sub>		6		ns
Data input time from address	t <sub>ADD1</sub>			(2 + 2n)t <sub>cy</sub> - 54	ns
	t <sub>ADD2</sub>			(3 + 2n)t <sub>cy</sub> - 60	ns
Address output time from $\overline{RD}\downarrow$	t <sub>RDAD</sub>		0	100	ns
Data input time from $\overline{RD}\downarrow$	t <sub>RDD1</sub>			(2 + 2n)t <sub>cy</sub> - 87	ns
	t <sub>RDD2</sub>			(3 + 2n)t <sub>cy</sub> - 93	ns
Read data hold time	t <sub>RDH</sub>		0		ns
$\overline{RD}$ low-level width	t <sub>RDL1</sub>		(1.5 + 2n)t <sub>cy</sub> - 33		ns
	t <sub>RDL2</sub>		(2.5 + 2n)t <sub>cy</sub> - 33		ns
$\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$	t <sub>RDWT1</sub>			0.5t <sub>cy</sub> - 43	ns
	t <sub>RDWT2</sub>			t <sub>cy</sub> - 43	ns
$\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$	t <sub>WRWT</sub>			0.5t <sub>cy</sub> - 25	ns
$\overline{WAIT}$ low-level width	t <sub>WTL</sub>		(0.5 + 2n)t <sub>cy</sub> + 10	(2 + 2n)t <sub>cy</sub>	ns
Write data setup time	t <sub>WDS</sub>		60		ns
Write data hold time	t <sub>WDH</sub>		6		ns
$\overline{WR}$ low-level width	t <sub>WRL1</sub>		(1.5 + 2n)t <sub>cy</sub> - 15		ns
$\overline{RD}\downarrow$ delay time from $\overline{ASTB}\downarrow$	t <sub>ASTRD</sub>		6		ns
$\overline{WR}\downarrow$ delay time from $\overline{ASTB}\downarrow$	t <sub>ASTWR</sub>		2t <sub>cy</sub> - 15		ns
ASTB $\uparrow$ delay time from $\overline{RD}\uparrow$ in external fetch	t <sub>RDAST</sub>		0.8t <sub>cy</sub> - 15	1.2t <sub>cy</sub>	ns
Address hold time from $\overline{RD}\uparrow$ in external fetch	t <sub>RDADH</sub>		0.8t <sub>cy</sub> - 15	1.2t <sub>cy</sub> + 30	ns
Write data output time from $\overline{RD}\uparrow$	t <sub>RDWD</sub>		40		ns
Write data output time from $\overline{WR}\downarrow$	t <sub>WRWD</sub>		10	60	ns
Address hold time from $\overline{WR}\uparrow$	t <sub>WRADH</sub>		0.8t <sub>cy</sub> - 15	1.2t <sub>cy</sub> + 30	ns
$\overline{RD}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t <sub>WTRD</sub>		0.8t <sub>cy</sub>	2.5t <sub>cy</sub> + 25	ns
$\overline{WR}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t <sub>WTWR</sub>		0.8t <sub>cy</sub>	2.5t <sub>cy</sub> + 25	ns

Remarks 1. t<sub>cy</sub> = T<sub>cy</sub>/4

2. n indicates the number of waits.

(2) Read/Write Operation (T<sub>A</sub> = -40 to + 85°C, V<sub>DD</sub> = 2.7 to 4.5 V) (2/2)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t <sub>ASTH</sub>		0.5t <sub>cy</sub>		ns
Address setup time	t <sub>ADS</sub>		0.5t <sub>cy</sub> - 54		ns
Address hold time	t <sub>ADH</sub>		10		ns
Data input time from address	t <sub>ADD1</sub>			(2 + 2n)t <sub>cy</sub> - 108	ns
	t <sub>ADD2</sub>			(3 + 2n)t <sub>cy</sub> - 120	ns
Address output time from $\overline{RD}\downarrow$	t <sub>RDAD</sub>		0	200	ns
Data input time from $\overline{RD}\downarrow$	t <sub>RDD1</sub>			(2 + 2n)t <sub>cy</sub> - 148	ns
	t <sub>RDD2</sub>			(3 + 2n)t <sub>cy</sub> - 162	ns
Read data hold time	t <sub>RDH</sub>		0		ns
$\overline{RD}$ low-level width	t <sub>RDL1</sub>		(1.5 + 2n)t <sub>cy</sub> - 40		ns
	t <sub>RDL2</sub>		(2.5 + 2n)t <sub>cy</sub> - 40		ns
$\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$	t <sub>RDWT1</sub>			0.5t <sub>cy</sub> - 60	ns
	t <sub>RDWT2</sub>			t <sub>cy</sub> - 60	ns
$\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$	t <sub>WRWT</sub>			0.5t <sub>cy</sub> - 50	ns
$\overline{WAIT}$ low-level width	t <sub>WTL</sub>		(0.5 + 2n)t <sub>cy</sub> + 10	(2 + 2n)t <sub>cy</sub>	ns
Write data setup time	t <sub>WDS</sub>		60		ns
Write data hold time	t <sub>WDH</sub>		10		ns
$\overline{WR}$ low-level width	t <sub>WRL1</sub>		(1.5 + 2n)t <sub>cy</sub> - 30		ns
$\overline{RD}\downarrow$ delay time from $\overline{ASTB}\downarrow$	t <sub>ASTRD</sub>		10		ns
$\overline{WR}\downarrow$ delay time from $\overline{ASTB}\downarrow$	t <sub>ASTWR</sub>		2t <sub>cy</sub> - 30		ns
ASTB $\uparrow$ delay time from $\overline{RD}\uparrow$ in external fetch	t <sub>RDAST</sub>		0.8t <sub>cy</sub> - 30	1.2t <sub>cy</sub>	ns
Address hold time from $\overline{RD}\uparrow$ in external fetch	t <sub>RDADH</sub>		0.8t <sub>cy</sub> - 30	1.2t <sub>cy</sub> + 60	ns
Write data output time from $\overline{RD}\uparrow$	t <sub>RDWD</sub>		40		ns
Write data output time from $\overline{WR}\downarrow$	t <sub>WRWD</sub>		20	120	ns
Address hold time from $\overline{WR}\uparrow$	t <sub>WRADH</sub>		0.8t <sub>cy</sub> - 30	1.2t <sub>cy</sub> + 60	ns
$\overline{RD}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t <sub>WTRD</sub>		0.5t <sub>cy</sub>	2.5t <sub>cy</sub> + 50	ns
$\overline{WR}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t <sub>WTWR</sub>		0.5t <sub>cy</sub>	2.5t <sub>cy</sub> + 50	ns

Remarks 1. t<sub>cy</sub> = T<sub>cy</sub>/4

2. n indicates the number of waits.

(3) Serial Interface (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 2.7 to 5.5 V)

(a) 3-wire serial I/O mode (SCK30 ... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
SCK30 cycle time	t <sub>KCY1</sub>	V <sub>DD</sub> = 4.5 to 5.5 V	954			ns
			1600			ns
SCK30 high-/low-level width	t <sub>KH1</sub> , t <sub>KL1</sub>	V <sub>DD</sub> = 4.5 to 5.5 V	t <sub>KCY1</sub> /2 - 50			ns
			t <sub>KCY1</sub> /2 - 100			ns
SI30 setup time (to SCK30, SCK31↑)	t <sub>SIK1</sub>	V <sub>DD</sub> = 4.5 to 5.5 V	100			ns
			150			ns
SI30 hold time (from SCK30, SCK31↑)	t <sub>KS1</sub>		400			ns
SO30 output delay time from SCK30↓	t <sub>KSO1</sub>	C = 100 pF <sup>Note</sup>			300	ns

**Note** C is the load capacitance of the SCK30, SO30 output lines.

(b) 3-wire serial I/O mode (SCK30 ... External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
SCK30	t <sub>KCY2</sub>	V <sub>DD</sub> = 4.5 to 5.5 V	800			ns
			1600			ns
SCK30, high-/low-level width	t <sub>KH2</sub> , t <sub>KL2</sub>	V <sub>DD</sub> = 4.5 to 5.5 V	400			ns
			800			ns
SI30 setup time (to SCK30↑)	t <sub>SIK2</sub>		100			ns
SI30 hold time (from SCK30↑)	t <sub>KS2</sub>		400			ns
SO30 output delay time from SCK30↓	t <sub>KSO2</sub>	C = 100 pF <sup>Note</sup>			300	ns
SCK30 rise fall time	t <sub>R2</sub> , t <sub>F2</sub>	When using external device expansion function			160	ns
		When not using external device expansion function	When using 16-bit timer output function		700	ns
			When not using 16-bit timer output function		1000	ns

**Note** C is the load capacitance of the SO30 output line.

(c) UART mode (Dedicated baud rate generator output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		V <sub>DD</sub> = 4.5 to 5.5 V			125000	bps
					78125	bps

(d) UART mode (External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
ASCK0 cycle time	t <sub>KCY3</sub>	V <sub>DD</sub> = 4.5 to 5.5 V	800			ns
			1600			ns
ASCK0 high-/low-level width	t <sub>KH3</sub> , t <sub>KL3</sub>	V <sub>DD</sub> = 4.5 to 5.5 V	400			ns
			800			ns
Transfer rate		V <sub>DD</sub> = 4.5 to 5.5 V			39063	bps
					19531	bps
ASCK0 rise, fall time	t <sub>r3</sub> , t <sub>f3</sub>	V <sub>DD</sub> = 4.5 to 5.5 V, when not using external device expansion function			1000	ns
					160	ns

(e) UART mode (Infrared ray data transfer mode)

Parameter	Symbol	Test Conditions	TYP.	MAX.	Unit
Transfer rate		V <sub>DD</sub> = 4.5 to 5.5 V		115200	bps
Bit rate allowable error		V <sub>DD</sub> = 4.5 to 5.5 V		±0.87	%
Output pulse width		V <sub>DD</sub> = 4.5 to 5.5 V	1.2	0.24/f <sub>br</sub> <sup>Note</sup>	μs
Input pulse width		V <sub>DD</sub> = 4.5 to 5.5 V	4/f <sub>x</sub>		μs

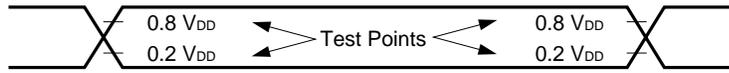
**Note** fbr: specified baud rate

(f) I<sup>2</sup>C bus Mode

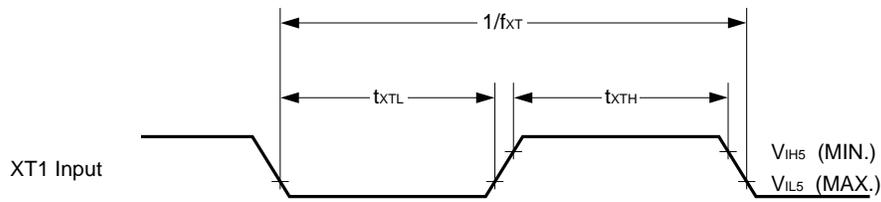
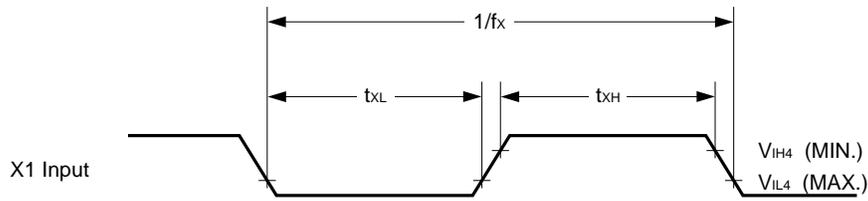
Parameter	Symbol	Standard Mode		High-speed Mode		Unit	
		MIN.	MAX.	MIN.	MAX.		
SCL0 clock frequency	f <sub>CLK</sub>	0	100	0	400	kHz	
Bus free time (between stop and start conditions)	t <sub>BUF</sub>	4.7	—	1.3	—	μs	
Hold time <sup>Note 1</sup>	t <sub>HD:STA</sub>	4.0	—	0.6	—	μs	
SCL0 clock low-level width	t <sub>LOW</sub>	4.7	—	1.3	—	μs	
SCL0 clock high-level width	t <sub>HIGH</sub>	4.0	—	0.6	—	μs	
Start/restart condition setup time	t <sub>SU:STA</sub>	4.7	—	0.6	—	μs	
Data hold time	CBUS compatible master	t <sub>HD:DAT</sub>	5.0	—	—	—	μs
	I <sup>2</sup> C bus		0 <sup>Note 2</sup>	—	0 <sup>Note 2</sup>	0.9 <sup>Note 3</sup>	μs
Data setup time	t <sub>SU:DAT</sub>	250	—	100 <sup>Note 4</sup>	—	ns	
SDA0 and SCL0 signal rise time	t <sub>r</sub>	—	1000	20 + 0.1Cb <sup>Note 5</sup>	300	ns	
SDA0 and SCL0 signal fall time	t <sub>f</sub>	—	300	20 + 0.1Cb <sup>Note 5</sup>	300	ns	
Stop condition setup time	t <sub>SU:STO</sub>	4.0	—	0.6	—	μs	
Spike pulse width controlled by input filter	t <sub>SP</sub>	—	—	0	50	ns	
Capacitive load per each bus line	C <sub>b</sub>	—	400	—	400	pF	

- Notes**
1. On start condition, the first clock pulse is generated after this period.
  2. To fulfill undefined area of the SCL0 falling edge, it is necessary for the device to provide internally SDA0 signal (on V<sub>IHmin.</sub> of SCL0 signal) with at least 300 ns of hold time.
  3. If the device does not extend the SCL0 signal low hold time (t<sub>LOW</sub>), only maximum data hold time (t<sub>HD:DAT</sub>) needs to be fulfilled.
  4. The high-speed mode I<sup>2</sup>C bus is available in the standard mode I<sup>2</sup>C bus system. At this time, the conditions described below must be satisfied.
    - If the device does not extend the SCL0 signal low state hold time  
t<sub>SU:DAT</sub> ≥ 250 ns
    - If the device extends the SCL0 signal low state hold time  
Be sure to transmit the next data bit to the SDA0 line before the SCL0 line is released (t<sub>Rmax.</sub> + t<sub>SU:DAT</sub> = 1000 + 250 = 1250 ns by standard mode I<sup>2</sup>C bus specification).
  5. C<sub>b</sub> : total capacitance per one bus line (unit : pF)

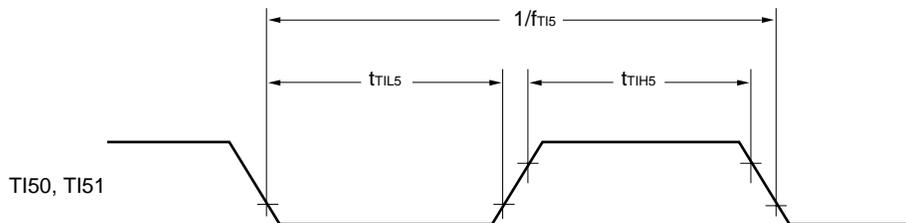
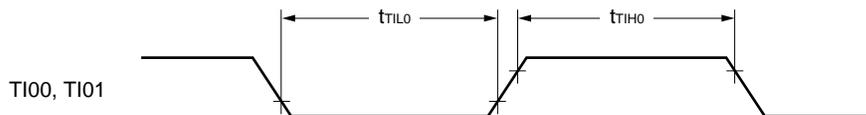
AC Timing Test Point (Excluding X1, XT1 Input)



Clock Timing

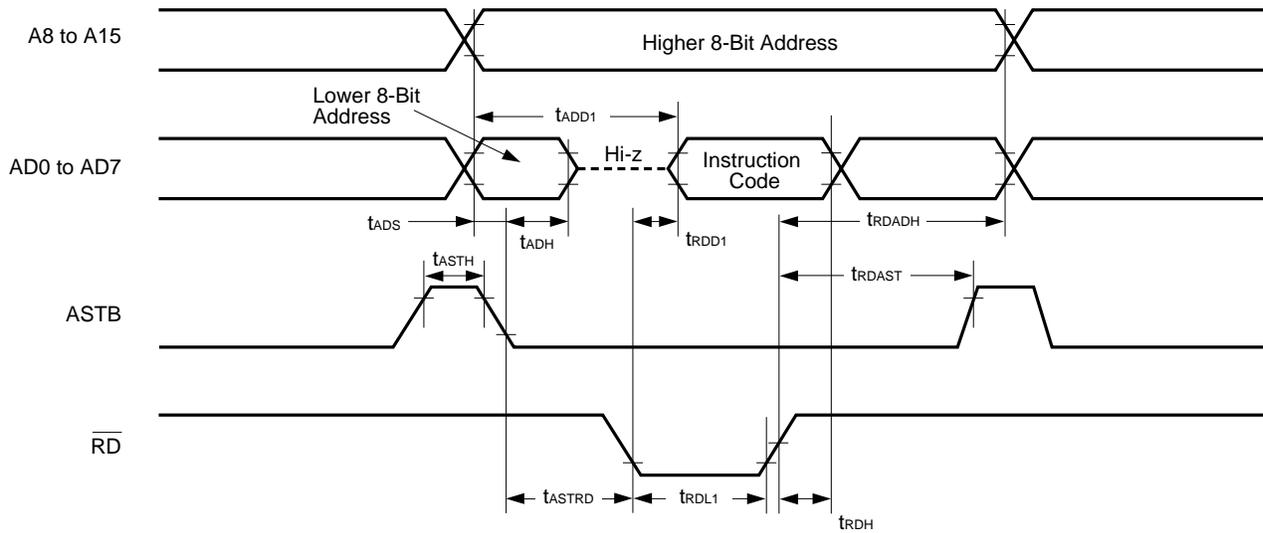


TI Timing

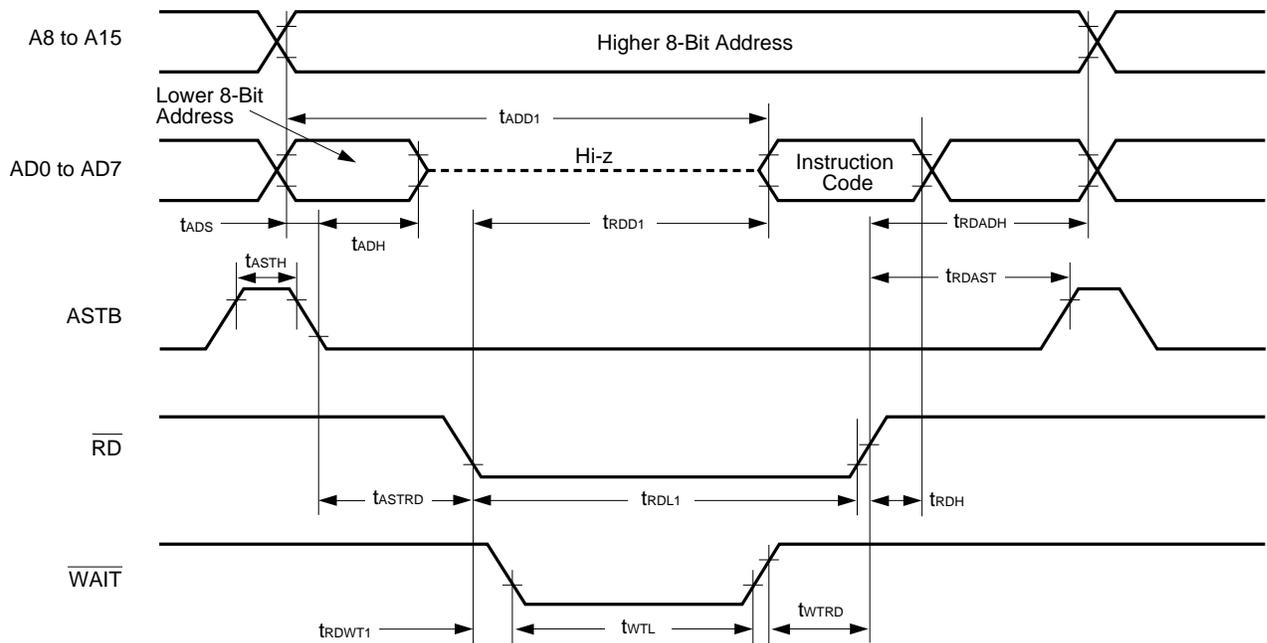


Read/Write Operation

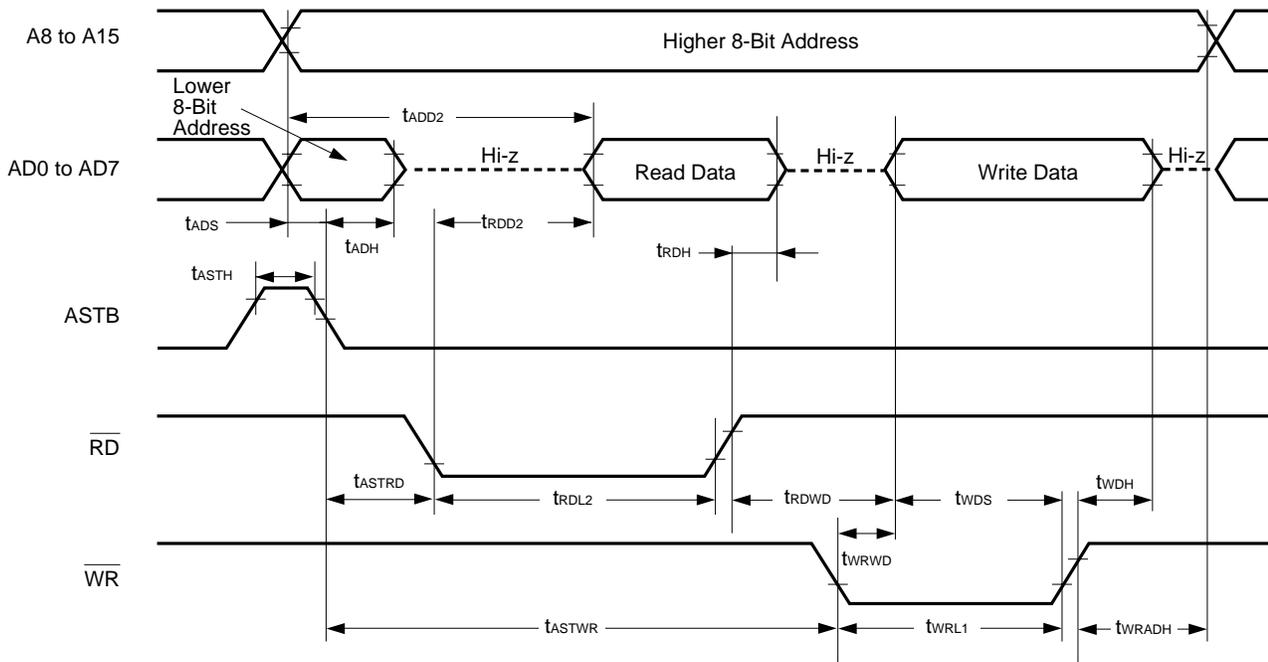
External Fetch (No Wait) :



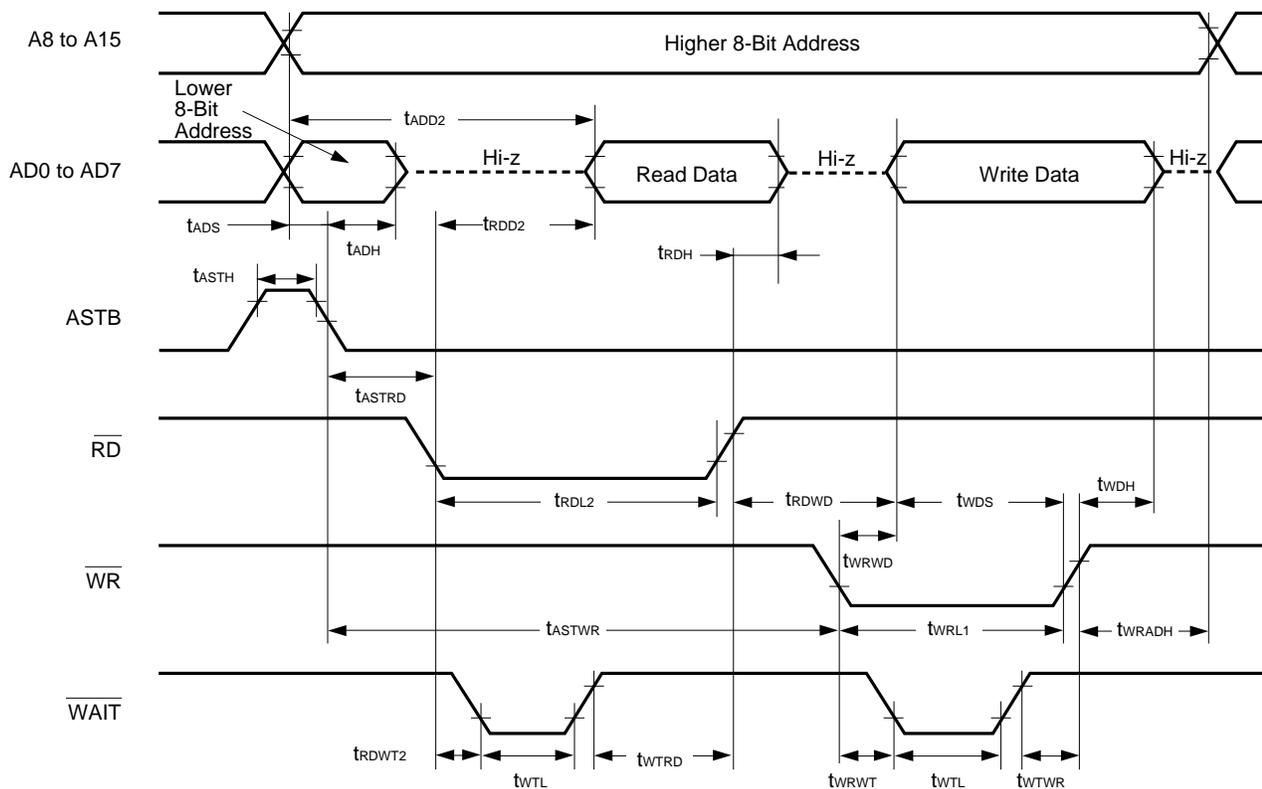
External Fetch (Wait Insertion) :



External Data Access (No Wait) :

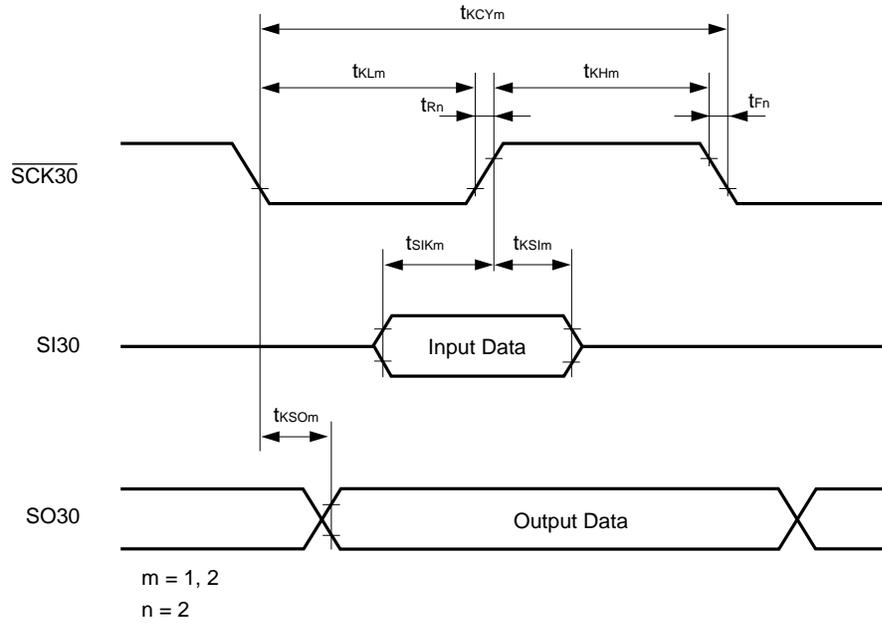


External Data Access (Wait Insertion) :

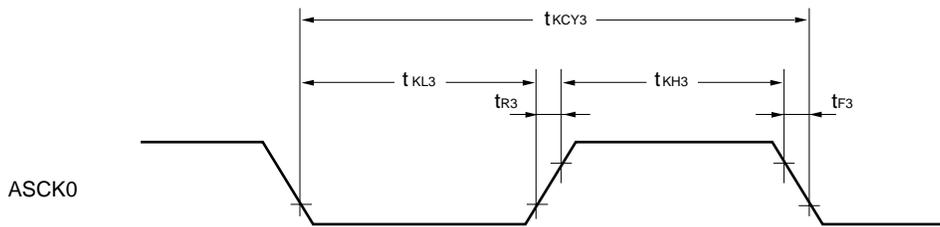


Serial Transfer Timing

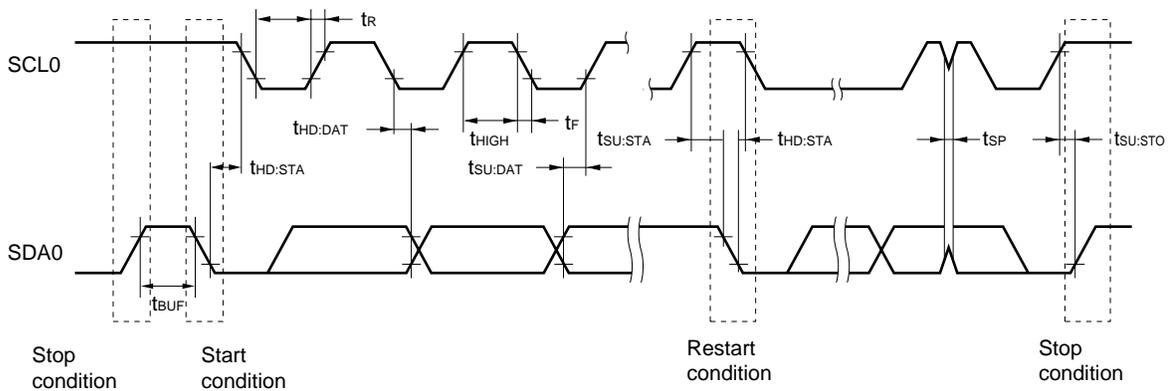
3-wire Serial I/O Mode :



UART Mode (External Clock Input) :



I<sup>2</sup>C Bus Mode



**A/D Converter Characteristics (T<sub>A</sub> = -40 to 85°C, V<sub>DD</sub> = AV<sub>DD</sub> = AV<sub>REF</sub> = 2.7 to 5.5 V, AV<sub>SS</sub> = V<sub>SS</sub> = 0 V)**

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Overall error <sup>Note</sup>		AV <sub>REF</sub> = 4.5 to 5.5 V			±0.4	%
					±0.7	%
Conversion time	T <sub>CONV</sub>	AV <sub>REF</sub> = 4.5 to 5.5 V	14		200	μs
			20		200	μs
Analog input voltage	V <sub>IAN</sub>		0		AV <sub>REF</sub> + 0.3	V
Reference voltage	AV <sub>REF</sub>		2.7		AV <sub>DD</sub>	V
AV <sub>REF</sub> resistance	RA <sub>REF</sub>		10	20		kΩ

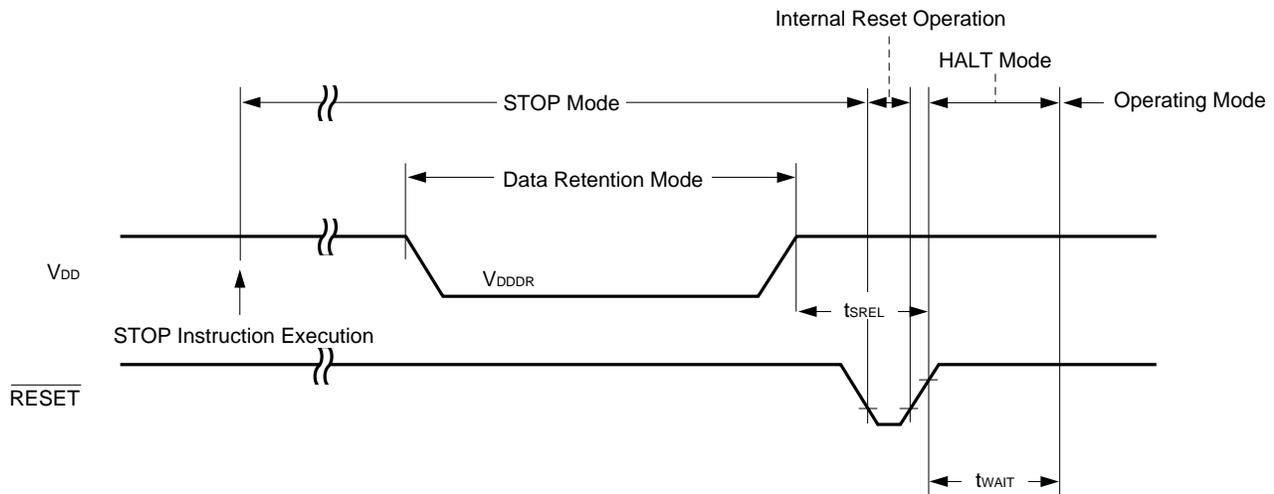
**Note** Excluding quantization error (±1/2LSB). Shown as a percentage of the full scale value.

**Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T<sub>A</sub> = -40 to +85°C)**

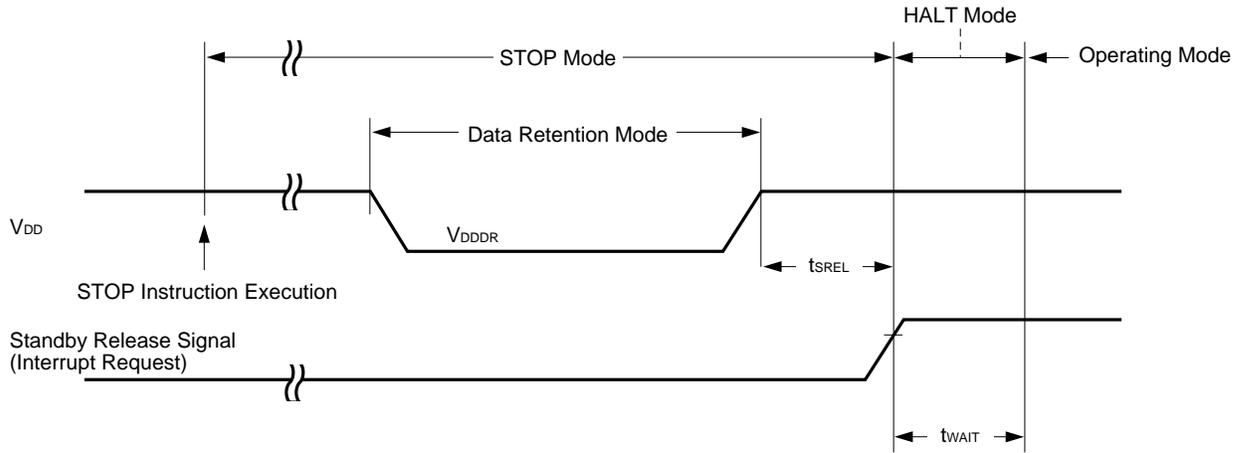
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V <sub>DDDR</sub>		1.6		5.5	V
Data retention power supply current	I <sub>DDDR</sub>	V <sub>DDDR</sub> = 1.6 V Subsystem clock stops and feed-back resistor disconnected		0.1	10	μA
Release signal set time	t <sub>SREL</sub>		0			μs
Oscillation stabilization wait time	t <sub>WAIT</sub>	Release by $\overline{\text{RESET}}$		2 <sup>17</sup> /f <sub>x</sub>		ms
		Release by interrupt request		<b>Note</b>		ms

**Note** Selection of 2<sup>12</sup>/f<sub>x</sub> and 2<sup>14</sup>/f<sub>x</sub> to 2<sup>17</sup>/f<sub>x</sub> is possible with bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

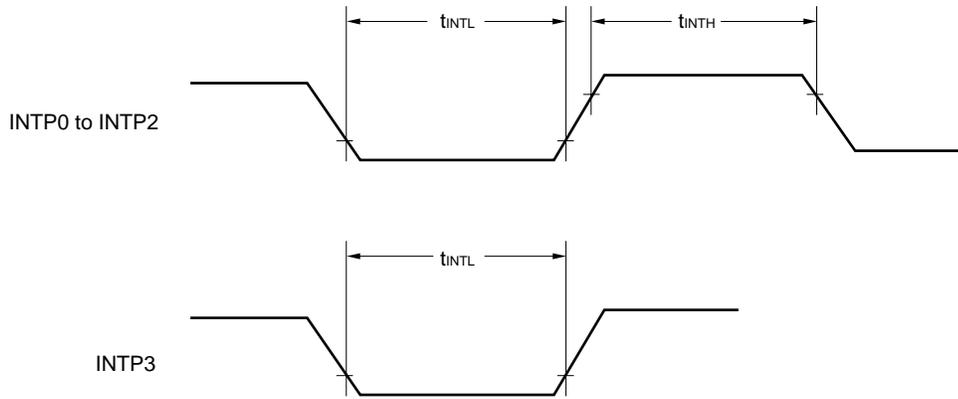
**Data Retention Timing (STOP Mode Release by  $\overline{\text{RESET}}$ )**



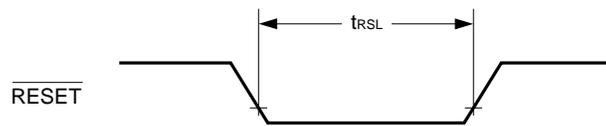
Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Request Signal)



Interrupt Request Input Timing

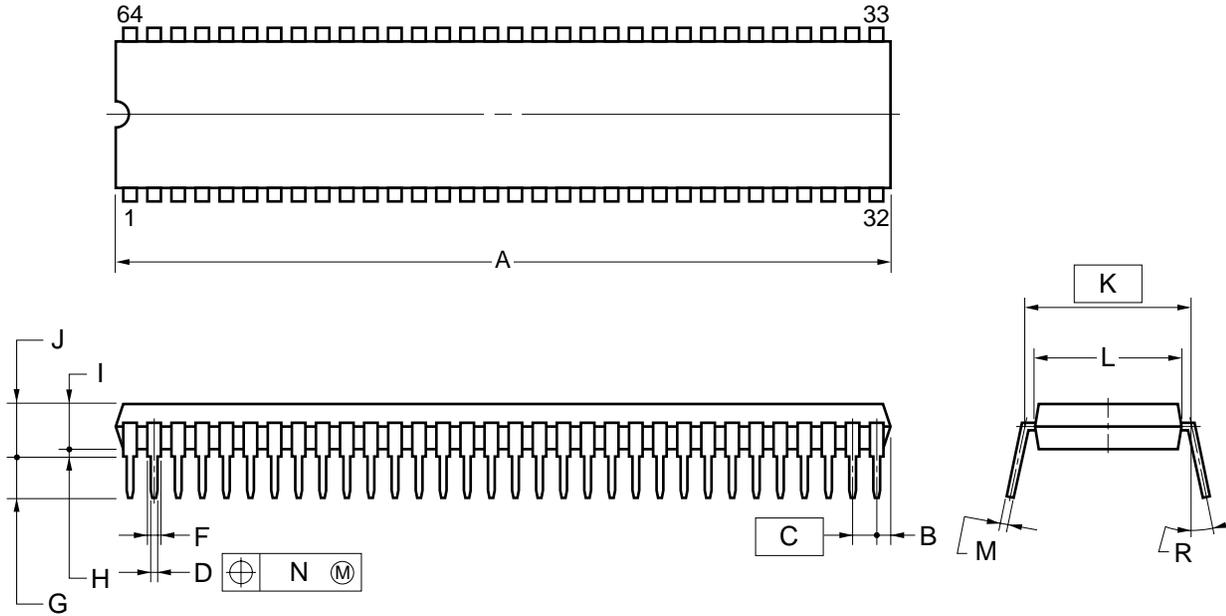


RESET Input Timing



6. PACKAGE DRAWINGS

64-PIN PLASTIC SHRINK DIP (750 mils) (Unit: mm)



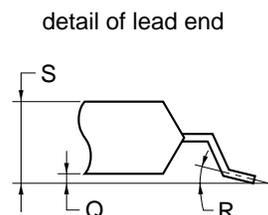
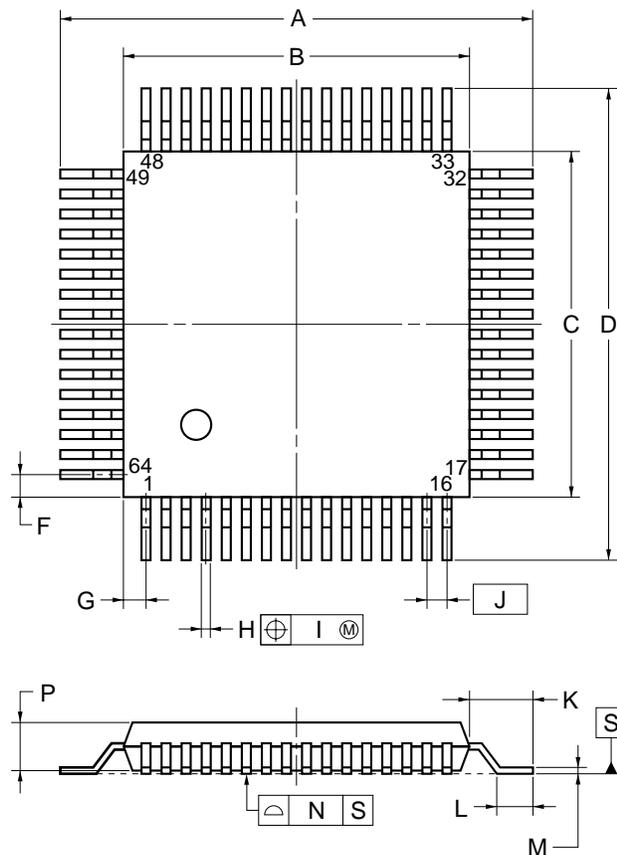
NOTES

1. Controlling dimension— millimeter.
2. Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
3. Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.0 <sup>+0.68</sup> <sub>-0.20</sub>	2.283 <sup>+0.028</sup> <sub>-0.008</sub>
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50±0.10	0.020 <sup>+0.004</sup> <sub>-0.005</sub>
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.05 <sup>+0.26</sup> <sub>-0.20</sub>	0.159 <sup>+0.011</sup> <sub>-0.008</sub>
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0±0.2	0.669 <sup>+0.009</sup> <sub>-0.008</sub>
M	0.25 <sup>+0.10</sup> <sub>-0.05</sub>	0.010 <sup>+0.004</sup> <sub>-0.003</sub>
N	0.17	0.007
R	0 to 15°	0 to 15°

P64C-70-750A,C-3

64-PIN PLASTIC QFP (14 x 14) (Unit: mm)



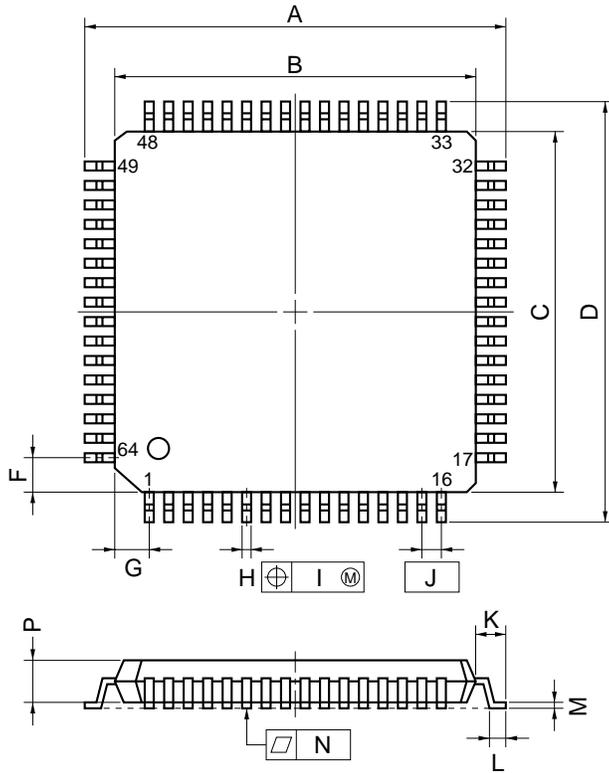
NOTE

1. Controlling dimension — millimeter.
2. Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

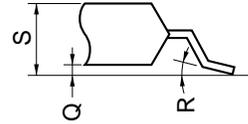
ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	0.551 <sup>+0.009</sup> <sub>-0.008</sub>
C	14.0±0.2	0.551 <sup>+0.009</sup> <sub>-0.008</sub>
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.37 <sup>+0.08</sup> <sub>-0.07</sub>	0.015 <sup>+0.003</sup> <sub>-0.004</sub>
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071±0.008
L	0.8±0.2	0.031 <sup>+0.009</sup> <sub>-0.008</sub>
M	0.17 <sup>+0.08</sup> <sub>-0.07</sub>	0.007 <sup>+0.003</sup> <sub>-0.004</sub>
N	0.10	0.004
P	2.55±0.1	0.100±0.004
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	2.85 MAX.	0.113 MAX.

P64GC-80-AB8-4

64-PIN PLASTIC LQFP (12 x 12) (Unit: mm)



detail of lead end



NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.8±0.4	0.583±0.016
B	12.0±0.2	0.472 <sup>+0.009</sup> <sub>-0.008</sub>
C	12.0±0.2	0.472 <sup>+0.009</sup> <sub>-0.008</sub>
D	14.8±0.4	0.583±0.016
F	1.125	0.044
G	1.125	0.044
H	0.30±0.10	0.012 <sup>+0.004</sup> <sub>-0.005</sub>
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.4±0.2	0.055±0.008
L	0.6±0.2	0.024 <sup>+0.008</sup> <sub>-0.009</sub>
M	0.15 <sup>+0.10</sup> <sub>-0.05</sub>	0.006 <sup>+0.004</sup> <sub>-0.003</sub>
N	0.10	0.004
P	1.4	0.055
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	1.7 MAX.	0.067 MAX.

P64GK-65-8A8-1

★ **APPENDIX A. DEVELOPMENT TOOLS**

The following development tools are available for system development using the μPD78F0034Y.  
Be sure to refer to **(5) Cautions on using development tools.**

**(1) Language Processing Software**

RA78K/0	Assembler package common to 78K/0 Series
CC78K/0	C compiler package common to 78K/0 Series
DF780034	Device file common to μPD780034 Subseries
CC78K/0-L	C compiler library source file common to 78K/0 Series

**(2) Flash Memory Writing Tools**

Flashpro II (FL-PR2)	Flash programmer dedicated to on-chip flash memory microcontroller
FA-64CW FA-64GC FA-64GK <sup>Note</sup>	Adapter for flash writing

**Note** Under development

**(3) Debugging Tool**

- **When using in-circuit emulator IE-78K0-NS**

IE-78K0-NS <sup>Note</sup>	In-circuit emulator common to 78K/0 Series
IE-70000-MC-PS-B	Power supply unit for IE-78K0-NS
IE-70000-98-IF-C <sup>Note</sup>	Interface adapter when using PC-9800 series as host machine (excluding notebook PCs)
IE-70000-CD-IF <sup>Note</sup>	PC card and interface cable when using notebook PC of PC-9800 series as host machine
IE-70000-PC-IF-C <sup>Note</sup>	Interface adapter when using IBM PC/AT™ or compatible as host machine
IE-780034-NS-EM1 <sup>Note</sup>	Emulation board to emulate μPD780034 Subseries
NP-64CW	Emulation probe for 64-pin plastic shrink DIP (CW type)
NP-64GC	Emulation probe for 64-pin plastic QFP (GC-AB8 type)
NP-64GK <sup>Note</sup>	Emulation probe for 64-pin plastic LQFP (GK-8A8 type)
TGK-064SBW	Conversion adapter for connecting target system board designed to allow mounting of 64-pin plastic LQFP (GK-8A8 type) and NP-64GK.
EV-9200GC-64	Socket to be mounted on target system board manufactured for 64-pin plastic QFP (GC-AB8 type)
ID78K0-NS <sup>Note</sup>	Integrated debugger for IE-78K0-NS
SM78K0	System simulator common to 78K/0 Series
DF780034	Device file common to μPD780034 Subseries

**Note** Under development

- When using in-circuit emulator IE-78001-R-A

IE-78001-R-A <sup>Note</sup>	In-circuit emulator common to 78K/0 Series
IE-70000-98-IF-B IE-70000-98-IF-C <sup>Note</sup>	Interface adapter when using PC-9800 series as host machine (excluding notebook PCs)
IE-70000-PC-IF-B IE-70000-PC-IF-C <sup>Note</sup>	Interface adapter when using IBM PC/AT or compatible as host machine
IE-78000-R-SV3	Interface adapter and cable when using EWS as host machine
IE-780034-NS-EM1 <sup>Note</sup>	Emulation board to emulate μPD780034 Subseries
IE-78K0-R-EX1 <sup>Note</sup>	Emulation probe conversion board to use IE-780034-NS-EM1 on IE-78001-R-A
EP-78240CW-R	Emulation probe for 64-pin plastic shrink DIP (CW type)
EP-78240GC-R	Emulation probe for 64-pin plastic QFP (GC-AB8 type)
EP-78012GK-R	Emulation probe for 64-pin plastic LQFP (GK-8A8 type)
TGK-064SBW	Conversion adapter for connecting target system board and EP-78012GK-R designed to allow mounting of 64-pin plastic LQFP (GK-8A8).
EV-9200GC-64	Socket to be mounted on target system board manufactured for 64-pin plastic QFP (GC-AB8 type)
ID78K0	Integrated debugger for IE-78001-R-A
SM78K0	System simulator common to 78K/0 Series
DF780034	Device file common to μPD780034 Subseries

**Note** Under development

**(4) Real-time OS**

RX78K/0	Real-time OS for 78K/0 Series
MX78K0	OS for 78K/0 Series

**(5) Cautions on using development tools**

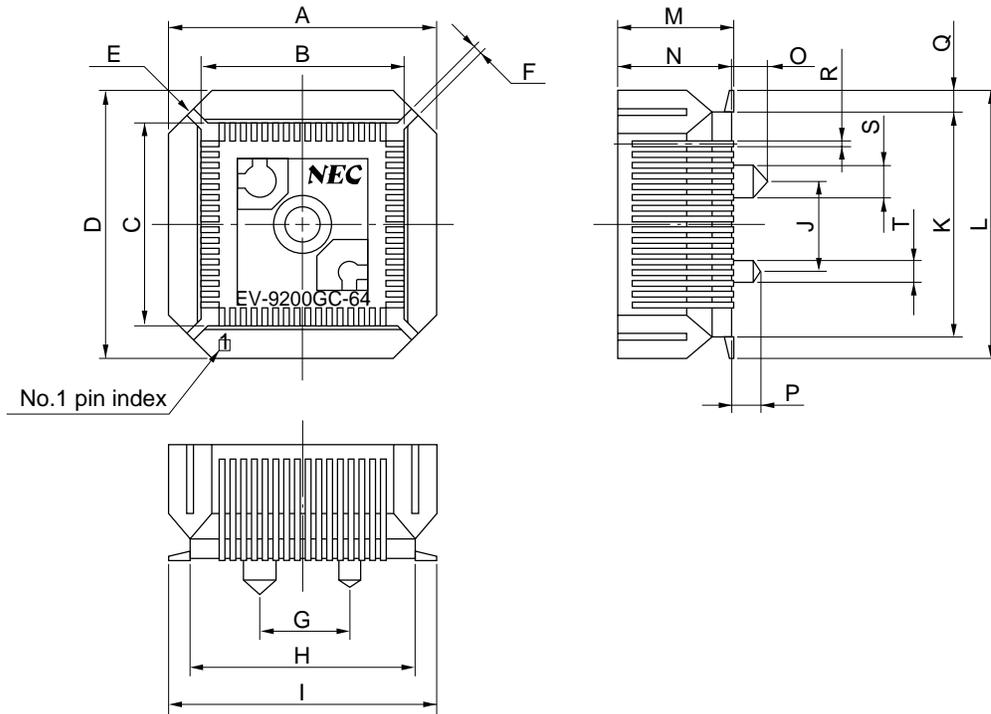
- The ID-78K0-NS, ID78K0, and SM78K0 are used in combination with the DF780034.
- The CC78K/0 and RX78K/0 are used in combination with the RA78K/0 and the DF780034.
- The Flashpro II, FA-64CW, FA-64GC, FA64GK, NP-64CW, NP64GC, and NP-64GK are products made by Naitou Densei Machidaseisakusho (044-822-3813).  
Contact an NEC distributor regarding the purchase of these products.
- The TGK-064SBW is a product made by TOKYO ELETECH CORPORATION.  
Refer to: Daimaru Kogyo, Ltd.  
Tokyo Electronic Components Division (03-3820-7112)  
Osaka Electronic Components Division (06-244-6672)
- For third party development tools, see the **78K/0 Series Selection Guide (U11126E)**.
- The host machines and OSs supporting each software are as follows.

Software	Host Machine [OS]	PC	EWS
		PC-9800 series [Windows™] IBM PC/AT or compatibles [Japanese/English Windows]	HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™] NEWS™ (RISC) [NEWS-OS™]
RA78K/0		√ <sup>Note</sup>	√
CC78K/0		√ <sup>Note</sup>	√
ID78K0-NS		√	—
ID78K0		√	√
SM78K0		√	—
RX78K/0		√ <sup>Note</sup>	√
MX78K0		√ <sup>Note</sup>	√

**Note** DOS-based software

★ Conversion Socket Drawing (EV-9200GC-64) and Footprints

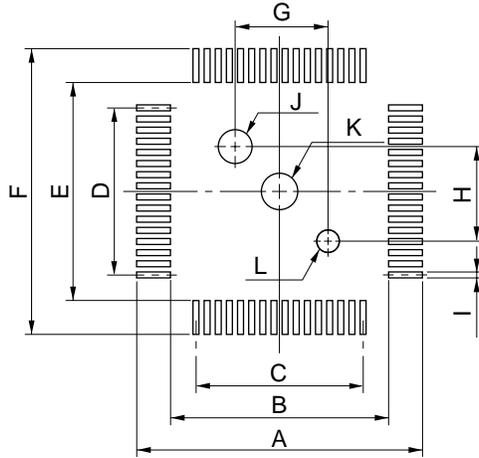
Figure A-1. EV-9200GC-64 Drawing (for reference only)



EV-9200GC-64-G0

ITEM	MILLIMETERS	INCHES
A	18.8	0.74
B	14.1	0.555
C	14.1	0.555
D	18.8	0.74
E	4-C 3.0	4-C 0.118
F	0.8	0.031
G	6.0	0.236
H	15.8	0.622
I	18.5	0.728
J	6.0	0.236
K	15.8	0.622
L	18.5	0.728
M	8.0	0.315
N	7.8	0.307
O	2.5	0.098
P	2.0	0.079
Q	1.35	0.053
R	0.35±0.1	0.014 <sup>+0.004</sup> <sub>-0.005</sub>
S	φ2.3	φ0.091
T	φ1.5	φ0.059

Figure A-2. EV-9200GC-64 Footprints (for reference only)



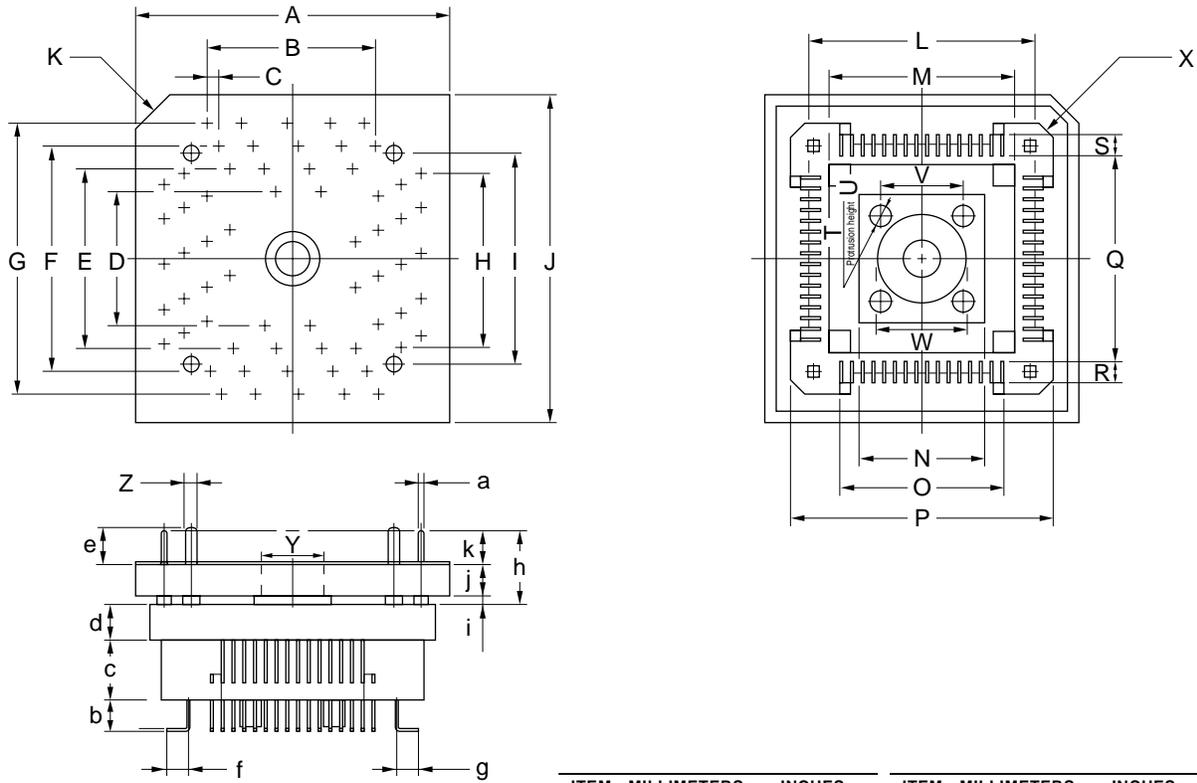
EV-9200GC-64-P1E

ITEM	MILLIMETERS	INCHES
A	19.5	0.768
B	14.8	0.583
C	$0.8 \pm 0.02 \times 15 = 12.0 \pm 0.05$	$0.031^{+0.002}_{-0.001} \times 0.591 = 0.472^{+0.003}_{-0.002}$
D	$0.8 \pm 0.02 \times 15 = 12.0 \pm 0.05$	$0.031^{+0.002}_{-0.001} \times 0.591 = 0.472^{+0.003}_{-0.002}$
E	14.8	0.583
F	19.5	0.768
G	$6.00 \pm 0.08$	$0.236^{+0.004}_{-0.003}$
H	$6.00 \pm 0.08$	$0.236^{+0.004}_{-0.003}$
I	$0.5 \pm 0.02$	$0.197^{+0.001}_{-0.002}$
J	$\phi 2.36 \pm 0.03$	$\phi 0.093^{+0.001}_{-0.002}$
K	$\phi 2.2 \pm 0.1$	$\phi 0.087^{+0.004}_{-0.005}$
L	$\phi 1.57 \pm 0.03$	$\phi 0.062^{+0.001}_{-0.002}$

**Caution** Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E).

★ Conversion Adapter Drawing (TGK-064SBW)

Figure A-3. TGK-064SBW Drawing (for reference only)



ITEM	MILLIMETERS	INCHES	ITEM	MILLIMETERS	INCHES
A	18.4	0.724	a	φ0.3	φ0.012
B	0.65x15=9.75	0.026x0.591=0.384	b	1.85	0.073
C	0.65	0.026	c	3.5	0.138
D	7.75	0.305	d	2.0	0.079
E	10.15	0.400	e	3.9	0.154
F	12.55	0.494	f	1.325	0.052
G	14.95	0.589	g	1.325	0.052
H	0.65x15=9.75	0.026x0.591=0.384	h	5.9	0.232
I	11.85	0.467	i	0.8	0.031
J	18.4	0.724	j	2.4	0.094
K	C 2.0	C 0.079	k	2.7	0.106
L	12.45	0.490			
M	10.25	0.404			
N	7.7	0.303			
O	10.02	0.394			
P	14.92	0.587			
Q	11.1	0.437			
R	1.45	0.057			
S	1.45	0.057			
T	4-φ1.3	4-φ0.051			
U	1.8	0.071			
V	5.0	0.197			
W	φ5.3	φ0.209			
X	4-C 1.0	4-C 0.039			
Y	φ3.55	φ0.140			
Z	φ0.9	φ0.035			

TGK-064SBW-G0E

Note: Product made by TOKYO ELETECH Corporation.

★ APPENDIX B. RELATED DOCUMENTS

Device Related Documents

Document Name	Document No. (English)	Document No. (Japanese)
μPD780024, 780024Y, 780034, 780034Y Subseries User's Manual	U12022E	U12022J
μPD780031Y, 780032Y, 780033Y, 780034Y Data Sheet	U12166E	U12166J
μPD78F0034Y Data Sheet	This document	U11994J
78K/0 Series User's Manual-Instruction	U12326E	U12326J
78K/0 Series Instruction Table	—	U10903J
78K/0 Series Instruction Set	—	U10904J
μPD780034Y Subseries Special Function Register Table	—	To be prepared

Development Tool Documents (User's Manual)

Document Name	Document No. (English)	Document No. (Japanese)
RA78K0 Assembler Package	Operation	U11802E U11802J
	Assembly Language	U11801E U11801J
	Structured Assembly Language	U11789E U11789J
RA78K Series Structured Assembler Preprocessor	EEU-1402	U12323J
CC78K0 C Compiler	Operation	U11517E U11517J
	Language	U11518E U11518J
CC78K/0 C Compiler Application Note	Programming Know-how	EEA-1208 U13034J
CC78K Series Library Source File	U12322E	U12322J
IE-78K0-NS	To be prepared	To be prepared
IE-78001-R-A	To be prepared	To be prepared
IE-780034-NS-EM1	To be prepared	To be prepared
EP-78240	U10332E	EEU-986
EP-78012GK-R	EEU-1538	EEU-5012
SM78K0 System Simulator-Windows based	Reference	U10181E U10181J
SM78K Series System Simulator	External Part User Open Interface Specifications	U10092E U10092J
ID78K0-NS Integrated Debugger	Reference	To be prepared U12900J
ID78K0 Integrated Debugger — EWS based	Reference	— U11151J
ID78K0 Integrated Debugger — PC based	Reference	U11539E U11539J
ID78K0 Integrated Debugger — Windows based	Guide	U11649E U11649J

**Caution** The above related documents are subject to change without notice. Be sure to read the latest documents before designing.

**Embedded Software Documents (User's Manual)**

Document Name		Document No. (English)	Document No. (Japanese)
78K/0 Series Real-time OS	Basics	U11537E	U11537J
	Installation	U11536E	U11536J
78K/0 Series OS MX78K0	Basics	U12257E	U12257J

**Other Documents**

Document Name	Document No. (English)	Document No. (Japanese)
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535E	C10535J
Quality Grades on NEC Semiconductor Devices	C11531E	C11531J
NEC Semiconductor Device Reliability/Quality Control System	C10983E	C10983J
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E	C11892J
Guide to Quality Assurance for Semiconductor Devices	MEI-1202	—
Microcomputer Product Series Guide	—	U11416J

**Caution** The above related documents are subject to change without notice. Be sure to read the latest documents before designing.

[MEMO]

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

**Note:** Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

**Note:** No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

**Note:** Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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