SGS-THOMSON MICROELECTRONICS

TH6P04T6V5CL
TH6P04T25CL

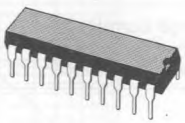
TRANSIL ARRAY FOR DATA LINE PROTECTION

DESCRIPTION

Developed specially for data line protection at the PC Board Level, the component offers 8 protective Bidirectionnal devices with common bus connections per package.

In addition to the parallel protection given by the Transils ®, the pin-die connection wires provide a serie protection in case of short circuit on the line. Therefore this device is a feature of 8 serie/parallel protection elements.

The dual in line design allows compatible packaging for microprocessors, memories and controllers.



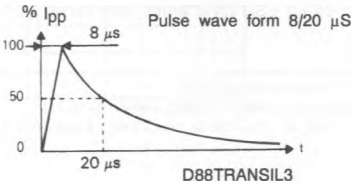
DIP-20
(Plastic)

ABSOLUTE RATINGS (limiting values) ($0°C \leq T_{amb} \leq 70\ °C$)

Symbol	Parameter		Value	Unit
I_{pp}	Peak Pulse Power for 8.20 µs Exponential Pulse	See note 1	40	A
I^2t	Wire I^2t Value	See note 1	0.6	A^2s
ESD	Electrostatic Overstress	See note 2	25	kV
T_{stg} T_j	Storage and Junction Temperature Range		– 55 to 150 125	°C °

Notes : 1. For surges upper than the maximum value specified, the input/output will present first a short circuit to the common bus line and after an open circuit caused by the wire

2. According to MIL STD 883C method 3015-2.

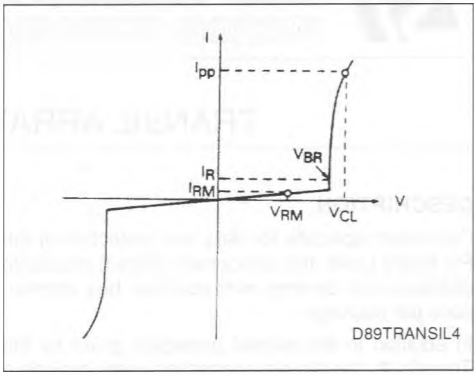


D88TRANSIL3

ELECTRICAL CHARACTERISTICS

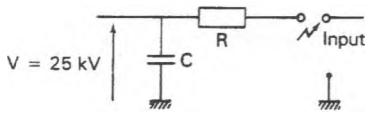
$0\ °C \leq T_{amb} = T_j \leq 70\ °C$

Symbol	Parameter
V_{RM}	Stand-off Voltage
V_{BR}	Breakdown Voltage
V_{CL}	Clamping Voltage
I_{RM}	Leakage Current @ V_{RM}
I_{pp}	Surge Current
C	Input Capacitance



Symbol	Test Conditions	Types	Min.	Typ.	Max.	Unit
V_{BR}	$I_R = \pm 1$ mA	TH6P04T6V5CL	± 6.5			V
		TH6P04T25CL	± 25			
I_{RM}	$V_{RM} = \pm 6$ V	TH6P04T6V5CL			± 50	µA
	$V_{RM} = \pm 24$ V	TH6P04T25CL			± 10	
C1	Each Input Pin to Ground at 0 V Bias	TH6P04T6V5CL			700	pF
		TH6P04T25CL			500	
C2	Each Input Pin to Ground at 5 V Bias	TH6P04T6V5CL			500	pF
		TH6P04T25CL			300	
$V_{CL}1$	$I_{pp} = 40$ A 8-20 µs to all Inputs Sequentially (see note 1)	TH6P04T6V5CL			± 12	V
		TH6P04T25CL			± 38	
$V_{CL}2$	8-20 µs Simultaneously 80 A peak pulse current to all inputs with a 10 Ω resistor in serie. (see note 1)	TH6P04T6V5CL			± 12	V
		TH6P04T25CL			± 35	
$V_{CL}3$	25 kV ESD Overstress (see notes 1-2)	TH6P04T6V5CL			± 12	V
		TH6P04T25CL			± 35	

Notes : 1. V_{CL} mesured on outputs.
2. According to MIL STD 883C method 3015-2.
C = 150 pF R = 150 Ω F = 10 Hz Exposure = 5 secs.



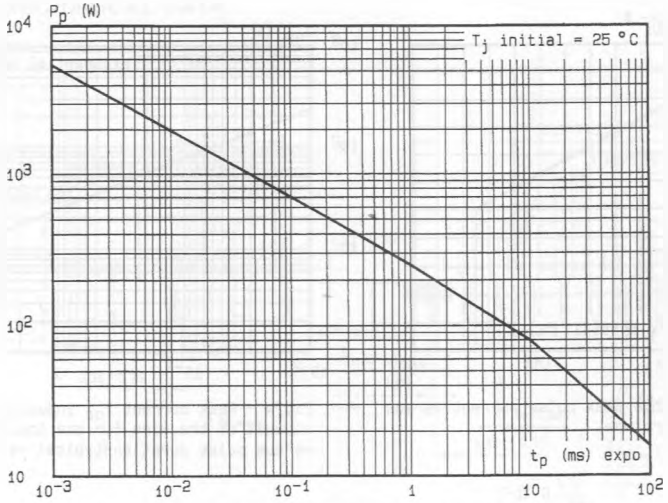


Fig.1 - Peak pulse power versus exponential pulse duration.

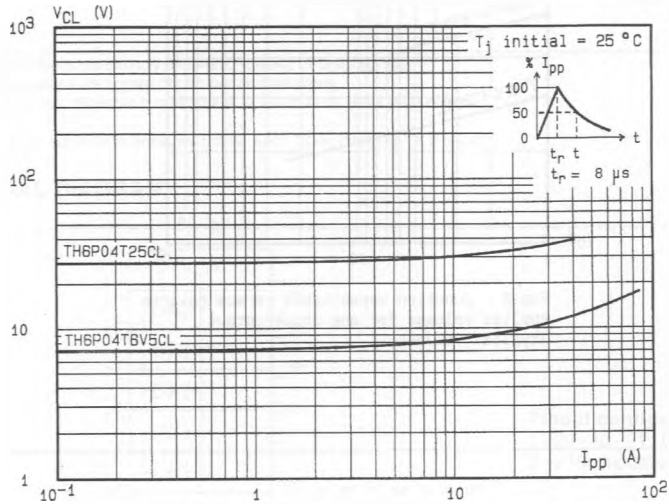


Fig.2 - Clamping voltage versus peak pulse current exponential waveform t = 20 µs.

Note : The curves of the figure 2 are specified for a junction temperature of 25 °C before surge. The given results may be extrapolated for other junction temperatures by using the following formula : $\Delta V_{(BR)} = \alpha_{T(V(BR))} \times [T_j - 25] \times V_{(BR)}$
For intermediate voltages, extrapolate the given results.

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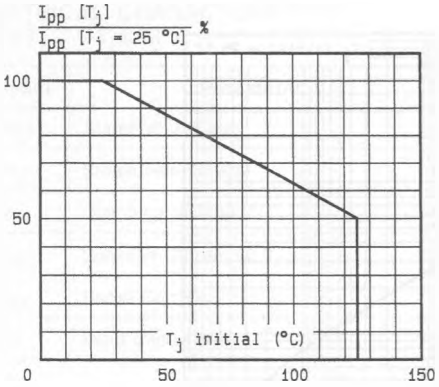

Fig.3 - Allowable peak pulse current versus junction temperature.

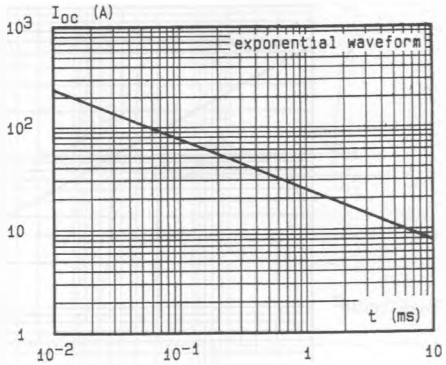

Fig.4 - Peak current I_{OC} inducing open circuit of the wire for one input/output versus pulse duration (typical values).

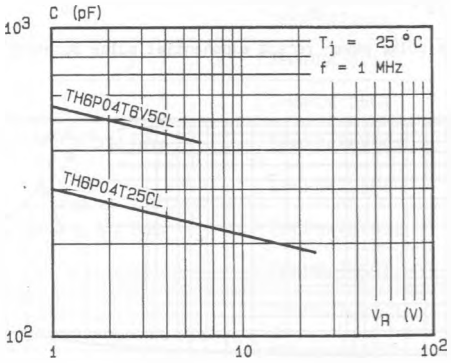

Fig.5 - Junction capacitance versus reverse applied voltage for one input/output (typical values).

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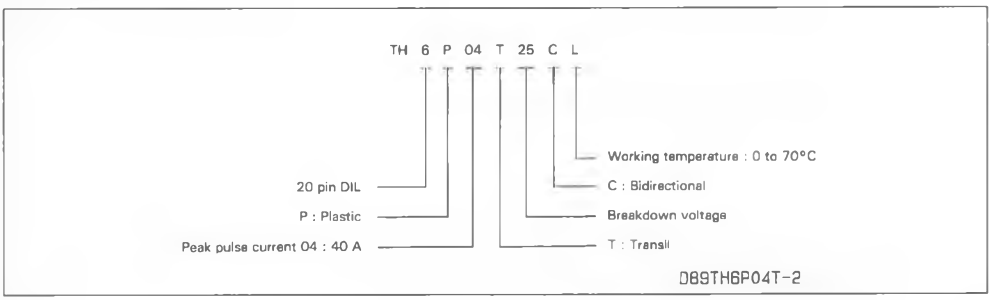
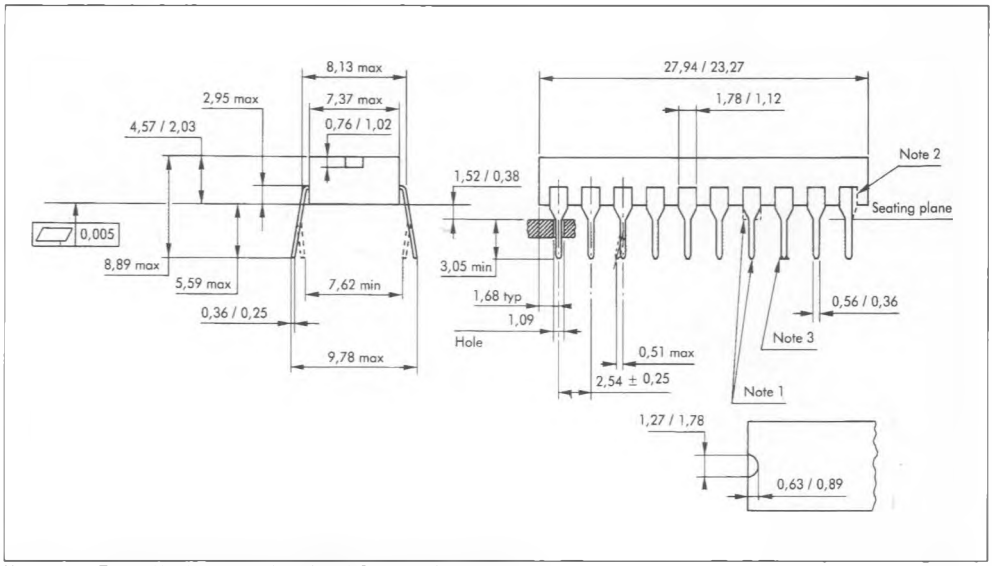
ORDER CODE



PACKAGE MECHANICAL DATA

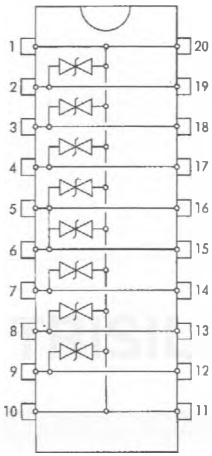
DIP-20 Plastic



Notes : 1. Tapered leads are strongly preferred. Squared off is acceptable.
2. Half shoulders are acceptable on four end leads only.
3. On blunt tips, allowable burr or spur is .003 in max on either sude of lead.

Packaging : Products supplied in antistatic tubes. Each tubes contains 18 products.

FUNCTIONNAL DIAGRAM



Pinout configuration :
1 - 20 - 10 - 11 : GND
2 → 19 : Inputs/outputs