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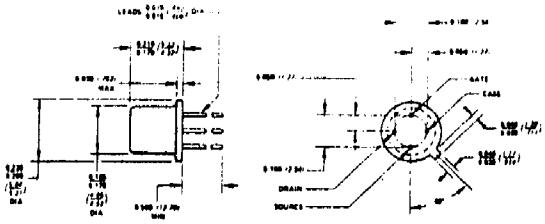
2N4117 2N4119 2N4118
2N4117A 2N4119A 2N4118A

N-CHANNEL SILICON JUNCTION FIELD-EFFECT TRANSISTORS

FOR VERY LOW INPUT CURRENT DC AMPLIFIERS

- I_{GSS} < 1 pA (2N4117A Series)
- I_{GSS} < 10 pA (2N4117 Series)



JEDEC TO-72
Fourth lead is in electrical contact with case.

PRODUCT CONDITIONING

Units receive the following treatment before final electrical tests:

High Temp Storage: 24 Hours at 150°C
Thermal Shock: +100 to 0°C for 5 Cycles
25,000g Acceleration/Impact in the Y_1 Plane
Helium and/or Gross Leak Tests for Hermeticity

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) ..... -40 V
Gate-Current ..... 50 mA
Total Device Dissipation (Derate 2 mW/°C to 175°C) ..... 300 mW
Storage Temperature Range ..... -65 to +175°C
Lead Temperature 1/16" from Case for 10 sec ..... 255°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic		Test Conditions		2N4117 2N4117A Min	2N4117 2N4117A Max	2N4118 2N4118A Min	2N4118 2N4118A Max	2N4119 2N4119A Min	2N4119 2N4119A Max	Unit
I_{GSS}	Gate Reverse Current 2N4117 Series Only	V_{GS} = -20 V, V_{DS} = 0	25°C		-10		-10		-10	pA
			150°C		-25		-25		-25	nA
I_{GSS}	Gate Reverse Current 2N4117A Series Only	V_{GS} = -20 V, V_{DS} = 0	25°C		-1		-1		-1	pA
			150°C		-2.5		-2.5		-2.5	nA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = -1 μA, V_{DS} = 0		-40		-40		-40		V
V_P	Gate-Source Pinch-Off Voltage	V_{DS} = 10 V, I_D = 1 nA		-0.6	-1.8	-1	-3	-2	-6	V
I_{DSS}	Drain Current at Zero Gate Voltage (Note 2)	V_{DS} = 10 V, V_{GS} = 0		0.03	0.09	0.08	0.24	0.20	0.60	mA
g_{fs}	Common-Source Forward Transconductance (Note 2)	V_{DS} = 10 V, V_{GS} = 0, f = 1 kHz		70	210	80	250	100	330	μmho
g_{oss}	Common-Source Output Conductance	V_{DS} = 10 V, V_{GS} = 0, f = 1 kHz			3		5		10	μmho
C_{iss}	Common-Source Input Capacitance	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz			3		3		3	pF
C_{rss}	Common-Source Reverse Transfer Capacitance	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz			1.5		1.5		1.5	pF

NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. This parameter is measured during a 2 ms interval 100 ms after power is applied. (Not a JEDEC condition.)

*JEDEC registered data.