

2N5114JAN/JANTX/JANTXV
2N5115JAN/JANTX/JANTXV
2N5116JAN/JANTX/JANTXV

Product Summary

Part Number	V _{GS(off)} (V)	r _{DS(on)} Max (Ω)	I _{D(off)} Typ (pA)	t _{ON} Max (ns)
2N5114	5 to 10	75	-10	16
2N5115	3 to 6	100	-10	30
2N5116	1 to 4	150	-10	42

Features

- Low On-Resistance: 2N5114 <75 Ω
- Fast Switching—t_{ON}: 16 ns
- High Off-Isolation—I_{D(off)}: -10 pA
- Low Capacitance: 6 pF
- Low Insertion Loss

Benefits

- Low Error Voltage
- High-Speed Analog Circuit Performance
- Negligible “Off-Error,” Excellent Accuracy
- Good Frequency Response
- Eliminates Additional Buffering

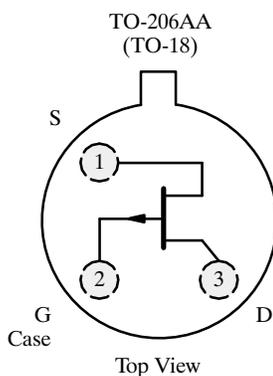
Applications

- Analog Switches
- Choppers
- Sample-and-Hold
- Normally “On” Switches
- Current Limiters

Description

The 2N5114JAN/JANTX/JANTXV series consists of p-channel JFET analog switches designed to provide low on-resistance, good off-isolation, and fast switching.

These JFETs are optimized for use in complementary switching applications with the Siliconix 2N4856A series.



Absolute Maximum Ratings

Gate-Drain Voltage	30 V
Gate-Source Voltage	30 V
Gate Current	-50 mA
Storage Temperature	-65 to 200°C
Operating Junction Temperature	-55 to 200°C

Lead Temperature (¹ / ₁₆ " from case for 10 sec.)	300°C
Power Dissipation ^a	500 mW

Notes
a. Derate 3 mW/°C above 25°C

2N5114JAN/JANTX/JANTXV Series

TEMIC

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Specifications^a

Parameter	Symbol	Test Conditions	Typ ^b	Limits						Unit	
				2N5114		2N5115		2N5116			
				Min	Max	Min	Max	Min	Max		
Static											
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	$I_G = 1 \mu A, V_{DS} = 0 V$	45	30		30		30		V	
Gate-Source Cutoff Voltage	$V_{GS(off)}$	$V_{DS} = -15 V, I_D = -1 nA$		5	10	3	6	1	4		
Saturation Drain Current ^c	I_{DSS}	$V_{GS} = 0 V$	$V_{DS} = -18 V$	-30	-90					mA	
			$V_{DS} = -15 V$			-15	-60	-5	-25		
Gate Reverse Current	I_{GSS}	$V_{GS} = 20 V, V_{DS} = 0 V$	$T_A = 150^\circ C$	5		500		500		pA	
				0.01		1		1		1	μA
Gate Operating Current ^d	I_G	$V_{DG} = -15 V, I_D = -1 mA$	-5								
Drain Cutoff Current	$I_{D(off)}$	$V_{DS} = -15 V$	$V_{GS} = 12 V$	-10		-500				pA	
			$V_{GS} = 7 V$	-10				-500			
			$V_{GS} = 5 V$	-10					-500		
		$V_{DS} = -15 V$ $T_A = 150^\circ C$	$V_{GS} = 12 V$	-0.02		-1					μA
			$V_{GS} = 7 V$	-0.02				-1			
			$V_{GS} = 5 V$	-0.02					-1		
Drain-Source On-Voltage	$V_{DS(on)}$	$V_{GS} = 0 V$	$I_D = -15 mA$	-1.0		-1.3				V	
			$I_D = -7 mA$	-0.7				-0.8			
			$I_D = -3 mA$	-0.5					-0.6		
Drain-Source On-Resistance	$r_{DS(on)}$	$V_{GS} = 0 V, I_D = -1 mA$			75		100		150	Ω	
Gate-Source Forward Voltage	$V_{GS(F)}$	$I_G = -1 mA, V_{DS} = 0 V$	-0.7		-1		-1		-1	V	
Dynamic											
Drain-Source On-Resistance	$r_{ds(on)}$	$V_{GS} = 0 V, I_D = 0 mA, f = 1 kHz$			75		100		175	Ω	
Common-Source Input Capacitance	C_{iss}	$V_{DS} = -15 V, V_{GS} = 0 V$ $f = 1 MHz$	20		25		25		27	pF	
Common-Source Reverse Transfer Capacitance	C_{rss}	$V_{DS} = 0 V$ $f = 1 MHz$	$V_{GS} = 12 V$	5		7					
			$V_{GS} = 7 V$	6				7			
Turn-On Time	$t_{d(on)}$	See Switching Circuit			6		10		25	ns	
	t_r				10		20		35		
Turn-Off Time	$t_{d(off)}$				6		8		20		
	t_f				15		30		60		

Notes

- $T_A = 25^\circ C$ unless otherwise noted.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- Pulse test: $PW \leq 300 \mu s$ duty cycle $\leq 3\%$.
- This parameter not registered with JEDEC.

PSCIA

Switching Time Test Circuit

	2N5114	2N5115	2N5116
V_{DD}	-10 V	-6 V	-6 V
V_{GG}	20 V	12 V	8 V
R_L^*	430 Ω	910 Ω	2000 Ω
R_G^*	100 Ω	220 Ω	390 Ω
$I_{D(on)}$	-15 mA	-7 mA	-3 mA
$V_{GS(H)}$	0 V	0 V	0 V
$V_{GS(L)}$	-11 V	-7 V	-5 V

*Non-inductive

Input Pulse

Rise Time < 1 ns
 Fall Time < 1 ns
 Pulse Width 100 ns
 PRF 1 MHz

Sampling Scope

Rise Time 0.4 ns
 Input Resistance 10 M Ω
 Input Capacitance 1.5 pF

See Typical Characteristics curves for changes.

